Systematic Memory Test Generation for DRAM Defects Causing Two Floating Nodes

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Abstract: *The high complexity of the faulty behavior observed in DRAMs is caused primarily by the presence of internal floating nodes in defective DRAMs. This paper describes a new analysis method to apply electrical simulation for investigating the faulty behavior resulting from defects causing two floating nodes within the memory. The paper also presents the results of a simulation study performed on bit line opens to validate the newly proposed method, and suggests a test to detect these bit line opens.*

Key words: *DRAMs, dynamic faults, two floating nodes, defect simulation, memory testing.*

1 Introduction

DRAMs are memory devices that store information in the form of floating electrical charge in an isolated storage capacitor, which is expected to retain this stored charge for a specific amount of time. In a defect free DRAM, charging and discharging the storage capacitor takes place in a proper way according to specifications. In a defective DRAM, on the other hand, the charge storage behaves in a manner that is difficult to predict at design time. Therefore, specific simulation-based analysis of the faulty behavior is needed to provide the required understanding of the behavior and subsequently help generate an efficient test to detect it.

The fact that DRAMs have a floating charge in the storage capacitor makes the faulty behavior difficult to analyze, since the voltage of the floating node depends on previously performed memory operations. This makes the faulty behavior dependent not only on the memory operation currently performed, but also on the previous history of the memory. The situation is further exacerbated when a memory defect creates more floating lines in the memory, each of which adds to the complex dependence of the current memory behavior on its previous history. Direct measurement of stored cell voltages and other floating node voltages in DRAMs is a rather complex task [Vollrath97, Vollrath02], which means that electrical simulation is important to understand the faulty behavior.

Previous work on applying simulation to understand the faulty behavior of memories has either been limited to a small number of performed operations [Naik93], or to specific types of expected faults [Adams96] in order to limit simulation time. One more general study has been able to analyze the total faulty behavior resulting from only *one* floating node in the memory (stored cell voltage) [Al-Ars02]. This paper introduces a simulation based fault analysis approach that allows for the approximation of the behavior of a defective memory with *two* independent floating nodes.

The paper begins with Section 2 where the memory simulation model used throughout the paper is presented. Section 3 discusses the one-dimensional fault analysis method used to evaluate the faulty behavior of defective memories containing only one floating node. Section 4 introduces the new two-dimensional analysis method to perform the fault analysis on memories with two floating nodes. Then, Section 5 presents the results of applying the new analysis method on a number of memory defects. The paper ends with the conclusions in Section 6.

2 DRAM simulation model

The simulation model used in this paper is based on a design-validation model of an actual DRAM produced by Infineon Technologies. Since the time needed for simulating a complete memory model is excessively long, the simulation model used in our analysis is simplified, taking two factors into consideration in order to preserve the model accuracy and usefulness. First, removed components should be electrically compensated, and second, the resulting simplified circuit should describe enough of the memory to enable injecting and simulating the defects of interest.

Figure 1 shows a block diagram of the bit line pair to

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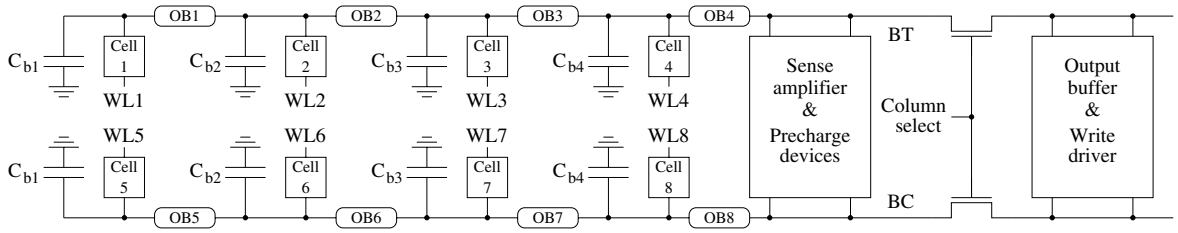


Figure 1. Block diagram of the bit line pair used for simulation.

be simulated. (The blocks labeled OB1, OB2, etc., are locations of opens on bit lines, as discussed in Section 5. In a defect free model, these blocks represent zero resistance on the bit lines.) This simplified simulation model contains a 4×2 cell array with nMOS access transistors, in addition to a sense amplifier and precharge devices. The removed memory cells are compensated for by capacitances of different values distributed along the bit line. External to the bit line pair, the simulation model contains one data output buffer needed to examine data on the output, and a write driver needed to perform write operations.

At the beginning of each simulation run, cell capacitances (C_s) are initialized to the voltage level corresponding to the logic value they are supposed to store; bit line capacitances (C_b) are set to the precharge voltage (equals $\frac{V_{dd}}{2}$); and the data output buffer is forced to contain a logic 1 at the true side.

3 One dimensional analysis

This section describes the one dimensional analysis method to analyze the dynamic faulty behavior of defective DRAMs with one floating node [Al-Ars02]. Consider the defective DRAM cell shown in Figure 2, where a resistive open (R_{op}) between BT (true bit line) and the access transistor limits the ability to control and observe the voltage across the cell capacitor (V_c). The open is injected into Cell 1 and simulated as part of the reduced memory model shown in Figure 1. The analysis takes a range of possible open resistances 10 kΩ $\leq R_{op} \leq$ 10 MΩ, and a range of possible cell voltages (GND $\leq V_c \leq V_{dd}$) into consideration.

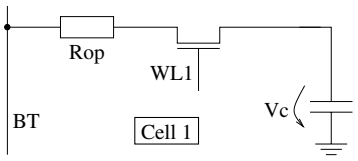


Figure 2. Open injected into Cell 1.

Three different (V_c, R_{op}) result planes are generated, one for each memory operation ($w0$, $w1$, and r). These result planes describe the impact of successive $w0$, successive $w1$, and successive r operations on V_c, for a given value of R_{op}. Read and write operations described here refer to single-cycle operations, where a cell is accessed, read or written, then disconnected, and followed by a memory precharge. Figure 3 shows an automatically generated result plane corresponding to a $w0$ operation, while Figure 4 shows the result plane corresponding to a $w1$ operation, for the open R_{op} shown in Figure 2.

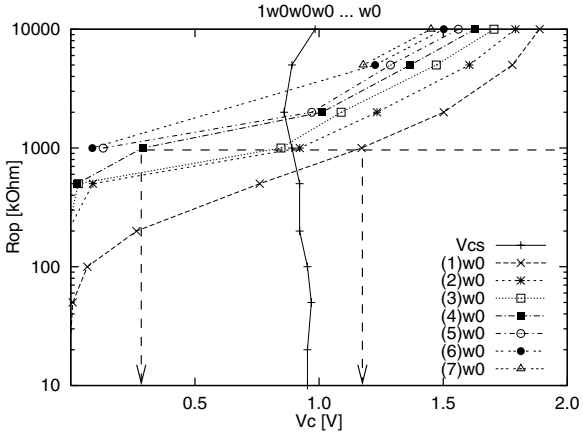


Figure 3. Result plane corresponding to $w0$.

Plane of $w0$: This result plane is shown in Figure 3. To generate this figure, the floating cell voltage V_c is initialized to V_{dd} (because a $w0$ operation is performed) and then the operation sequence $1w0w0...w0$ is applied to the cell. The net result of this sequence is the gradual decrease (depending on the value of R_{op}) of V_c towards GND. The voltage level after each $w0$ operation is recorded on the result plane, resulting in a number of curves. The curves are numbered as $(n)w0$, where n is the number of $w0$ operations needed to get to the curve. For example, the arrows in the figure indicate that, for $R_{op} = 1000$ kΩ, a single $w0$ operation represented by $(1)w0$ pulls V_c from $V_{\rm dd}$ to about 1.2

V, while four $w0$ operations represented by $(4)w0$ pull V_c to about 0.3 V. We stop performing the $w0$ sequence when the voltage change ΔV_c, as a result of $w0$ operations, becomes $\Delta V_c \leq 0.05$ V, which results in identifying up to 7 different $w0$ curves in the plane. Initially, an arbitrary small value for ΔV_c is selected, which can be reduced afterwards if it turns out that more than 7 $w0$ operations are needed to describe the faulty behavior. The sense threshold cell voltage (V_{cs}), shown as a solid line that runs across the center of the figure, is the cell voltage above which the sense amplifier reads a 1, and below which the sense amplifier reads a 0. This curve is generated by performing a read operation for a number of V_c values and recursively identifying the V_c border that distinguishes a 1 and a 0 on the output.

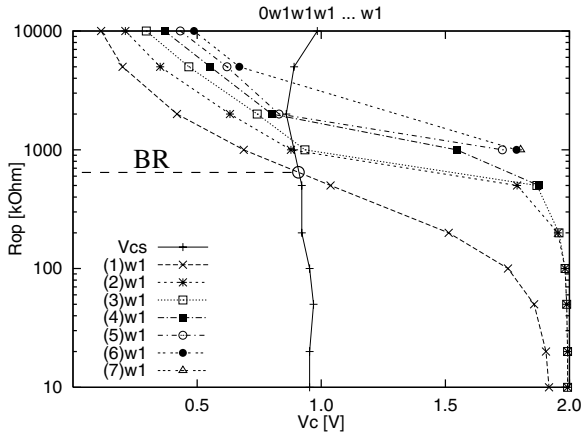


Figure 4. Result plane corresponding to $w1$.

Plane of $w1$: This result plane is shown in Figure 4, and it is generated in the same way the result plane of $w0$ is generated. First, V_c is initialized to GND and then the operation sequence $0w1w1...w1$ is applied to the cell. The result is a gradual increase of V_c towards V_{dd}. The voltage level after each $w1$ operation is recorded on the result plane, which gives a number of curves in the plane. We stop the $w1$ sequence when ΔV_c becomes small enough (0.05 V in this example). V_{cs} is also shown in the figure as a solid line.

It is possible to use the result planes to analyze a number of important aspects of the faulty behavior [Al-Ars02]. One such aspect relevant to this paper is the *border resistance (BR)*, which is the R_{op} value where the cell *starts* to cause faults on the output. BR is derived on the result planes as the resistive value of the intersection point of the first write curve, either $(1)w1$ or $(1)w0$, and the V_{cs} curve. For the faulty behavior shown in Figures 3 and 4, both $(1)w1$ and $(1)w0$ intersect the V_{cs} curve at about 650 kΩ, which also means that BR ≈ 650 kΩ.

Another important aspect relevant to this paper is generating a test that detects the faulty behavior of the defect. Since BR has a value of 650 kΩ, a test should be able to detect faults for defects with a resistance value above, but as close as possible to, BR. If we assume that V_c is initialized to V_{dd}, then a fault is detected by performing a sequence of $w0r0$, while a V_c initialized to GND causes the sequence $w1r1$ to fail. In order to initialize V_c to V_{dd}, a sequence of $w1$ operations is used, and to initialize V_c to GND, a sequence of $w0$ operations is used. Inspecting the result planes at $R_{op} = 650$ kΩ indicates that in the worst case the sequence $w1w1w1w1w1$ charges V_c up to about 1.8 V, while the sequence $w0w0w0w0w0$ discharges V_c to about 0.05 V. It is possible to achieve higher and lower cell voltages by increasing the number of write operations in the initialization sequence, but the more operations are used the less the effect of each added operation becomes. Therefore, there are two possible conditions for detecting R_{op}:

- Cond1: $\Updownarrow(..., w0, w0, w0, w0, w1, r1, ...)$
- Cond0: $\Updownarrow(..., w1, w1, w1, w1, w0, r0, ...)$

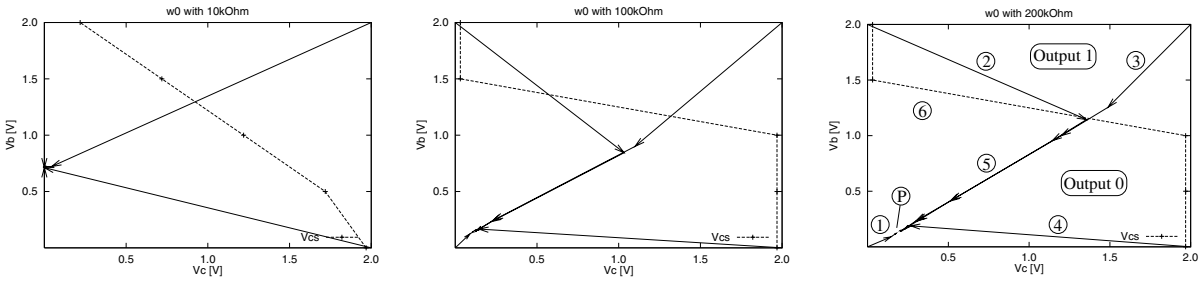
But since $w0$ operations are more able to bring V_c closer to GND than $w1$ operations are able to charge V_c up to V_{dd}, Cond1 is expected to detect defects with lower R_{op} values than Cond0.

4 Two dimensional analysis

This section discusses the new two dimensional analysis used to evaluate the dynamic faulty behavior of defective DRAMs with two floating nodes. Consider the bit line open location OB4 shown in Figure 1, a resistive open (R_{op}) at this location on the bit line reduces the ability of the memory to control the voltage on the left hand side of the bit line and across all cells on BT. We chose to analyze the faulty behavior of OB4 within Cell 4, since OB4 has an identical impact on all cells on BT.

Figure 5 gives a closeup view of the bit line open OB4, where only Cell 4 is shown in addition to the combined bit line capacitor C_b which, in the case of OB4, is equal to C_{b1} + C_{b2} + C_{b3} + C_{b4}. The figure shows that R_{op} causes *two* floating voltages: **(1)** the cell voltage V_c across the cell capacitor C_c, and **(2)** the bit line voltage V_b across the combined parasitic bit line capacitance C_b.

The fact that OB4 causes two floating nodes in the memory, implies that the analysis of the faulty behavior of OB4 should take all possible BT voltages (GND $\leq V_b \leq V_{dd}$) and cell voltages (GND $\leq V_c \leq V_{dd}$) into consideration.



(a) $w0$ plane with R_{op} = 10 kΩ (b) $w0$ plane with R_{op} = 100 kΩ (c) $w0$ plane with R_{op} = 200 kΩ

Figure 6. Simulation results for $w0$ in the (V_c, V_b) planes for (a) 10 kΩ, (b) 100 kΩ and (c) 200 kΩ.

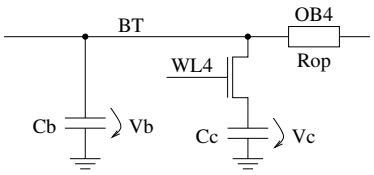


Figure 5. Open defect OB4 on BT.

In addition, the analysis should include a range of possible open resistances (10 kΩ $\leq R_{op} \leq$ 10 MΩ) to inspect the faulty behavior for a number of values of the open resistance. The results of the analysis can be represented as three analysis spaces, one for each memory operation ($w0$, $w1$ and r), where the x-axis of the analysis space stands for V_c, the y-axis stands for V_b, while the z-axis stands for R_{op}. Since it is difficult to visualize 3D figures, it is more convenient to represent the results as a number of (V_c, V_b) planes, one for each R_{op} value, which in turn are organized into three sets, one for each memory operation ($w0$, $w1$ and r).

Planes for $w0$

Figure 6 shows three different (V_c, V_b) planes for three R_{op} values, resulting from performing a sequence of $w0$ operations on the defective memory model shown in Figure 5. For example, Figure 6(c), with $R_{op} = 200$ kΩ, has six main curves numbered in the figure as 1 through 6. Curve 1 is a vector from point $(V_c, V_b) = (0, 0)$ to $(0.13, 0.08)$, describing the impact of performing one $w0$ on a memory initialized to $(0, 0)$. Curves 2, 3 and 4 describe the impact of performing one $w0$ operation on a memory initialized to $(0.0, 2.0)$, $(2.0, 2.0)$ and $(2.0, 0.0)$, respectively. Curve 5 is a bundle of vectors that describe the impact of the sequence $w0w0...w0$ on V_c and V_b. The net effect of performing the $w0$ sequence is the gradual convergence of V_c and V_b voltages to a specific point P $= (0.16, 0.11)$ that is independent of the initialization.

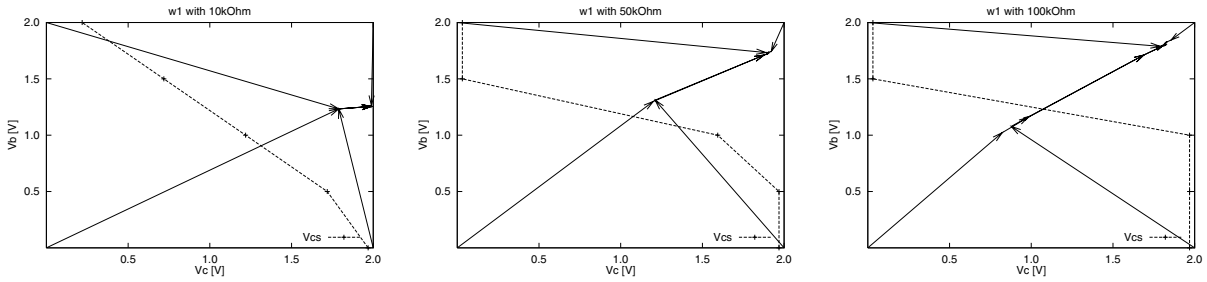
The sequence of $w0$ operations is stopped when the distance ($D = \sqrt{\Delta V_c^2 + \Delta V_b^2}$) between two (V_c, V_b) points resulting from consecutive $w0$ operations becomes less than $D = 0.025$ V, which is shown by simulations to be small enough to represent the faulty behavior. This selection of D is arbitrary at the first iteration of the fault analysis and may later be reduced if a more detailed analysis is required.

Curve 6 in the figure is the sense threshold cell voltage (V_{cs}) curve, which indicates the cell voltage below which the sense amplifier detects a 0 and above which the sense amplifier detects a 1. This curve is generated by initializing V_b to a specific voltage between 0 V and 2.0 V and then identifying the V_c threshold that distinguishes a 0 and a 1 on the output. Five points have been chosen on V_b which result in the following V_{cs} points (identified by a little "+" in the figure): $(1.77, 0.00)$, $(1.77, 0.45)$, $(1.77, 0.90)$, $(0.03, 1.35)$ and $(0.03, 1.80)$. Curve 3 in Figure 6(c) shows that, with an initial $(V_c, V_b) = (2.0, 2.0)$, a single $w0$ operation is not able to discharge V_c low enough for the sense amplifier to detect a 0, which means that $w0$ operations fail with $R_{op} = 200$ kΩ.

Figure 6(a) with $R_{op} = 10$ kΩ and Figure 6(b) with $R_{op} = 100$ kΩ are generated in the same way as Figure 6(c). Figure 6(a) shows that the $w0$ sequence gradually modifies the floating voltages in the memory such that they eventually settle at $(V_c, V_b) = (0.0, 0.7)$, where V_c has the proper $w0$ value of 0.0 V but V_b has a value of 0.7 V that is different from the proper precharge value of 1.0 V. Figure 6(b) shows that the $w0$ sequence results in a voltage equilibrium point of $(0.1, 0.15)$. Both Figures 6(a) and (b) show that, irrespective of the initialization, a single $w0$ operation sets (V_c, V_b) to a value below the V_{cs} curve, which means that $w0$ operations behave properly for 10 kΩ $\leq R_{op} \leq$ 100 kΩ.

Planes for $w1$

Figure 7 shows three different (V_c, V_b) planes for three R_{op} values, resulting from performing a sequence of $w1$ oper-



(a) $w1$ plane with R_{op} = 10 kΩ (b) $w1$ plane with R_{op} = 50 kΩ (c) $w1$ plane with R_{op} = 100 kΩ

Figure 7. Simulation results for $w1$ in the (V_c, V_b) planes for (a) 10 kΩ, (b) 50 kΩ and (c) 100 kΩ.

ations. To generate each plane in the figure, the V_c and V_b voltages are initialized to a given value and then a sequence of $w1w1...w1$ operations is performed on the cell. The net effect is the gradual convergence of V_c and V_b voltages toward a specific point in the (V_c, V_b) plane.

In the example shown in Figure 7, 4 different (V_c, V_b) initializations have been used: $(0.0, 0.0)$, $(2.0, 0.0)$, $(2.0, 2.0)$, and $(0.0, 2.0)$; all values are in volts. The sequence of $w1$ operations is stopped when $D \leq 0.025$ V. In addition to the $w1$ vectors in each result plane, there is also the sense threshold cell voltage (V_{cs}) curve, which indicates the cell voltage (V_c) below which the sense amplifier detects a 0 and above which the sense amplifier detects a 1 for a given value of V_b and R_{op}.

Figure 7(a) with $R_{op} = 10$ kΩ shows that the $w1$ sequence gradually modifies the voltages in the memory toward the point $(V_c, V_b) = (2.0, 1.3)$, which is close to the proper value after $w1$ of $(2.0, 1.0)$. Figure 7(b) shows that, with $R_{op} = 50$ kΩ, the $w1$ sequence gradually modifies memory voltages towards the point $(1.9, 1.7)$. In these two planes, a single $w1$ operation is able to pull V_c up from any initial voltage to a voltage above the V_{cs} curve, which means that with 10 kΩ $\leq R_{op} \leq$ 50 kΩ no fail can be detected on the output.

Figure 6(c) with $R_{op} = 100$ kΩ shows that the $w1$ sequence gradually approaches a voltage point of $(1.8, 1.8)$ that is above the V_{cs} curve, which means that after a sequence of $w1$ operations the memory succeeds in writing a 1 into the cell. However, a single $w1$ operation with an initialization of $(0.0, 0.0)$ or $(2.0, 0.0)$ fails to write a high enough V_c voltage for the sense amplifier to detect a 1. Therefore, $w1$ operations start to fail with an R_{op} value of about 100 kΩ.

BR & detection condition

The result planes in Figures 6 and 7 can be used to identify important aspects of the faulty behavior, such as the value of BR and a detection condition to detect the defective memory.

The result planes indicate that both $w0$ and $w1$ fail for a specific R_{op} value and with some initial conditions. Since $w1$ fails at an open resistance of about 100 kΩ, which is less than the $R_{op} = 200$ kΩ needed for $w0$ to fail, the BR value corresponds to the lower 100 kΩ value.

The failing $w1$ operation can be detected with the sequence $w1r1$, in case V_c and V_b are properly initialized. Figure 7(c) shows that $w1$ fails for an initialization of $(0.0, 0.0)$ and $(0.0, 2.0)$, which means that $w1$ fails as long as V_c is equal to 0.0 V irrespective of the value of V_b. Therefore, in order to force $w1$ to fail for R_{op} as close as possible to BR, V_c should be brought as close as possible to 0.0 V. Figure 6(b) shows that, with $R_{op} = 100$ kΩ and for any initialization, the sequence $w0w0w0w0$ gradually modifies the floating voltages toward the point $(V_c, V_b) = (0.1, 0.15)$, which could be used as an initialization for V_c. In conclusion, the detection condition to detect the bit line open OB4 that ensures the lowest possible failing R_{op} value is $\Updownarrow(..., w0, w0, w0, w0, w1, r1, ...)$. Note that this detection condition is identical to Cond1 derived in Section 3 to detect the cell open of Figure 2. This is due to the similar detrimental impact both defects have on the behavior of the memory.

5 Application results

In this section, the application results of a fault analysis study are presented, where the two dimensional fault analysis is applied as it is described in this paper. The memory model used for the analysis is shown in Figure 1 along with the positions where a number of bit line opens are injected (OB1 through OB8). For each of the defects (OBx), the cell inspected for the faulty behavior is the one with the name Cell x, as shown in the figure. The simulations have been performed using an electrical Spice-based simulator called Titan, developed by Siemens/Infineon.

The results of the analysis are listed in Table 1. The ta-

Table 1. Results of two dimensional fault analysis performed on the memory model of Figure 1

Open	BR	Detection condition	Open	BR	Detection condition
OB1	650 kΩ	$\Updownarrow(..., w0, w0, w0, w0, w1, r1, ...)$	OB5	650 kΩ	$\Updownarrow(..., w1, w1, w1, w1, w0, r0, ...)$
	650 kΩ	$\Updownarrow(..., w1, w1, w1, w1, w0, r0, ...)$		650 kΩ	$\Updownarrow(..., w0, w0, w0, w0, w1, r1, ...)$
OB2	150 kΩ	$\Updownarrow(..., w0, w0, w0, w0, w1, r1, ...)$	OB6	150 kΩ	$\Updownarrow(..., w1, w1, w1, w1, w0, r0, ...)$
OB3	68 kΩ	$\Updownarrow(..., w1, w1, w1, w1, w0, r0, ...)$	OB7	68 kΩ	$\Updownarrow(..., w0, w0, w0, w0, w1, r1, ...)$
OB4	67 kΩ	$\Updownarrow(..., w0, w0, w0, w0, w1, r1, ...)$	OB8	67 kΩ	$\Updownarrow(..., w1, w1, w1, w1, w0, r0, ...)$

ble lists the BR value and the corresponding detection condition to detect the faulty behavior for each of the analyzed defects. Note that the results for the defects injected on BC (complementary bit line) are complemetary to the results for the defects injected on BT, which means that each pair of complementary defects starts to fail at the same BR value and can be detected with a complementary detection condition (same sequence of writes and reads but with 0s replaced by 1s and 1s by 0s).

The table shows that the BR value for the defects OB1 to OB4 decreases monotonically from 650 kΩ for OB1 to 67 kΩ for OB4. This can be explained by noting that OB1 and OB4 represent extreme situations where defects are present on either side of the bit line, while OB2 and OB3 represent intermediate transitions of the defect from OB1 toward OB4. Therefore, it is expected that the BR value would gradually change from that for OB1, through OB2 and OB3, toward the BR value for OB4.

The table also shows that all defects share exactly the same detection condition $\Updownarrow(..., w0, w0, w0, w0, w1, r1, ...)$, which starts with an initialization sequence of four $w0$ operations, followed by the detection sequence of $w1r1$ which fails and results in detecting the defect. The fact that OB2, OB3 and OB4 only fail using the sequence $w1r1$, and not $w0r0$, can be attributed to the fact that an nMOS transistor is used as the access transistor of the memory cell in this design. And since it is more difficult for an nMOS DRAM cell to store a logic 1 than storing a logic 0, it is expected that writing a 1 would be easier to fail than writing a 0.

It is interesting to note that the faulty behavior of OB1 has the same BR value and detection conditions as that of the open within the cell shown in Figure 2 of Section 3. A detailed comparison of both types of faulty behavior shows that they are in fact almost identical because, for open OB1, the floating bit line part has the capacitance C_{b1} (see Figure 1), a capacitance that is very small relative to the cell capacitance. Therefore, it is expected that the faulty behavior of the memory would mainly be influenced by the floating voltage within the cell rather than the floating voltage on the bit line. As a result, the analysis of OB1 is expected to be similar to an analysis of an open within Cell 1.

6 Conclusions

This paper introduced the new two dimensional fault analysis method, that is able to approximate the infinite dynamic faulty behavior of a defective DRAM with two floating nodes. This method facilitates an effective and time efficient analysis of defects taking place outside the memory cell, such as bit line opens and shorts. The two dimensional analysis represents a generalization of the one dimensional analysis introduced previously to analyze defective DRAMs with one floating node [Al-Ars02]. The analysis has been applied to evaluate the faulty behavior of bit line opens where it has been shown to be effective in identifying the border resistance and deriving an appropriate detection condition for the defects. The results are consistent with the experience of the commodity memory testing departments at Infineon Technologies in Munich, Germany.

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