# Optimizing Stresses for Testing DRAM Cell Defects Using Electrical Simulation

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**Abstract:** *Stresses are considered an integral part of any modern industrial DRAM test. This paper describes a novel method to optimize stresses for memory testing, using defect injection and electrical simulation. The new method shows how each stress should be applied to achieve a higher fault coverage of a given test, based on an understanding of the internal behavior of the memory. In addition, results of a fault analysis study, performed to verify the new optimization method, show its effectiveness.*

**Key words:** *stresses, memory testing, test optimization, defect simulation.*

## 1 Introduction

The effectiveness of memory tests does not merely depend on a sequence of write and read operations with the associated data patterns; it heavily employs modifications to various operational parameters or *stresses (STs)*, either to ensure a higher fault coverage of a given test or to target specific failure mechanisms not detected at nominal operational conditions [Falter00]. The STs usually used in testing are temperature, supply voltage and timing [Vollrath00].

Experimental studies on the impact of STs on the faulty behavior show strong correlation between the analyzed defect and STs. Many studies have been performed to optimize a large number of supply voltages at test time [Schanstra99], to simulate the operation of memory tests for different *stress combinations (SCs)* [Goto97], and to simulate the effect of temperature on the faulty behavior [Al-Ars01]. These studies give general conclusions, based on some statistical analysis, that is not representative of the behavior of a particular defect. This makes these methods not particularly useful to optimize STs for industrial production purposes.

This paper proposes a new method to optimize STs, using defect injection and electrical Spice simulation of a memory model. The results are specific to the simulated memory defect, and indicate the direction in which each ST should be driven to get the highest coverage for a given memory test. In addition, the fault analysis results of a number of defects are given to validate the proposed method.

Section 2 of this paper identifies the STs used in optimizing memory tests and describes how Shmoo plots are used to optimize them for a given defect. Section 3 presents the fault analysis approach that makes test optimization, using simulation, possible. Section 4 shows the optimization method proposed in this paper. Section 5 presents the fault analysis results performed to validate the methodology. Section 6 ends with conclusions.

## 2 Stress specification

The exact specification of the used STs depends on the device being tested and the amount of control we have on the internal behavior of the memory. In general, there are three different types of ST used to optimize memory tests: timing, temperature, and voltage.

Almost all recent memory devices are so-called synchronous memories, referring to the fact that all events that take place in the memory are governed by a global clock signal (an input signal to any synchronous memory). For the use of timing as a ST, this clock signal can be modified in two different ways: by changing the period of the clock (also called the cycle time, $t_{cyc}$) or by changing the duty cycle time ($\tau$).

Temperature may also be used as a ST to optimize testing. Temperature has proven to be a very effective ST to bring devices closer to failure. In general, a higher testing temperature results in a higher fault coverage for many tests [vdGoor99].

Supply voltage ($V_{dd}$) is one more ST commonly controlled at test time to increase the fault coverage of memory test. According to memory specification, there is a range within which this voltage may vary ($\pm 10\%$, for example).

A Shmoo plot is an important method used to optimize STs for a given memory test [Baker97], where two STs (S1 and S2) are usually chosen to be optimized in a given range. A test is then applied to the memory and, for each

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combination of S1 and S2, the pass/fail outcome of the test is registered on the Shmoo plot. This creates a two dimensional graphical representation of the pass/fail behavior of the memory under the applied test.

Shmoo plotting has the advantage of direct optimization of a pair of STs for a given test on a chip, in case the chip is known to have the targeted defect. Shmoo plotting suffers, however, from the following disadvantages: possibly long test times, restricted controllability and observability of internal memory parts, and limited diagnostic ability to relate the externally observed memory failure to the internal faulty behavior. For a test designer, attempting to optimize a given test for a specific defect using Shmoo plots, these mentioned problems make optimization a rather difficult and challenging task.

# 3 Fault analysis approach

The single most important development in fault analysis that enables simulation based optimization of STs is the ability to state the *border resistance (BR)* of a defect [Al-Ars02]. BR is the resistive value of a defect at which the memory starts to show faulty behavior. Using this important piece of information, the criterion to optimize any ST can be stated as follows:

**Optimizing a given ST** should modify the value of BR in that direction which maximizes the resistance range that results in a detectable functional fault.

In this section, we describe the approach used to identify the BR of cell defects. Consider the defective DRAM cell shown in Figure 1, where a resistive open ($R_{op}$) reduces the ability to control and observe the voltage across the cell capacitor ($V_c$). The analysis takes a range of possible open resistances (1 k$\Omega \leq R_{op} \leq$ 10 M$\Omega$) and possible cell voltages (GND $\leq V_c \leq V_{dd}$) into consideration.

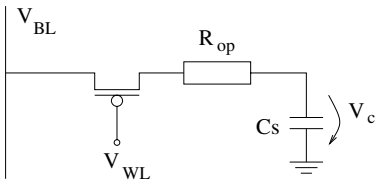


**Figure 1.** Electrical model of memory cell.

Next, a number of $R_{op}$ values are selected for which the analysis is to be performed. Three different $(V_c, R_{op})$ result planes are generated, one for each memory operation ($w0$, $w1$, and $r$). These result planes describe the impact of successive $w0$, successive $w1$, and successive $r$ operations on $V_c$, for a given value of $R_{op}$. Figure 2 shows the three result planes for the three memory operations performed for the open shown in Figure 1.

To generate Figures 2(a) and (b), the floating cell voltage $V_c$ is initialized to $V_{dd}$ for a $w0$ sequence and to GND for a $w1$ sequence, and then the sequence of write operations is performed. The net result of this sequence is the gradual change of $V_c$ towards a settlement point in the plane. The voltage level after each write operation is recorded on the result plane, resulting in a number of curves. Each curve is indicated by an arrow pointing in the direction of the voltage change. The mid-point voltage ($V_{mp}$) (the cell voltage that makes up the border between a stored 0 and 1) is also indicated in the figure with a solid vertical line. The sense amplifier threshold voltage ($V_{sa}$) is shown in the figure as a dotted line. $V_{sa}$ is the cell voltage above which the sense amplifier reads a 1, and below which the sense amplifier reads a 0.

To generate Figure 2(c), first $V_{sa}$ is established and indicated on the result plane (shown as a bold curve in the figure). As $R_{op}$ increases, $V_{sa}$ turns closer to GND which means that it gets easier to detect a 1 and more difficult to detect a 0.[1] Then the sequence $rrr...r$ is applied twice: first for $V_c$ that is initially slightly lower than $V_{sa}$ (0.12 V lower in this example), and a second time for $V_c$ that is slightly higher than $V_{sa}$ (0.12 V higher). The voltage level after each $r$ operation is recorded on the result plane which results in a number of curves on the plane.

It is possible to use the result planes of Figure 2 to analyze a number of important aspects of the faulty behavior [Al-Ars02]. One such aspect relevant to this paper is the value of BR, which is the $R_{op}$ value where the cell *starts* to cause faults on the output. For the faulty behavior shown in Figure 2, BR has a value of 200 k$\Omega$, which is the value of $R_{op}$ at the intersection between the $(1)w0$ curve and the $V_{sa}$ curve (indicated as a dot in Figure 2(a)).

Another aspect relevant to this paper is generating a test that detects the faulty behavior of the defect. In the case of Figure 2, faults can be detected with $R_{op} \geq$ 200 k$\Omega$ using the sequence $w1w1w0r0$. Note that the two $w1$ operations are necessary to charge $V_c$ up fully to $V_{dd}$ when $R_{op}$ has a value close to BR. Performing one $w1$ instead of two, charges $V_c$ up to a voltage below $V_{dd}$, which makes it less demanding for the subsequent $w0$ operation to write a 0.

# 4 Optimization methodology

Optimizing any ST can generally be done by performing a full fault analysis (generating the three result planes as

[1] This is caused by the fact that the precharge cycle sets the bit line voltage to $V_{dd}$. Therefore, as $R_{op}$ increases, a 0 stored in the cell fails to pull the bit line voltage down during a read operation, and the sense amplifier detects a 1 instead of a 0.

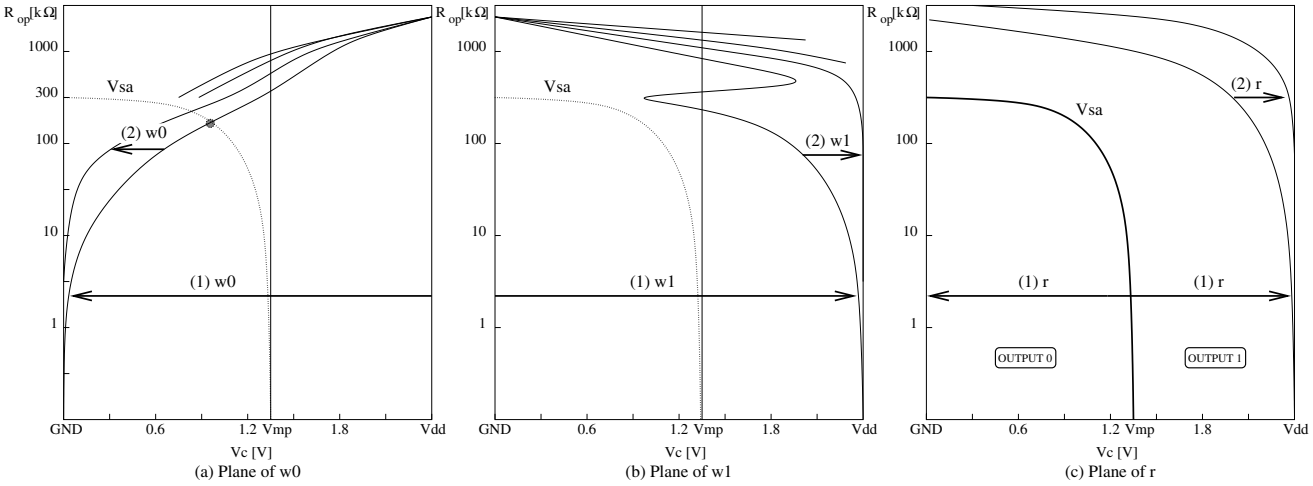


**Figure 2.** Result planes for the operations (a) $w0$, (b) $w1$, and (c) $r$.

shown in Figure 2) for each ST value of interest. The impact of each ST value can be inspected by evaluating the resulting border defect resistance in the way described in Section 3. This method is both labour intensive and time consuming. Fortunately, it is sometimes possible to deduce the impact of different STs on the value of the BR by performing a limited number of simulations only. Below, this method is outlined in an example to optimize STs for the detection condition derived for the open in Figure 1 with respect to $t_{cyc}$, T, and $V_{dd}$.

The result planes in Figure 2 have been generated for $t_{cyc}$ = 60 ns, T = +27° C and $V_{dd}$ = 2.4 V. The planes show that, for nominal STs, the BR has a value of about $R_{op}$ = 200 kΩ. This value is determined by the intersection point of the $(1)w0$ curve and the $V_{sa}$ curve as shown in Figure 2(a). Therefore, increasing the range of the failing $R_{op}$ can be done in two ways:

1. By reducing the ability of $1w0$ to write a low voltage into the cell. This stresses the $1w0$ operation and results in shifting the $(1)w0$ curve to higher $V_c$ voltages.

2.By reducing the range of cell voltages in which $r$ detects a 0. This stresses the $r$ operation and results in shifting the $V_{sa}$ curve to lower $V_c$ voltages.

## 4.1 Optimizing timing

Figure 3 shows the simulation results of reducing $t_{cyc}$ from 60 ns to 55 ns. The figure has two panels: the top is for applying a $1w0$ operation and the bottom for applying a $r$. The $x$-axis in the figure represents the time axis, while the $y$-axis gives the stored cell voltage $V_c$.

**Applying $1w0$:** The top panel outlines the cell voltage $V_c$ while performing a $1w0$ operation with $t_{cyc}$ = 60 ns and 55 ns. In the simulation, the initial cell voltage ($V_{ini}$) is $V_{dd}$ (physical 1), $R_{op}$ = 200 kΩ and T = +27° C. By the end of

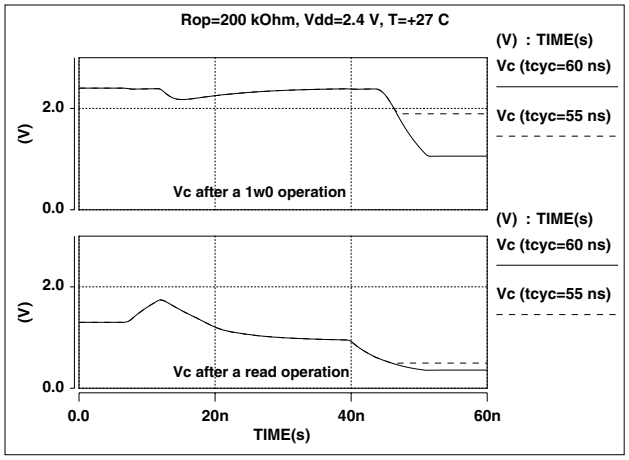


**Figure 3.** Simulation of reducing $t_{cyc}$ from 60 ns to 55 ns with $V_{dd}$ = 2.4 V, $R_{op}$ = 200 kΩ and T = +27° C.

the write operation, the value of $V_c$ is 1.0 V for $t_{cyc}$ = 60 ns, while $V_c$ = 1.9 V for $t_{cyc}$ = 55 ns. This indicates that reducing the cycle time reduces the ability of $1w0$ to write a 0 into the cell. As a result, reducing $t_{cyc}$ is considered as a more stressful condition for the $1w0$ operation.

**Applying $r$:** The bottom panel outlines the cell voltage $V_c$ while performing a $r$ operation with $t_{cyc}$ = 60 ns and 55 ns. In the simulation, $V_{ini}$ = 1.1 V, which is slightly below $V_{sa}$, $R_{op}$ = 200 kΩ and T = +27° C. The figure shows that after about $t$ = 13 ns, $V_c$ is pulled low and a 0 is written back to cell, which means the sense amplifier senses a 0 for both values of $t_{cyc}$. Note that the figure is only important to show the impact of ST on $V_{sa}$ (i.e., whether changing ST promotes detecting 0 or 1); the final of $V_c$ after performing $r$ is not important here. The figure indicates that the ability of the sense amplifier to detect 0 or 1 does not change as a result of changes in timing. This means that timing has no

impact on $V_{sa}$.

In conclusion, decreasing $t_{cyc}$ is more stressful for the $1w0$ operation and has no impact on the detected value of the $r$. Therefore, reducing the cycle time is more stressful for the test.

## 4.2 Optimizing temperature

Figure 4 shows the simulation results with T = $-33°$ C, +27° C and +87° C. The figure has two panels: the top is for applying a $1w0$ operation and the bottom for applying a $r$.

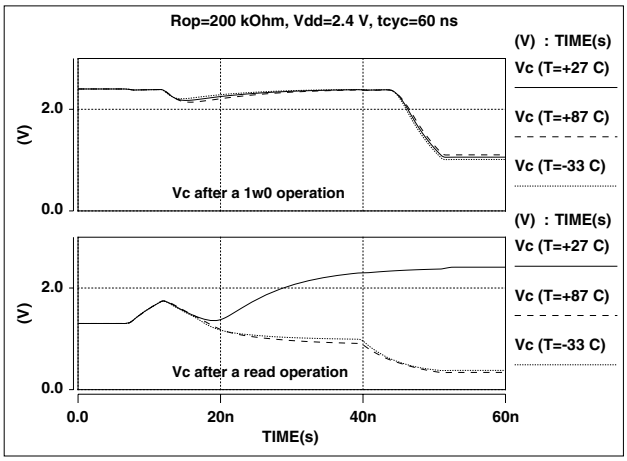


**Figure 4.** Simulation with T = $-33°$ C, +27° C and +87° C, $V_{dd}$ = 2.4 V, $R_{op}$ = 200 kΩ and $t_{cyc}$ = 60 ns.

**Applying $1w0$:** The top panel outlines the cell voltage $V_c$ while performing a $1w0$ operation with T = $-33°$ C, +27° C and +87° C. The simulation used $V_{ini} = V_{dd}$ (physical 1), $R_{op}$ = 200 kΩ and $t_{cyc}$ = 60 ns. By the end of the write operation (at $t$ = 60 ns), the value of $V_c$ is 1.1 V for T = +87° C, $V_c$ = 1.05 V for T = +27°, while $V_c$ = 1.0 V for T = $-33°$ C. This indicates that increasing the temperature reduces the ability of $1w0$ to write a 0 into the cell. This behavior can be attributed to the gradual decrease in drain current as temperature increases, which is in turn caused by the decreasing mobility of charge carriers with increasing T. As a result, increasing T is considered as a more stressful condition for the $1w0$ operation.

**Applying $r$:** The bottom panel outlines $V_c$ while performing a $r$ operation with T = $-33°$ C, +27° C and +87° C. The simulation used an initial cell voltage $V_{ini}$ = 1.3 V, which is slightly above $V_{sa}$, and $R_{op}$ = 200 kΩ. The sense amplifier detects a 1 with T = +27° C, while it detects a 0 both $-33°$ C and +87° C. This is an interesting, rarely observed behavior, where increasing ST changes the stresses in a non-monotonous way (increasing then decreasing). This suggests the presence of multiple temperature-related mechanisms with an opposing effect on the faulty behavior, such as: the increased transistor threshold voltage (promotes detecting 1), the increased drain current (promotes detecting 0), and the decreased leakage current (promotes detecting 0) with decreasing T. This indicates that increasing or decreasing temperature from +27° C shifts the $V_{sa}$ curve to the right. As a result, +27° is considered as a more stressful condition for the $r$ operation.

In conclusion, the most stressful T can either be at room temperature or high temperature. To specify which of these should be selected, the BR has to be identified for high T and compared with the BR for room T. The BR can be identified by performing a number of simulations to construct the $(1)w0$ curve and the $V_{sa}$ curve. This has been done, and the results indicate that high temperature is more effective since it reduces the BR by 5 kΩ.

## 4.3 Optimizing voltage

Figure 5 shows the simulation results with $V_{dd}$ = 2.1 V, 2.4 V and 2.7 V. The figure has two panels: the top is for applying a $1w0$ operation and the bottom for applying a $r$.

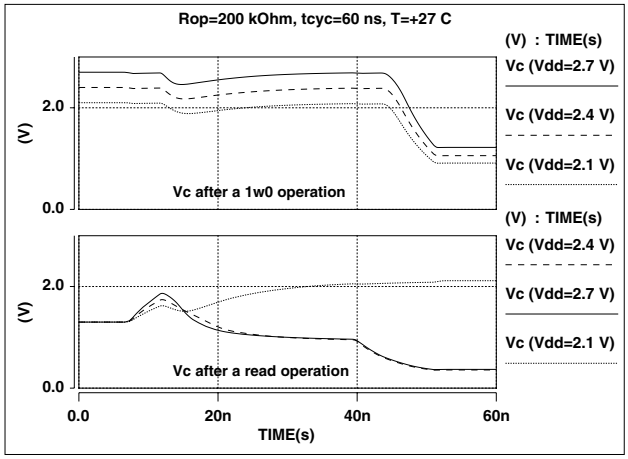


**Figure 5.** Simulation with $V_{dd}$ = 2.1 V, 2.4 V and 2.7 V, $t_{cyc}$ = 60 ns, $R_{op}$ = 200 kΩ and T = +27° C.

**Applying $1w0$:** The top panel outlines the cell voltage $V_c$ while performing a $1w0$ operation with $V_{dd}$ = 2.1 V, 2.4 V and 2.7 V. The simulation used $V_{ini} = V_{dd}$ (physical 1), $R_{op}$ = 200 kΩ and T = +27° C. By the end of the write operation (at $t$ = 60 ns), the value of $V_c$ is 1.0 V for $V_{dd}$ = 2.4 V, $V_c$ = 1.2 V for $V_{dd}$ = 2.7 V, while $V_c$ = 0.9 V for $V_{dd}$ = 2.1 V. This indicates that increasing the supply voltage reduces the ability of $1w0$ to write a 0 into the cell. As a result, increasing $V_{dd}$ is considered as a more stressful condition for the $1w0$ operation.

**Applying $r$:** The bottom panel outlines the cell voltage $V_c$ while performing a $r$ operation with $V_{dd}$ = 2.1 V,

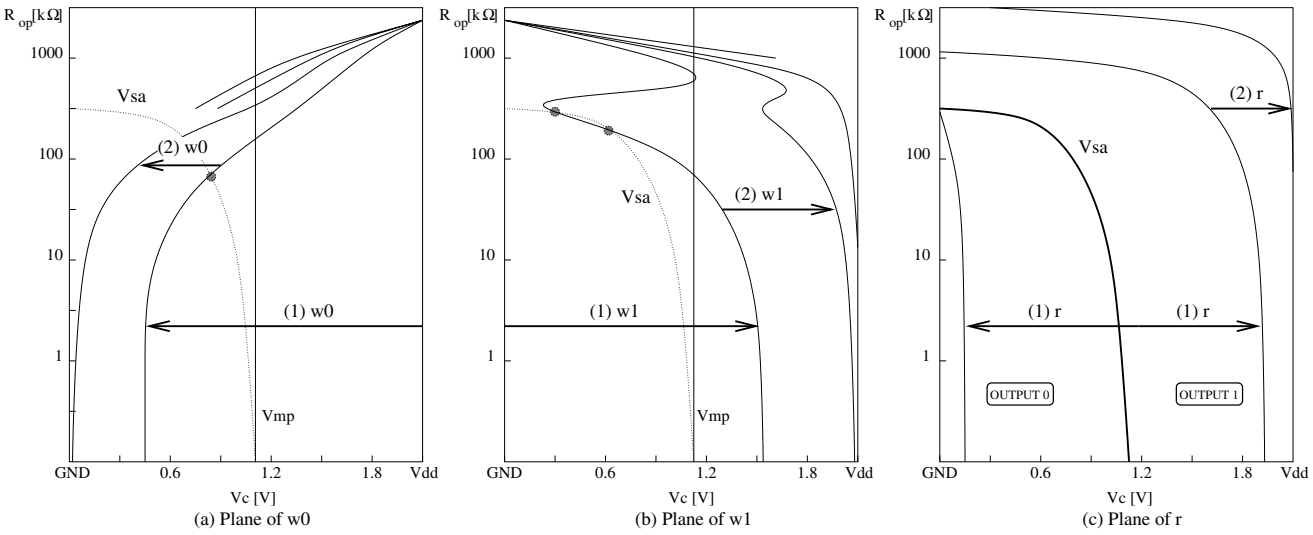


**Figure 6.** Result planes with $V_{dd}$ = 2.1 V, $t_{cyc}$ = 55 ns and T = +87° C, for the operations (a) $w0$, (b) $w1$, and (c) $r$.

2.4 V and 2.7 V. In the simulation, $V_{ini}$ = 1.1 V, which is slightly below $V_{sa}$, $R_{op}$ = 200 kΩ and T = +27° C. The figure shows that after about $t$ = 13 ns, $V_c$ is discharged for $V_{dd}$ = 2.4 V and 2.7 V, which means that the sense amplifier detects a 0 with these voltages. On the other hand, $V_c$ is charged up for $V_{dd}$ = 2.1 V, which means that the sense amplifier detects a 1. This indicates that increasing the supply voltage increases the range of $V_c$ values that result in detecting a 0. As a result, increasing $V_{dd}$ is considered as a less stressful condition for the $r$ operation.

In conclusion, increasing $V_{dd}$ is more stressful for the $1w0$ and less stressful for the $r$. This provides no information on the way $V_{dd}$ stresses the test. Therefore, the BR should be identified by performing a number of simulations to construct the $(1)w0$ curve and the $V_{sa}$ curve with $V_{dd}$ = 2.7 V and 2.1 V. This has been performed and the results indicate that the BR is 170 kΩ for $V_{dd}$ = 2.1 V, 200 kΩ for $V_{dd}$ = 2.4 V and 220 kΩ for $V_{dd}$ = 2.7 V. This means that $V_{dd}$ = 2.1 V is the most effective voltage since it gives the lowest BR.

### 4.4 SC evaluation

After identifying most stressful values of each ST, it is important to apply the resulting SC and construct the fault analysis planes of $w0$, $w1$ and $r$ again to see whether new detection conditions are needed to detect the faulty behavior. Figure 6 shows these result planes using the SC: $V_{dd}$ = 2.1 V, $t_{cyc}$ = 55 ns, and T = +87° C.

The figure shows a number of interesting changes in the behavior as compared to Figure 2, as listed below:

1. The BR represented by the intersection point of the $(1)w0$ curve and the $V_{sa}$ curve is reduced to about 50 kΩ (see the dot in Figure 6(a)).

2. With the used SC, a new detection condition should be used that includes more $w1$ operations to charge the cell to a high enough voltage. The detection condition is $\Updownarrow(..., w1, w1, w1, w0, r0, ...)$.

3. The applied SC induces a fail in the $0w1$ operation for the $R_{op}$ range 150 kΩ to 200 kΩ (see the two dots in Figure 6(b)). But this $R_{op}$ value does not represent a BR since $1w0$ fails at a lower $R_{op}$.

4. The used SC is very stressful since (even with $R_{op}$ = 0 Ω) a $w0$ operation cannot discharge $V_c$ from $V_{dd}$ to GND, and $w1$ cannot charge $V_c$ up from GND to $V_{dd}$.

## 5 Analysis results

The optimization method outlined in Section 4 has been applied to optimize tests to detect the faulty behavior of a number of DRAM cell defects. This section presents the simulation methodology first, then the analysis results are discussed.

### 5.1 Simulation methodology

The used electrical simulation model is a simplified design-validation model of a real DRAM. The simplified model includes one folded cell array column (2×2 memory cells, 2 reference cells, precharge devices and a sense amplifier), one write driver and one data output buffer. The used simulation tool is the electrical Spice-based simulator Titan, which is a proprietary simulator developed by Siemens/Infineon.

Figure 7 shows the 7 analyzed defects: 3 opens, 2 shorts and 2 bridges. Opens are added resistive components on

signal lines within memory cells. Shorts are resistive connections to $V_{dd}$ or GND. Bridges are resistive connections between nodes within the memory cell.

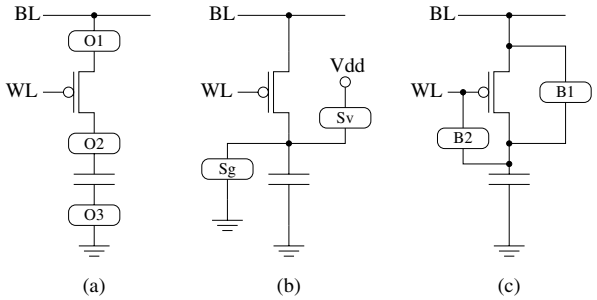


**Figure 7.** Simulated cell defects: (a) opens, (b) shorts and (c) bridges.

## 5.2 Simulation results

Table 1 summarizes the simulation results. The first column lists the analyzed defects as shown in Figure 7. Defects described by "true" are simulated on the true bit line, while defects described by "comp." are simulated on the complementary bit line. The column "Nom. border $R$" gives the value of the border $R$ at a nominal SC. The columns with the STs give the direction in which these STs should be modified in order to stress the memory test. The table also lists the stressed value of the border $R$ and the corresponding detection condition.

**Table 1.** ST optimization results for defects shown in Figure 7.

| Defect | Nom. border $R$ | $V_{dd}$ | $t_{cyc}$ | T | Str. border $R$ | Str. detection condition |
|---|---|---|---|---|---|---|
| O1–3 (true) | $R \geq 200$ kΩ | ↓ | ↓ | ↑ | $R \geq 50$ kΩ | $\Updownarrow(\ldots, w1, w1, w1, w0, r0, \ldots)$ |
| O1–3 (comp.) | $R \geq 200$ kΩ | ↓ | ↓ | ↑ | $R \geq 50$ kΩ | $\Updownarrow(\ldots, w0, w0, w0, w1, r1, \ldots)$ |
| Sg (true) | $R \leq 1$ MΩ | ↑ | ↓ | ↑ | $R \leq 10$ GΩ | $\Updownarrow(\ldots, w1, r1, \ldots)$ |
| Sg (comp.) | $R \leq 1$ MΩ | ↑ | ↓ | ↑ | $R \leq 10$ GΩ | $\Updownarrow(\ldots, w0, r0, \ldots)$ |
| Sv (true) | $R \leq 400$ kΩ | ↓ | ↓ | ↑ | $R \leq 1$ GΩ | $\Updownarrow(\ldots, w0, r0, \ldots)$ |
| Sv (comp.) | $R \leq 400$ kΩ | ↓ | ↓ | ↑ | $R \leq 1$ GΩ | $\Updownarrow(\ldots, w1, r1, \ldots)$ |
| B1 (true) | $R \leq 200$ kΩ | ↓ | ↓ | ↑ | $R \leq 100$ kΩ | $\Updownarrow(\ldots, w0, r0, \ldots)$ |
| B1 (comp.) | $R \leq 200$ kΩ | ↓ | ↓ | ↑ | $R \leq 100$ kΩ | $\Updownarrow(\ldots, w1, r1, \ldots)$ |
| B2 (true) | $R \leq 200$ kΩ | ↑ | ↓ | ↑ | $R \leq 100$ kΩ | $\Updownarrow(\ldots, w0, r0, \ldots)$ |
| B2 (comp.) | $R \leq 200$ kΩ | ↑ | ↓ | ↑ | $R \leq 100$ kΩ | $\Updownarrow(\ldots, w1, r1, \ldots)$ |

Note that the border $R$ value as well as the direction of ST optimization are the same for true and comp. defects in the table. In addition, the detection conditions for the comp. entries have the same structure as their true counterparts, but with 1s and 0s interchanged. This is due to the fact that the physical voltages stored within the cell are the same for the true and complementary defects.

The table shows that the applied SCs are very effective in increasing the range of the failing $R$. In terms of testing, this means that the applied SCs increase the coverage of a given test. For example, the BR of cell opens (O1–3) have been reduced from 200 kΩ to 50 kΩ.

For all analyzed defects, reducing the clock cycle time has proven to be more stressful than relaxing the clock. This can be explained by noting that reducing $t_{cyc}$ reduces the time the memory has to charge or discharge the cell, which affects the write operation and not the read operation. Since the more stressful situation occurs when we limit the ability of a write to influence $V_c$, it follows directly that reducing $t_{cyc}$ is the more stressful condition.

For all analyzed defects, increasing the temperature has proven to be more stressful than reducing the temperature. This can be attributed to the fact that all simulated defects are modeled using regular ohmic resistances, the value of which does not change in the simulation. Modeling the defects to increase their $R$ with decreasing T (which is the case with silicon based defects) may result in a different stress value for T.

# 6 Conclusions

This paper presented a new approach to optimize the stresses for tests of cell defects, using defect injection and electrical Spice simulation of a memory model. The approach provides more insight into the effectiveness of different stresses than traditional optimization methods since it internally studies the impact of each stress for the targeted defect. The paper also presented the results of a study performed to verify the newly proposed approach. The results show that the stresses are very effective in bringing defective devices closer to failure, and in increasing the fault coverage of memory tests.

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