NBTI Monitoring and Design for Reliability in Nanoscale Circuits

Seyab Khan Nor Zaidi Haron Said Hamdioui *Francky Catthoor
Computer Engineering Laboratory, Delft University of Technology,
Mekelweg 4, 2628 CD, Delft, The Netherlands
*IMEC Kapeldreef 75, 3001 Heverlee, Belgium
{M.S.K.Seyab, N.Z.B.Haron S.Hamdioui}@tudelft.nl, *francky.catthoor@imec.be

***Abstract*—Negative Bias Temperature Instability (NBTI) has become one of the major threats to circuit reliability in nanoscale-era. This paper presents a novel technique to monitor and tolerate NBTI in nanoscale circuits. First, it models NBTI impact on the gate output transition time; the simulation results show that NBTI can cause up to 8.56$\%$ increment to the transition time. Second, it presents a scheme to monitor the NBTI impact; the scheme is based on measuring transition time of the gate output. The proposed scheme converts the transition time increment into a voltage with a sensitivity of 0.50$\mathrm{mV/ps}$; the simulation results show that the transition time increment can cause up to 80mV increment in the monitoring circuit output voltage. Third, it proposes a design for reliability technique to mitigate NBTI impact by applying a positive body bias to the PMOS transistors; simulations carried out on a 33-stage ring oscillator reveal that the technique reduces NBTI impact by 34$\%$ in 10 years operational life. To show its effectiveness, leakage overhead of the proposed technique is also analyzed.**

Keywords-Negative Bias Temperature Instability; Transition Time Increment; Self Adjusting Threshold Voltage; Body Biasing; Leakage Current

I. Introduction

International Technology Roadmap for Semiconductors (ITRS) predicts 10-100 failures per million for sub-100nm process technology nodes in 10^9 hours operation [1]. Industrial data reveal that Negative Bias Temperature Instability (NBTI) is one of the major threats to contain failures in these limits [2,3]. NBTI degrades the performance of a PMOS transistor under a negative gate stress. The effects of NBTI on a PMOS transistor include: (a) threshold voltage increment, (b) drain current reduction, and (c) delay increment [4,5]. These effects appear at the circuit level and degrade the timing parameters; in extreme cases, they cause circuit timing/functional failures.

In recent years, there is an escalation of interest in two aspects of NBTI: (a) modeling and monitoring, and (b) tolerance and design for reliability. NBTI modeling and monitoring has been done both at the transistor [4,6,7] as well as at the circuit [5,8,10] levels. The proposed NBTI monitoring schemes so far can be classified in two categories.

- **Transistor parameter monitoring**: This technique is based on monitoring the selected transistors to measure NBTI impact on the circuit. For instance, Denias et al. [11] monitored the transistor drain current, threshold voltage, and transconductance to quantify the impact. Kang et al. [12] monitored the transistor leakage current to characterize NBTI.
- **Circuit parameter monitoring:** This technique is based on monitoring the circuit parameters to measure NBTI impact. For instance, Kim et al. [14] monitored the beat frequency of two ring oscillators (which is a special structure used on the chip), one stressed and the other unstressed, to characterize the impact. Keane et al. [16] characterized NBTI in terms of the control voltage of the two delay locked loops.

Although all the above proposed schemes measure NBTI impact, they require significant area overhead and/or possess lower accuracy. For example, transistor parameters monitoring [11–13] for a larger group of PMOS transistors that degrade at different rates require enormous area overhead [10]. Similarly, the circuit parameters monitoring schemes [14,16] lack accuracy in measuring NBTI impact because the monitoring results include the effects of all the degradation mechanisms. In this case, the NBTI impact on the PMOS transistors is not isolated. *Therefore, a scheme that implies lower area overhead and isolates NBTI impact on the circuit is required, this is one of the topics addressed in this paper.*

Apart from NBTI monitoring, researchers have focused on NBTI tolerance and design for reliability techniques. Wang et al. in [10] and Kang et al. in [9] suggested oversizing the PMOS transistors that cause up to 14.27$\%$ and 17.40$\%$ area overheads, respectively. Additionally, it causes the PMOS and NMOS transistors mismatching which are not tolerable in memory and analog circuits. Z. Qi et al. [19] proposed applying body biasing voltage for NBTI tolerance; the authors proposed an overly-conservative approach for applying the biasing voltage and proposed 50$\%$ change in the biasing voltage for 5$\%$ reduction in drain saturation current. Additionally, the paper does not quantify the leakage current overhead of the proposed 50$\%$ body biasing voltage variation. These two techniques have higher area overhead and *cannot* be changed dynamically to mitigate the

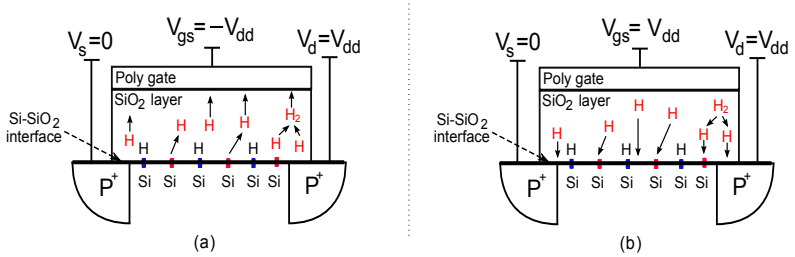

Fig. 1. Schematic view of (a) Si-H bond breaking, H and H_2 diffusions toward poly gate and their interconversion at Si/Si0_2 interface and inside oxide dielectric under negative gate stress (b) H and H_2 diffusions toward the Si-SiO_2 interface and ≡Si- bond recovery under positive gate stress

dynamically changing NBTI impact. *Therefore, there is a need to dynamically adjust the biasing voltage that follows NBTI impact on the circuit and quantify its impact on the leakage current of the circuit.*

This paper addresses the two shortcomings in NBTI research mentioned above: (a) it presents an efficient monitoring scheme that only measure the NBTI impact on PMOS transistors in the circuit, and. (b) it presents a design for reliability technique to minimize NBTI impact by dynamically adjusting the body biasing voltage. The monitoring scheme measures NBTI induced delay increment in the circuit with a sensitivity of 0.50mV/ps, and the design for reliability technique ensures reliable circuit operation for 10 years at the cost of only 4.09% leakage current increment. The rest of the paper is organized as follows. Section II briefly overviews NBTI mechanism. Section III proposes an analytical model for NBTI impact on the gate output transition time, which will be used to develop a monitoring scheme. Section IV introduces an NBTI monitoring scheme based on the gate output transition time, together with its design implementation. Section V presents a design-for-reliability technique - based on transistor body biasing - to minimize the impact of NBTI and extends the circuit lifetime; the technique generates a suitable biasing voltage to redress NBTI impact. Section VI provides the simulation results and analyzes the leakage current overhead of the proposed techniques. Finally, Section VII concludes the paper.

II. NBTI Mechanism

NBTI is characterized by the threshold voltage increment of the PMOS transistor under negative gate stress. NBTI originates from Silicon Hydrogen bonds (≡Si-H) breaking that occur at Silicon-Silicon dioxide (Si-SiO_2) interface as shown in Fig. 1(a). The broken Silicon bonds (≡Si-) act as interface traps at the Si-SiO_2 interface and the H atoms/molecules diffuse toward the poly gate. The *number of interface traps (N_{IT})* depends on ≡Si-H bond breaking rate (k_f) and ≡Si- bond recovery rate (k_r).

In recent times, exhaustive efforts has been put to understand NBTI [4,6,20]. Kackzer et al. in [20] have analyzed NBTI reasonably well but have not extended their analysis to deal with NBTI at a higher level. Alam et al. in [4] have modeled NBTI and presented the overall dynamics of NBTI as a reaction diffusion process. The model is usable at a higher level such as circuit level. Since in this work, NBTI analysis is done at the circuit level, model of [4] will be used that relates N_{IT} with time (t) as follows [4]:

$$N_{IT}(t) = \left(\frac{k_f N_o}{k_r}\right)^{2/3} \left(\frac{k_H}{k_{H_2}}\right)^{1/3} (6D_{H_2}t)^{1/6}, \tag{1}$$

where N_o, k_H, k_{H2}, and D_{H2} represent initial bond density, H to H_2 conversion rate, H_2 to H conversion rate, and H_2 diffusion rate inside SiO_2 layer, respectively. Interface traps are assumed to be positive charges remaining at the Si-SiO_2 interface that oppose the applied gate stress resulting in the threshold voltage increment (ΔV_{th}). The relation between N_{IT} and ΔV_{th} is [4]:

$$\Delta V_{th} = (1+m)qN_{IT}/C_{ox}, \tag{2}$$

where m, q, and C_{ox} are the holes mobility degradation that contribute to the V_{th} increment [5,23], electron charge, and oxide capacitance respectively. On the other hand, NBTI annealing takes place under the positive gate stress; in this case, the H atoms anneal back towards the Si-SiO_2 interface as shown in Fig. 1(b). The H atoms/molecules anneal the ≡Si- bonds at Si-SiO_2 interface resulting in lower N_{IT} and consequently lower ΔV_{th}.

III. Transition Time Increment Model

Sakuri et al. in [22] suggested that the gate output rise and fall transition times depend on the threshold voltages of the PMOS and NMOS transistors, respectively. Since NBTI affects PMOS transistor threshold voltage, only gate rise transition time has to be considered [8,23]. Using NBTI induced ΔV_{th} given in Eq. 2, the variation in gate rise transition time (T_{rise}) can be modeled as a function of NBTI.

On the other hand, Bellido et al. has argued in [24] that T_{rise} is a function of the load capacitance (C_L), PMOS and NMOS transistors aspect ratio (k) and PMOS transistor strength, i.e., drain saturation current (I_{dsat}). These dependencies are combined to get T_{rise} as:

$$T_{rise} = \frac{C_L k}{I_{dsat}}, \tag{3}$$

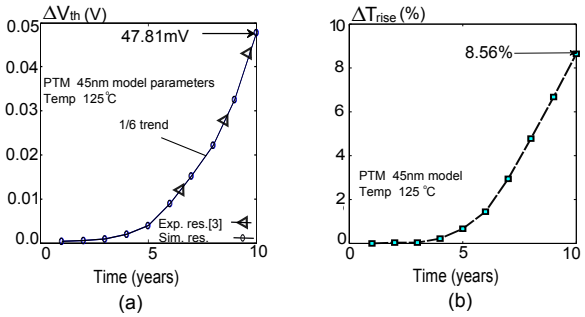

Fig. 2. (a) NBTI induced (ΔV_{th}) increment of a PMOS transistor as a function of time (b) Inverter output ΔT_{rise} increment as function of time

It is assumed that C_L and k remain fixed, therefore, T_{rise} only depends on I_{dsat}, which is given by [22]:

$$I_{dsat} = B(V_g - V_{th})^{\alpha}, \qquad B = \frac{\mu C_{ox} L_{eff}}{W_{eff}} \tag{4}$$

where V_g, α, μ, C_{ox}, L_{eff}, and W_{eff} represent gate potential, velocity saturation index, hole mobility in PMOS transistor channel, oxide capacitance, transistor effective length and width, respectively. By substituting Eq. 4 into Eq. 3, T_{rise} becomes:

$$T_{rise} = \frac{C_L k}{B(V_g - V_{th})^{\alpha}} \tag{5}$$

The impact of NBTI induced ΔV_{th} increment on T_{rise} is attained by differentiating Eq. 5 with respect to V_{th}. Thereafter, by expanding the result with Taylor series and neglecting the higher order terms, the increment in T_{rise} (ΔT_{rise}) is given by:

$$\Delta T_{rise} = C\frac{\Delta V_{th}}{(V_g - V_{th})^{\alpha}}, \qquad C = \frac{C_L k \alpha}{B}. \tag{6}$$

A simple CMOS inverter was synthesized using 45nm Predictive Technology Model (PTM) transistor models [21] and simulated using HSPICE for 10 years operation. To focus on NBTI, we assume that other failure mechanisms, e.g. Hot Carrier Degradation, Electromigrations and Time Dependent Dielectric Breakdown are not affecting the inverter. Throughout the simulation, NBTI parameters used to get ΔV_{th} are, $k_f = 8\times10^{-4}s^{-1}$, $k_r = 3\times10^{-18}cm^3s^{-1}$, $N_o = 5\times10^{16}cm^2$, $D_{H2} = 4\times10^{-21}cm^2s^{-1}$ and T = 125^{o}C [17]. Fig. 2 (a) gives the ΔV_{th} increment of PMOS transistor due to NBTI; it shows that ΔV_{th} approaches 47.81mV after 10 years of operation. The curve follows the $1/6$ trend and have a good match with the experimental results presented in [3]. Fig. 2(b) shows ΔT_{rise} increment of the inverter output that approaches 8.56% after 10 years operation. Paul et al. in [8] has suggested the same ΔT_{rise} increment trend due to NBTI for the other gates in the circuit.

The ΔT_{rise} increment follows a similar trend as NBTI induced ΔV_{th} increment. *Therefore, the ΔT_{rise} can be used as a metric to monitor NBTI in nanoscale circuits.*

IV. NBTI Monitoring

This section presents the concept of NBTI monitoring using the gate output transition time as the metric and proposes a scheme for implementing the concept. Several techniques have been proposed in the literature to monitor NBTI in the circuits [14,16]. However, their results contain the overall degradations and do not isolate NBTI impact. The technique proposed in this paper focuses on the rise transition of a gate output that is effected *only* by NBTI in the PMOS transistors.

A. NBTI Monitoring Concept

Fig. 3(a) shows the rising transition in output voltage (V_{gout}) of the last gate in a critical path. The figure shows that in the absence of NBTI ($NoNBTI$), V_{gout} starts the rising transition from 0V at time t_0 and approaches V_{dd} at time t_1.

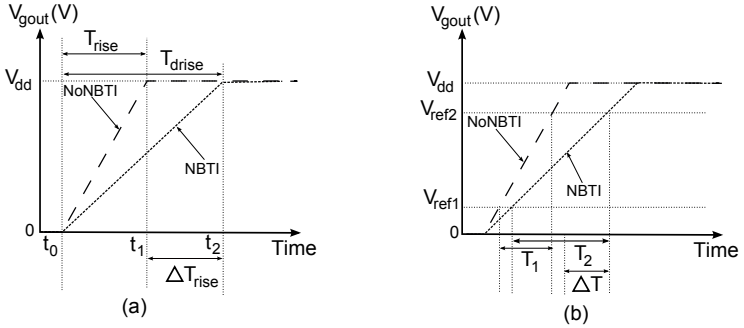

Fig. 3. (a) T_{rise} of a gate with NBTI and without NBTI (b) NBTI monitoring by comparing V_{gout} with reference voltages V_{ref1} and V_{ref2}

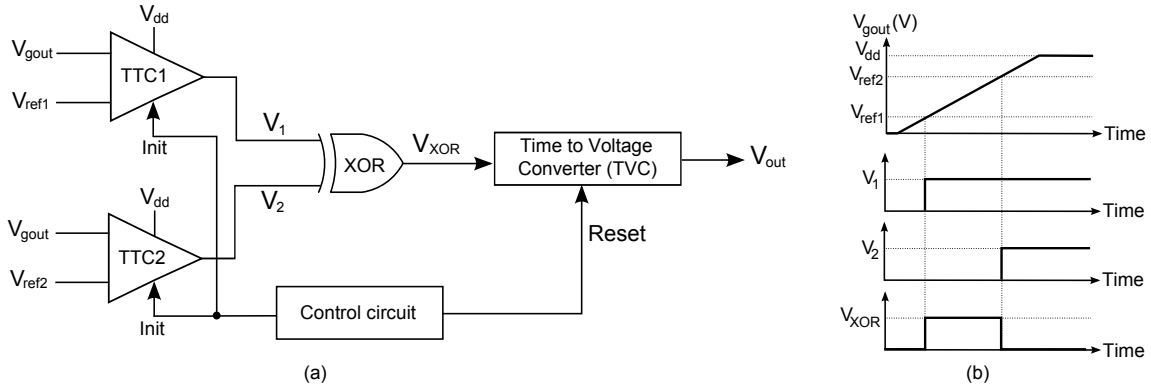

Fig. 4. (a) Block diagram of the proposed NBTI monitoring scheme that compares gate output with two reference voltages (b) Timing diagram of NBTI monitor

Let's now consider two reference voltages V_{ref1} and V_{ref2} as shown in Fig. 3(b). In the absence of NBTI, V_{gout} will require a transition time T_1 to proceed from V_{ref1} to V_{ref2}. However, in the presence of NBTI, V_{gout} will require a transition time T_2 to proceed from V_{ref1} to V_{ref2}. In this case, V_{gout} transition is delayed by ΔT; this ΔT is a representation of NBTI in the PMOS transistors as discussed in the previous section.

B. NBTI Monitoring Scheme

A block diagram of the scheme for implementing the concept proposed in the previous section is shown in Fig. 4(a). It consists of a Transition Time Comparator (TTC) pair (i.e. TTC1 and TTC2), a XOR gate, a Time-to-Voltage Converter (TVC) and a control circuit. The TTC pair compares the gate output transition (V_{gout}) with two reference voltages (i.e. V_{ref1} and V_{ref2}). TTC1 compares V_{gout} with V_{ref1} =10%×V_{dd}, and TTC2 compares V_{gout} with V_{ref2}=90%×V_{dd}. The output of TTC1 (V_1) goes high when V_{gout} exceeds V_{ref1} as shown in Fig. 4(b). Similarly, the output of TTC2 (V_2) goes high when V_{gout} crosses V_{ref2}. *For V_{gout} rise transition, V_1 should go high earlier than V_2*. Both V_1 and V_2 are inputs to a XOR gate. The active high duration of the XOR output (V_{XOR}) represents the interval between V_1 and V_2 low-to-high transitions as shown in Fig. 4(b). V_{XOR} is fed to the Time-to-Voltage Converter (TVC) that converts its high duration into a voltage. The amplitude of the TVC output V_{out} is proportional to the transition time of V_{gout} of the gate. The entire operation of the monitoring circuit is controlled by the control circuit. The control circuit sends a $Reset$ signal to the TVC block before the comparison. It is important to reset TVC before the comparison, so that V_{out} is not affected by the previous results. It also initates and terminates the comparison by setting and resetting $Init$ signal respectively.

In the rest of this section, the design structures and operating principles of the main blocks of Fig. 4 are described.

Transition Time Comparator (TTC)

The accuracy of the NBTI monitoring scheme depends on performance of the TTC pair. The schematic of a TTC that compares V_{gout} with V_{ref1}=10%×V_{dd} is shown in Fig. 5(a). The PMOS transistors M_5 and M_6 manifest the *decision making latch* for the comparison, while the NMOS transistors M_1 and M_2 are the decision *controlling elements*. The currents through M_1 and M_2 produce a differential current in the latch and switches it accordingly. The NMOS transistors M_3 and M_4 connect and isolate the latch from the controlling elements. The outputs of the latch (i.e., $Node_1$ and $Node_2$) are fed to the inputs of an *RS latch* that holds the decision till the next comparison. The comparison between V_{gout} and V_{ref1} is initiated and

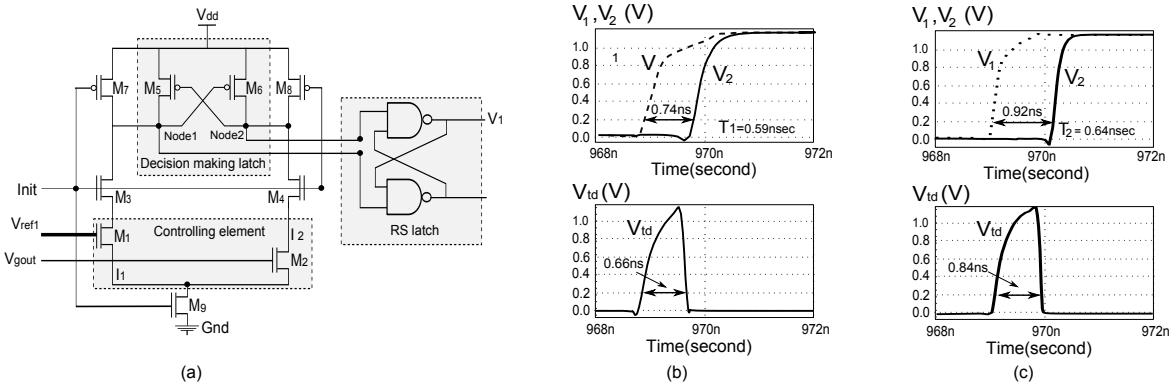

Fig. 5. (a) Schematic of transition time comparator (b) Low-to-high transitions of TTC1 and TTC2; Active high duration of XOR without and (c) with NBTI

terminated by $Init$ signal. The PMOS transistors M_7 and M_8 charge drain capacitances of M_3 and M_4 during low $Init$ signal that speed-up the next comparison.

To initiate the comparison, $Init$ signal gets high and connects the latch to the controlling elements. When V_{ref1} is larger than V_{gout}, the current flow through M_1 (I_1) surmounts the current through M_2 (I_2), causing M_5 to turn on while M_6 is turned off; this results in setting $Node_2$ to high. However, when V_{gout} exceeds V_{ref1} during the rise transition, I_2 becomes larger than I_1. Now the drain-source voltage of M_5 is large enough to switch M_6 on. The temporary on states of both M_5 and M_6 causes metastability in the latch. However, due to the current regeneration in the latch, the $Node_1$ voltage gets a stable high level and is fed to the RS latch that memorize the decision. The second TTC has been designed such that it produces high V_2 when V_{gout} exceeds 90% of V_{dd}. Both V_1 and V_2 are fed into the XOR gate inputs. The interval between V_1 and V_2 low-to-high transitions is obtained from the active high duration of the XOR output.

The functionality of the TTC1, TTC2 and XOR gate is verified through timing simulations using HSPICE. The 45nm PTM transistor models [21] are used to synthesize the comparators and XOR gate. A V_{gout} with T_{rise} of $0.7ns$ was applied to the TTC pair. The simulation results are shown in Fig. 5(b). In the absence of NBTI, V_{gout} takes T_1=$0.59ns$ to proceed from V_{ref1} to V_{ref2}. Under this condition, the interval between low-to-high transitions of V_1 and V_2 is $0.74ns$ (the extra time is due to the internal delays of the comparators) as shown in the top part of Fig. 5(b). The XOR gate converts this interval to a active high logical value with a duration of $0.66ns$ (see the bottom part of Fig. 5(b)). On the other hand, in the presence of NBTI, the transition time of V_{gout} to proceed from V_{ref1} to V_{ref2} increases up to T_2=$0.64ns$ as shown in top part of Fig. 5(c), about 9% higher. The increment extends the interval between low-to-high transitions of V_1 and V_2 that approaches $0.92ns$. Now the active high duration of XOR gate is $0.84ns$ as shown in the bottom part of Fig. 5(c), i.e., 27% more than the previous case.

C. Time-to-Voltage Converter (TVC)

The active high duration of XOR gate (i.e V_{XOR} in Fig. 4(a)) represent T_{rise}/T_{drise} of the gate. Time-to-Voltage Converter (TVC) converts this representation into a voltage. Fig. 6(a) shows an implementation of a simple charge pump based TVC that comprises two NMOS transistors N_1 and N_2, and a capacitor C_{int}. N_1 acts a control switch that controls voltage build across C_{int}. N_2 is used to discharge C_{int} before initiating NBTI measurement. C_{int} is main entity of the TVC that produces the TVC output voltage (i.e. V_{out}). V_{out} depends upon V_{XOR} high duration, C_{int} capacitance and time constant of N_1. W/L of N_1 are adjusted to get smaller time constant and C_{int} is kept such that the voltage developed is substantial yet not so high to saturate to the V_{dd}.

Before asserting $Init$ signal (see Fig. 6) to measure NBTI impact, V_{Reset} in the control circuit is set to high. The signal turns on the transistor N_2 and discharge C_{int} to the ground. V_{Reset} is kept high for a longer duration to ensure full discharge of C_{int}. Once the capacitor is fully discharged, $Init$ signal is set high and the output of the XOR gate (V_{XOR} in Fig. 4) is applied to N_1 that acts as a control switch. The high value of V_{XOR} will allow charge pumping from V_{dd} that builds a voltage across C_{int}. The amplitude of the voltage across C_{int} depends on V_{XOR} high duration.

The TVC is synthesized with 45nm NMOS transistor PTM models [21] with C_{int}=$0.62pF$. Fig. 6(b) shows that the amplitude of the TVC output (V_{out}) has almost a linear relationship with XOR output (V_{XOR}) high duration width. The figure suggests that 24% increment in V_{XOR} high duration causes 25% increment in the V_{out} voltage with a sensitivity of 0.50mV/psec.

At this point it can be observed that NBTI induced T_{rise} increment of the gate is represented by the increment in voltage, i.e. TVC output voltage V_{out}. The V_{out} can be used directly or indirectly to initiate an NBTI tolerating scheme. In this paper, the V_{XOR} is used to modify substrate (body) bias voltage of the PMOS transistors as will be discussed in the next section.

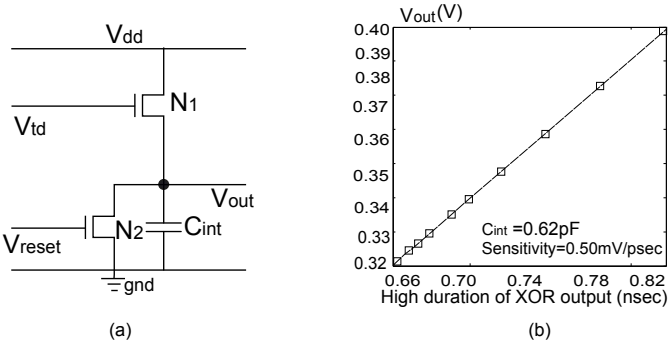

Fig. 6. (a) Schematics of TVC, (b) Output characteristics of TVC

D. Control Circuit

Control circuit decides the initiation and termination of the monitoring. There are many ways of implementing the circuitry to initiate monitoring, but optimally the circuit should periodically reset the TVC and then initiate the comparison and monitoring. Due to space constraints, the complete design and operating principle of the control circuit is omitted from the paper and only its signals used for the monitoring are discussed.

V. Proposed Design for Reliability Technique

This section proposes a technique to improve the reliability in the NBTI effected circuits. It starts by illustrating that dynamic body biasing is an effective technique for redressing NBTI induced V_{th} increment of PMOS transistors. Thereafter, it proposes a Self Adjusting Threshold Voltage (SATV) technique that applies body biasing to redress the NBTI impact.

A. Adaptive Body Biasing

Transistor can be body biased by applying a voltage between the source/drain and the substrate. The body bias affects V_{th} and therefore the speed and leakage current of the transistor. A negative body biasing increases V_{th} causing a slower and less leaky transistor. On the other hand, a positive body biasing decreases V_{th} resulting in faster and more leaky transistor [29]. Body bias can be applied in two difference ways: (a) all the transistors on a chip have the same bias voltage and (b) transistors are grouped in different groups and each particular group has the same bias voltage. Note that the second method ensures different but optimum V_{th} for all transistors on the chip.

Body biasing is an effective industrial technique to mitigate process variations of transistors within the same die or in different dies across the wafer. After fabrication, transistors in same/different dies may have different V_{th}. Applying body bias voltage to the transistors shifts the V_{th} of the transistors to an acceptable margin [28]. Similarly, body biasing the PMOS transistors can be used to redress NBTI induced V_{th} increment. As illustrated in section II, NBTI causes 47.81mV V_{th} increment to the PMOS transistors. For this reason, applying a positive bias to the PMOS is considered to redress the increment.

As NBTI in the PMOS transistors anneals during positive gate stress, it is desirable to have a dynamic bias voltage that redresses NBTI impact yet ensure minimum leakage currents in the circuit. Applying dynamic bias voltage is common in modern chips; e.g., Narendra et al. [27] proposed a dynamic biasing scheme that produced 24 different biasing voltages based on the results of monitoring circuits. Next, we propose a Self Adjusting Threshold Voltage (SATV) technique to adjust body bias voltage according to the output of the monitoring scheme.

B. Self Adjusting Threshold Voltage (SATV)

The main idea of SATV is to redress NBTI induced V_{th} increment. In presence of NBTI in the circuit, SATV lowers V_{th} by body biasing. However, in absence of NBTI, SATV applies no body biasing to the circuit. Fig 7(a) shows the proposed SATV scheme for a circuit consisting of an inverter that represents a gate in the circuit. The inverter output is monitored by the NBTI monitoring scheme proposed in the previous section. The monitoring circuit senses NBTI in the gate in terms of V_{out} increment. In absence of NBTI, V_{out}=0.32V and it increases with NBTI as shown in Fig. 6. The V_{out} is applied to SATV that produces the modified body bias voltage (V_{bb}) when V_{out}>0.32V. Fig. 7(b) shows that the modified V_{bb} has a linear relationship with V_{out}. The modified V_{bb} is applied to the substrate of the PMOS transistor that decreases its V_{th}.

The inverter shown in Fig. 7(a) was synthesized using 45nm transistor models [21] and simulated for an operation time of 10 years. NBTI monitoring circuit measures the NBTI impact and SATV produces the corresponding body bias voltage. To

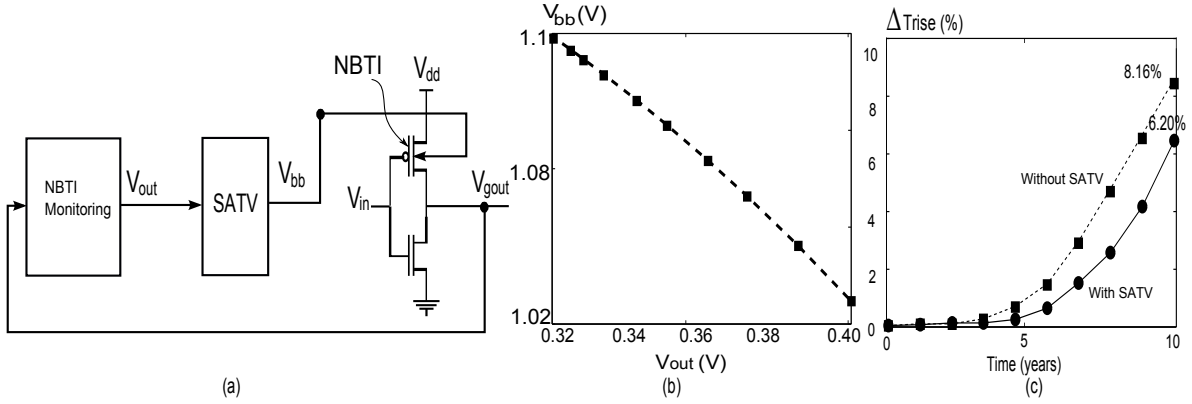

Fig. 7. (a) Schematic of the self adjusting threshold voltage scheme (b) The modified V_{bb} due to the TVC output (V_{out}) variation (c) T_{rise} increment due to NBTI with and without SATV

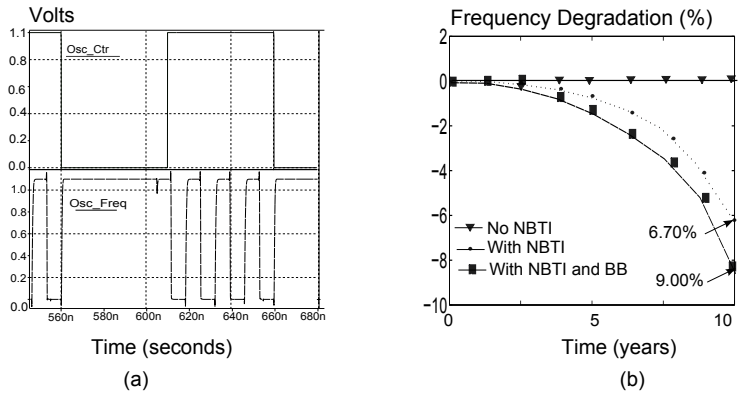

Fig. 8. (a) Samples of Osc_Ctr and Osc_Freq waveforms (b) Frequency degradation due to NBTI with and without body biasing

show effectiveness of the method, the NBTI indicator (i.e. rise transition time) T_{drise} is measured under two conditions: (a) no body bias was applied to the PMOS transistor, and (b) body bias was applied to PMOS transistor. Fig 7(c) shows T_{rise} increment due to NBTI under these two cases. The figure shows that when no body bias was applied, NBTI causes 8.16% increment to the rise transition time. However, when body biasing was applied, the increment in T_{rise} reduces to only 6.20%. Therefore, it can be deduced that the proposed technique reduces the NBTI impact by 31%.

VI. Experimental results and analysis

This section gives the simulation results of the proposed NBTI monitoring scheme and the design for reliability technique. As body bias may impact the leakage current of a transistor, the introduced design for reliability technique will be evaluated for leakage current overhead.

A. Simulation results

As a case study, a 33-stage ring oscillator is chosen as a test circuit to illustrate the effectiveness of the monitoring scheme and the design for reliability technique. The monitor circuit is attached to the last inverter of the oscillator. 45nm Predictive Technology Model (PTM) technology nodes are used to synthesize the circuit. The NBTI degradation is injected $only$ into the oscillator circuit by using a Verilog-A module [23]. The module injects degradation during negative gate stress and anneals the degradation during positive gate stress. The degradation follows $t^{1/6}$ time dependency presented in Eq. 1 and reported in [4]. The circuit is simulated for 10 years operation under three different cases:

- No NBTI: The impact of NBTI is not considered and hence no body biasing is applied.
- With NBTI: NBTI is considered and no body biasing is applied.
- With NBTI and BB: NBTI is considered and body biasing based on a design for reliability technique is applied.

Fig. 8(a) show the samples of the oscillation input control signal (Osc_Ctr) and the ring oscillator frequency output (Osc_Freq). The Osc_Ctr runs at 10MHz and the Osc_Freq oscillates at 70 MHz when Osc_Ctr signal is set high. Fig. 8(b) depicts the ring oscillator frequency degradation for the three considered cases. One can observe that in absence of NBTI (i.e. no NBTI case), the frequency remains the same for the entire simulation time. On the other hand, the case when NBTI affects the ring oscillator and body biasing is not applied, the frequency degrades with time. As expected from the analysis of our T_{rise} increment model of Section III, the oscillator frequency decreases by 9.00%. This degradation is in accordance to the observation presented in [14] and the experimental results reported [24]. Finally, when body biasing is applied to reduce the NBTI impact, the frequency degradation is only 6.70%; this means that the design for reliability technique is able to reduce NBTI impact by 34%. This improvement proves the effectiveness of the introduced design for reliability technique.

B. Leakage Current Overhead

As mentioned in the previous section, applying positive body biasing to a transistor increases its leakage current. Therefore, it is expected that our design for reliability technique will increase the leakage current of the PMOS transistors. On the other hand, in [15] Paul et al. has argued that NBTI causes exponential reduction in the leakage current. To verify the argument, a single stage of the ring oscillator is considered for the leakage current analysis. Fig. 9(a) shows leakage current reduction - in %- due to NBTI during 10 years operation. The figure shows that the reduction approaches 4.50% at the end of the operation time. This leakage reduction follows the trend presented in [15]. Therefore, the leakage current reduction caused by NBTI will automatically $compensate$ for the leakage current increment caused by body biasing. The question is now what the overall balance of the leakage is. To answer this question, we performed simulations in one of the oscillator stage for two cases (see Fig. 9(b)):

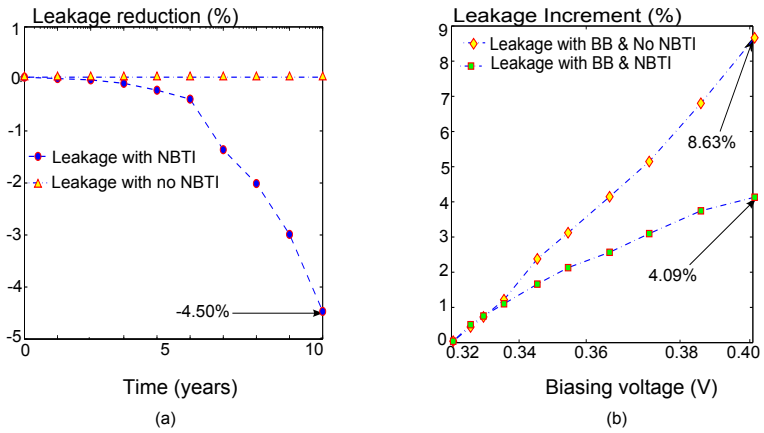

Fig. 9. (a) Leakage current reduction in absence and presence of NBTI (b) Leakage current increment due to body biasing in presence and presence of NBTI

- Leakage with BB and no NBTI: when body biasing is applied in absence of NBTI, the leakage current increment approaches 8.63%.
- Leakage with BB and NBTI: when NBTI is considered and body bias is applied to the PMOS transistor, the leakage current increment becomes only 4.09%.

Fig. 9 shows that the NBTI induced leakage reduction compensates 52.60% of the leakage current increment due to body biasing. As a consequence, the overall leakage increment due to the proposed design for reliability is not more than 4.09%.

VII. Conclusion

This paper has presented a scheme to monitor NBTI impact in nanoscale circuits and proposed a design technique for the circuit reliability improvement. Firstly, the impact of NBTI on gate output transition time is modeled. The analysis of the model showed that NBTI causes up to 8.56% increment in the gate output transition time. Secondly, a technique to monitor the NBTI impact is proposed; the technique is based on the measurement of the gate output transition time delay. The proposed technique converts the transition time increment into a voltage with a sensitivity of $0.50\mathrm{mV/ps}$. Thirdly, an NBTI mitigating technique that applies a dynamic biasing voltage to redress NBTI in the circuit is proposed. The technique ensures 34% reduction in NBTI impact on the circuit in 10 years operational life. Finally, it has been shown that the leakage current overhead of the proposed technique does not exceed 4.09% for an operational life of 10 years.

References

[1] ITRS "International Technology Road map for Semiconductors", *http://www.itrs.net/.*

[2] N. Kizmuka, et al., "The Impact of BTI for Direct Tunneling Ultra Thin Gate Oxide of MOSFET Scaling", *VLSI Technology, Digest of Technical Papers*, pp: 73-74, 1999.

[3] W. Abadeer, et al., "Behaviour of NBTI Under AC Dynamic Circuit Conditions", *Proc. of Intl. Physics Reliability Symp.(IPRS)*, pp: 17-22, 2003.

[4] M.A. Alam, et al., "A Comprehensive Model of PMOS NBTI Degradation", *Microelectronics Reliability* , Vol:45, Issue:1, pp: 71-81, 2005.

[5] A.T. Krishnan, et al., "NBTI impact on transistor and circuit: Models, mechanisms and scaling effects", *Proc. of Intl. Electronics Device Meeting (IEDM)*, pp: 14.5.1-14.5.4, 2003.

[6] S. Zafar, et al., "A comparative Study of NBTI and PBTI in SiO2/HfO2 Stacks with FUSI, TiN, gates", *Proc. of VLSI Technology Symposium (VTS)*, pp: 23-55, 2006.

[7] T. Grassor, et al., "TCAD Modeling of NBTI", *Pro. Int. Conf. on Simulation of Semiconductor Processes and Devices (SISPAD*, pp: 330-333, 2006.

[8] B.C. Paul, et al., "Impact of NBTI on the Temporal Performance Degradation of Digital Circuits", *IEEE Electron Device Letter*, Vol. 26, pp: 560-562, Aug. 2005.

[9] K. Kang, et al., "Efficient Transistor-Level Sizing Technique under Temporal Performance Degradation due to NBTI", *IEEE Intl. Conference on Computer Design (ICCD)*, pp: 216- 221, 2006.

[10] W. Wang, et al., "An Efficient Method to Identify Critical Gates under Circuit Aging", *Proc. of Design and Automation Conference (DAC)*, pp. 735-740, 2007.

[11] M. Denias, et al., "On-the-fly Characterization of NBTI in Ultra-thin Gate Oxide PMOSFET", *Proc. of Intl. Electronics Device Meeting(IEDM)*, pp: 109-112, 2004.

[12] K. Kang, et al., "Estimation of NBTI Degradation using IDDQ Measurement", *Proc. of Intl. Physics Reliability Symp.(IPRS)*, pp: 10-16, 2007.

[13] M Omana, et al., "Self-Checking Monitor for NBTI due Degradation", *Proc. of Intl. Mixed-Signals, Sensors, and Systems Test Workshop*, pp: 1-6 June 2010.

[14] T. Kim, et al., "Silicon Odometer: An on chip Reliability Monitor Frequency Degradation of Digital Circuits", *IEEE Jour. of Solid State Circ.*, pp: 874-880, April 2008.

[15] B.C. Paul, et al., "Temporal Performance Degradation under NBTI: Estimation and Design for Improved Reliability of Nanoscale Circuit", *Proc. of Design and Test in Europe (DATE)*, pp: 780-785, 2006.

[16] J. Keane, et al., "An on-chip NBTI Sensor for Measuring PMOS Threshold Voltage Degradation", *Proc. of Intl. Symp. on Low power Elect. Design*, pp: 189-193, 2007.

[17] H. Kufluoglu, "A Generalized Reaction Diffusion Model With Explicit HH2 Dynamics for Negative-Bias Temperature-Instability (NBTI) Degradation", *IEEE Transaction on Electron Devices*, pp: 1101-1106, April 2007.

[18] V. Reddy, et al., "Impact of Negative Bias Temperature Instability on Digital Circuit Reliability", *Proc. of Intl. Physics Reliability Symp.(IPRS)*, pp: 248-254, 2002.
[19] Z. Qi, et al., "NBTI Resilient Circuits Using Adaptive Body Biasing", *Proc. of Great Lakes symposium on VLSI (GLVLSI)*, pp: 285-290, 2008.
[20] B. Kackzar, et al., "Disorder-Controlled-Kinetics Model NBTI and its Experimental Verification", *Proc. of Intl. Physics Reliability Symp.(IPRS)*, pp: 381-387, 2005.
[21] Predictive Technology Model "http://ptm.asu.edu/",
[22] T. Sakurai, et al., "Alpha-Power law MOSFET Model and its Applications to CMOS Delay and other Formulas", *IEEE J. Solid-State Circuits*, pp: 584 - 594, Feb, 1990",
[23] S. Khan, et al., " NBTI Aware Nanoscale Circuit Delay Modeling and Mitigation", *Proc. of Intl. on-line Testing Symp. (IOLTS)*, pp: 3-8, 2011",
[24] M.J. Bellido, et al., "Logic Timing Simulation and the Degradation Delay Model ", *Imperial College Press*, 2006.
[25] T. Kobayashi, et al., "Self-adjusting Threshold Voltage scheme for Low Voltage High", *Proc. of Custom Integrated Circuits Conference (CICC)*, pp: 271-274, 1994.
[26] K. Stawiasz, et al., "On-Chip Circuit for Monitoring Frequency Degradation Due to NBTI", *Proc. of Intl. Reliability Physics Symp. (IPRS)*, pp: 532-535, 2008.
[27] S. Narendrar, et al., "1.1V 1GHz Communication Router with on-chip Body Bias in 150nm CMOS", *Proc. of Intl. Solid State Conference*, pp: 270-274, 2002.
[28] J.W. Chanz, et al., "Adaptive Body Bias for Reducing Impacts of Die-to-Die and Within-Die Parameter Variations on Microprocessor Frequency and Leakage", *IEEE Journal of Solid State Circuits*, pp: 1396-1402, Nov 2002.
[29] S.G. Narendra, et al., "Leakage in Nanometer CMOS Technologies", *Springer US*, 2006.
[30] T. Kuroda, et al., "A 0.9V 150MHz 10mW 4mm2 2-0 Discrete Cosine Transform Core Processor with Variable-Threshold-Voltage Scheme", *IEEE Inter. Solid-State Circuits Conf. (ISSCC)*, 1996.