NBToI Monitoring and Design for Reliability in Nanoscale Circuits

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Abstract—Negative Bias Temperature Instability (NBToI) has become one of the major threats to circuit reliability in nanoscale-era. This paper presents a novel technique to monitor and tolerate NBToI in nanoscale circuits. First, it models NBToI impact on the gate output transition time; the simulation results show that NBToI can cause up to 8.56% increment to the transition time. Second, it presents a scheme to monitor the NBToI impact; the scheme is based on measuring transition time of the gate output. The proposed scheme converts the transition time increment into a voltage with a sensitivity of 0.50 mV/ps; the simulation results show that the transition time increment can cause up to 80mV increment in the monitoring circuit output voltage. Third, it proposes a design for reliability technique to mitigate NBToI impact by applying a positive body bias to the PMOS transistors; simulations carried out on a 33-stage ring oscillator reveal that the technique reduces NBToI impact by 34% in 10 years operational life. To show its effectiveness, leakage overhead of the proposed technique is also analyzed.

Keywords—Negative Bias Temperature Instability; Transition Time Increment; Self Adjusting Threshold Voltage; Body Biasing; Leakage Current

I. INTRODUCTION

International Technology Roadmap for Semiconductors (ITRS) predicts 10-100 failures per million for sub-100nm process technology nodes in 10^9 hours operation [1]. Industrial data reveal that Negative Bias Temperature Instability (NBToI) is one of the major threats to contain failures in these limits [2,3]. NBToI degrades the performance of a PMOS transistor under a negative gate stress. The effects of NBToI on a PMOS transistor include: (a) threshold voltage increment, (b) drain current reduction, and (c) delay increment [4,5]. These effects appear at the circuit level and degrade the timing parameters; in extreme cases, they cause circuit timing/functional failures.

In recent years, there is an escalation of interest in two aspects of NBToI: (a) modeling and monitoring, and (b) tolerance and design for reliability. NBToI modeling and monitoring has been done both at the transistor [4,6,7] as well as at the circuit [5,8,10] levels. The proposed NBToI monitoring schemes so far can be classified in two categories.

- Transistor parameter monitoring: This technique is based on monitoring the selected transistors to measure NBToI impact on the circuit. For instance, Denias et al. [11] monitored the transistor drain current, threshold voltage, and transconductance to quantify the impact. Kang et al. [12] monitored the transistor leakage current to characterize NBToI.

- Circuit parameter monitoring: This technique is based on monitoring the circuit parameters to measure NBToI impact. For instance, Kim et al. [14] monitored the beat frequency of two ring oscillators (which is a special structure used on the chip), one stressed and the other unstressed, to characterize the impact. Keane et al. [16] characterized NBToI in terms of the control voltage of the two delay locked loops.

Although all the above proposed schemes measure NBToI impact, they require significant area overhead and/or possess lower accuracy. For example, transistor parameters monitoring [11–13] for a larger group of PMOS transistors that degrade at different rates require enormous area overhead [10]. Similarly, the circuit parameters monitoring schemes [14,16] lack accuracy in measuring NBToI impact because the monitoring results include the effects of all the degradation mechanisms. In this case, the NBToI impact on the PMOS transistors is not isolated. Therefore, a scheme that implies lower area overhead and isolates NBToI impact on the circuit is required. This is one of the topics addressed in this paper.

Apart from NBToI monitoring, researchers have focused on NBToI tolerance and design for reliability techniques. Wang et al. in [10] and Kang et al. in [9] suggested oversizing the PMOS transistors that cause up to 14.27% and 17.40% area overheads, respectively. Additionally, it causes the PMOS and NMOS transistors mismatching which are not tolerable in memory and analog circuits. Z. Qi et al. [19] proposed applying body biasing voltage for NBToI tolerance; the authors proposed an overly-conservative approach for applying the biasing voltage and proposed 50% change in the biasing voltage for 5% reduction in drain saturation current. Additionally, the paper does not quantify the leakage current overhead of the proposed 50% body biasing voltage variation. These two techniques have higher area overhead and cannot be changed dynamically to mitigate the
interface Si-SiO₂

where Nᵢₜ as circuit level. Since in this work, NBTI analysis is done at the circuit level, model of [4] will be used that relates Nᵢₜ and presented the overall dynamics of NBTI as a reaction diffusion process. The model is usable at a higher level such reasonably well but have not extended their analysis to deal with NBTI at a higher level. Alam et al. in [4] have modeled time (∆t) as follows [4]:

\[ N_{IT}(t) = \left( \frac{k_f N_{o}}{k_r} \right)^{2/3} \left( \frac{k_H}{k_{H2}} \right)^{1/3} (6D_{H2}t)^{1/6}, \]

where \( N_{o}, k_f, k_H, \) and \( D_{H2} \) represent initial bond density, H to H₂ conversion rate, H₂ to H conversion rate, and H₂ diffusion rate inside SiO₂ layer, respectively. Interface traps are assumed to be positive charges remaining at the Si-SiO₂ interface that oppose the applied gate stress resulting in the threshold voltage increment (\( \Delta V_{th} \)). The relation between \( N_{IT} \) and \( \Delta V_{th} \) is [4]:

\[ \Delta V_{th} = (1 + m)qN_{IT}/C_{ox}, \]

where \( m, q, \) and \( C_{ox} \) are the holes mobility degradation that contribute to the \( V_{th} \) increment [5,23], electron charge, and oxide capacitance respectively. On the other hand, NBTI annealing takes place under the positive gate stress; in this case, the H atoms anneal back towards the Si-SiO₂ interface as shown in Fig. 1(b). The H atoms/molecules anneal the ≡Si- bonds at Si-SiO₂ interface resulting in lower \( N_{IT} \) and consequently lower \( \Delta V_{th} \).

III. TRANSITION TIME INCREMENT MODEL

Sakuri et al. in [22] suggested that the gate output rise and fall transition times depend on the threshold voltages of the PMOS and NMOS transistors, respectively. Since NBTI affects PMOS transistor threshold voltage, only gate rise transition time has to be considered [8,23]. Using NBTI induced \( \Delta V_{th} \) given in Eq. 2, the variation in gate rise transition time (\( T_{rise} \)) can be modeled as a function of NBTI.

On the other hand, Bellido et al. has argued in [24] that \( T_{rise} \) is a function of the load capacitance (\( C_L \)), PMOS and NMOS transistors aspect ratio (k) and PMOS transistor strength, i.e., drain saturation current (\( I_{dsat} \)). These dependencies are combined to get \( T_{rise} \) as:

\[ T_{rise} = \frac{C_L k}{I_{dsat}} \]

This paper addresses the two shortcomings in NBTI research mentioned above: (a) it presents an efficient monitoring scheme that only measure the NBTI impact on PMOS transistors in the circuit, and. (b) it presents a design for reliability technique to minimize NBTI impact by dynamically adjusting the body biasing voltage. The monitoring scheme measures NBTI induced delay increment in the circuit with a sensitivity of 0.50mV/ps, and the design for reliability technique ensures reliable circuit operation for 10 years at the cost of only 4.09% leakage current increment. The rest of the paper is organized as follows. Section II briefly overviews NBTI mechanism. Section III proposes an analytical model for NBTI impact on the gate output transition time, which will be used to develop a monitoring scheme. Section IV introduces an NBTI monitoring scheme based on the gate output transition time, together with its design implementation. Section V presents a design-for-reliability technique - based on transistor body biasing - to minimize the impact of NBTI and extends the circuit lifetime; the technique generates a suitable biasing voltage to redress NBTI impact. Section VI provides the simulation results and analyzes the leakage current overhead of the proposed techniques. Finally, Section VII concludes the paper.

II. NBTI MECHANISM

NBTI is characterized by the threshold voltage increment of the PMOS transistor under negative gate stress. NBTI originates from Silicon Hydrogen bonds (≡Si-H) breaking that occur at Silicon-Silicon dioxide (Si-SiO₂) interface as shown in Fig. 1(a). The broken Silicon bonds (≡Si-) act as interface traps at the Si-SiO₂ interface and the H atoms/molecules diffuse toward the poly gate. The number of interface traps (\( N_{IT} \)) depends on ≡Si-H bond breaking rate (\( k_1 \)) and ≡Si- bond recovery rate (\( k_r \)).

In recent times, exhaustive efforts has been put to understand NBTI [4,6,20]. Kackzer et al. in [20] have analyzed NBTI reasonably well but have not extended their analysis to deal with NBTI at a higher level. Alam et al. in [4] have modeled NBTI and presented the overall dynamics of NBTI as a reaction diffusion process. The model is usable at a higher level such as circuit level. Since in this work, NBTI analysis is done at the circuit level, model of [4] will be used that relates Nᵢₜ with time (\( t \)) as follows [4]:

\[ N_{IT}(t) = \left( \frac{k_f N_{o}}{k_r} \right)^{2/3} \left( \frac{k_H}{k_{H2}} \right)^{1/3} (6D_{H2}t)^{1/6}, \]

where \( k_f \) and \( k_r \) are the holes mobility degradation that contribute to the Vₜh increment [5,23], electron charge, and oxide capacitance respectively. On the other hand, NBTI annealing takes place under the positive gate stress; in this case, the H atoms anneal back towards the Si-SiO₂ interface as shown in Fig. 1(b). The H atoms/molecules anneal the ≡Si- bonds at Si-SiO₂ interface resulting in lower Nᵢₜ and consequently lower ∆Vₜh.

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On the other hand, Bellido et al. has argued in [24] that \( T_{rise} \) is a function of the load capacitance (\( C_L \)), PMOS and NMOS transistors aspect ratio (k) and PMOS transistor strength, i.e., drain saturation current (\( I_{dsat} \)). These dependencies are combined to get \( T_{rise} \) as:

\[ T_{rise} = \frac{C_L k}{I_{dsat}} \]
It is assumed that $C_L$ and $k$ remain fixed, therefore, $T_{\text{rise}}$ only depends on $I_{\text{dsat}}$, which is given by [22]:

$$I_{\text{dsat}} = B(V_g - V_{\text{th}})^\alpha, \quad B = \frac{\mu C_{ox} L_{\text{eff}}}{W_{\text{eff}}}, \quad \alpha = \frac{1}{6}$$

where $V_g$, $\alpha$, $\mu$, $C_{ox}$, $L_{\text{eff}}$, and $W_{\text{eff}}$ represent gate potential, velocity saturation index, hole mobility in PMOS transistor channel, oxide capacitance, transistor effective length and width, respectively. By substituting Eq. 4 into Eq. 3, $T_{\text{rise}}$ becomes:

$$T_{\text{rise}} = \frac{C_L k}{B(V_g - V_{\text{th}})^\alpha}$$

The impact of NBTI induced $\Delta V_{\text{th}}$ increment on $T_{\text{rise}}$ is attained by differentiating Eq. 5 with respect to $V_{\text{th}}$. Thereafter, by expanding the result with Taylor series and neglecting the higher order terms, the increment in $T_{\text{rise}}$ ($\Delta T_{\text{rise}}$) is given by:

$$\Delta T_{\text{rise}} = C \frac{\Delta V_{\text{th}}}{(V_g - V_{\text{th}})^\alpha}, \quad C = \frac{C_L k \alpha}{B}.$$ 

A simple CMOS inverter was synthesized using 45nm Predictive Technology Model (PTM) transistor models [21] and simulated using HSPICE for 10 years operation. To focus on NBTI, we assume that other failure mechanisms, e.g. Hot Carrier Degradation, Electromigrations and Time Dependent Dielectric Breakdown are not affecting the inverter. Throughout the simulation, NBTI parameters used to get $\Delta V_{\text{th}}$, $k_f=8 \times 10^{-7}$s$^{-1}$, $k_r=3 \times 10^{-18}$cm$^3$s$^{-1}$, $N_o=5 \times 10^{16}$cm$^2$, $D_{eff}=4 \times 10^{-24}$cm$^2$s$^{-1}$ and $T = 125^\circ C$ [17]. Fig. 2 (a) gives the $\Delta V_{\text{th}}$ increment of PMOS transistor due to NBTI; it shows that $\Delta V_{\text{th}}$ approaches 47.81mV after 10 years of operation. The curve follows the 1/6 trend and have a good match with the experimental results presented in [3]. Fig. 2(b) shows $\Delta T_{\text{rise}}$ increment of the inverter output that approaches 8.56% after 10 years operation. Paul et al. in [8] has suggested the same $\Delta T_{\text{rise}}$ increment trend due to NBTI for the other gates in the circuit.

The $\Delta T_{\text{rise}}$ increment follows a similar trend as NBTI induced $\Delta V_{\text{th}}$ increment. Therefore, the $\Delta T_{\text{rise}}$ can be used as a metric to monitor NBTI in nanoscale circuits.

IV. NBTI MONITORING

This section presents the concept of NBTI monitoring using the gate output transition time as the metric and proposes a scheme for implementing the concept. Several techniques have been proposed in the literature to monitor NBTI in the circuits [14,16]. However, their results contain the overall degradations and do not isolate NBTI impact. The technique proposed in this paper focuses on the rise transition of a gate output that is effected only by NBTI in the PMOS transistors.

A. NBTI Monitoring Concept

Fig. 3(a) shows the rising transition in output voltage ($V_{\text{gout}}$) of the last gate in a critical path. The figure shows that in the absence of NBTI (NoNBTI), $V_{\text{gout}}$ starts the rising transition from 0V at time $t_0$ and approaches $V_{dd}$ at time $t_1$.

![Figure 3(a)](image)

Fig. 3. (a) $T_{\text{rise}}$ of a gate with NBTI and without NBTI (b) NBTI monitoring by comparing $V_{\text{gout}}$ with reference voltages $V_{\text{ref1}}$ and $V_{\text{ref2}}$
Let’s now consider two reference voltages $V_{\text{ref1}}$ and $V_{\text{ref2}}$ as shown in Fig. 3(b). In the absence of NBTI, $V_{\text{gout}}$ will require a transition time $T_1$ to proceed from $V_{\text{ref1}}$ to $V_{\text{ref2}}$. However, in the presence of NBTI, $V_{\text{gout}}$ will require a transition time $T_2$ to proceed from $V_{\text{ref1}}$ to $V_{\text{ref2}}$. In this case, $V_{\text{gout}}$ transition is delayed by $\Delta T$; this $\Delta T$ is a representation of NBTI in the PMOS transistors as discussed in the previous section.

### B. NBTI Monitoring Scheme

A block diagram of the scheme for implementing the concept proposed in the previous section is shown in Fig. 4(a). It consists of a Transition Time Comparator (TTC) pair (i.e. TTC1 and TTC2), a XOR gate, a Time-to-Voltage Converter (TVC) and a control circuit. The TTC pair compares the gate output transition ($V_{\text{gout}}$) with two reference voltages (i.e. $V_{\text{ref1}}$ and $V_{\text{ref2}}$). TTC1 compares $V_{\text{gout}}$ with $V_{\text{ref1}}=10\% \times V_{\text{dd}}$, and TTC2 compares $V_{\text{gout}}$ with $V_{\text{ref2}}=90\% \times V_{\text{dd}}$. The output of TTC1 ($V_1$) goes high when $V_{\text{gout}}$ exceeds $V_{\text{ref1}}$ as shown in Fig. 4(b). Similarly, the output of TTC2 ($V_2$) goes high when $V_{\text{gout}}$ crosses $V_{\text{ref2}}$. For $V_{\text{gout}}$ rise transition, $V_1$ should go high earlier than $V_2$. Both $V_1$ and $V_2$ are inputs to a XOR gate. The active high duration of the XOR output ($V_{\text{XOR}}$) represents the interval between $V_1$ and $V_2$ low-to-high transitions as shown in Fig. 4(b). $V_{\text{XOR}}$ is fed to the Time-to-Voltage Converter (TVC) that converts its high duration into a voltage. The amplitude of the TVC output $V_{\text{out}}$ is proportional to the transition time of $V_{\text{gout}}$ of the gate. The entire operation of the monitoring circuit is controlled by the control circuit. The control circuit sends a $\text{Reset}$ signal to the TVC block before the comparison. It is important to reset TVC before the comparison, so that $V_{\text{out}}$ is not affected by the previous results. It also initiates and terminates the comparison by setting and resetting $\text{Init}$ signal respectively.

In the rest of this section, the design structures and operating principles of the main blocks of Fig. 4 are described.

#### Transition Time Comparator (TTC)

The accuracy of the NBTI monitoring scheme depends on performance of the TTC pair. The schematic of a TTC that compares $V_{\text{gout}}$ with $V_{\text{ref1}}=10\% \times V_{\text{dd}}$ is shown in Fig. 5(a). The PMOS transistors $M_8$ and $M_9$ manifest the decision making latch for the comparison, while the NMOS transistors $M_1$ and $M_2$ are the decision controlling elements. The currents through $M_1$ and $M_2$ produce a differential current in the latch and switches it accordingly. The NMOS transistors $M_3$ and $M_4$ connect and isolate the latch from the controlling elements. The outputs of the latch (i.e., Node1 and Node2) are fed to the inputs of an $\text{RS latch}$ that holds the decision till the next comparison. The comparison between $V_{\text{gout}}$ and $V_{\text{ref1}}$ is initiated and
terminated by \textit{Init} signal. The PMOS transistors $M_7$ and $M_8$ charge drain capacitances of $M_3$ and $M_4$ during low \textit{Init} signal that speed-up the next comparison.

To initiate the comparison, \textit{Init} signal gets high and connects the latch to the controlling elements. When $V_{\text{ref1}}$ is larger than $V_{\text{gout}}$, the current flow through $M_1$ ($I_1$) surmounts the current through $M_2$ ($I_2$), causing $M_5$ to turn \textit{on} while $M_6$ is turned \textit{off}; this results in setting Node$_2$ to high. However, when $V_{\text{gout}}$ exceeds $V_{\text{ref1}}$ during the rise transition, $I_2$ becomes larger than $I_1$. Now the drain-source voltage of $M_5$ is large enough to switch $M_6$ \textit{on}. The temporary \textit{on} states of both $M_5$ and $M_6$ causes metastability in the latch. However, due to the current regeneration in the latch, the Node$_1$ voltage gets a stable high level and is fed to the RS latch that memorize the decision. The second TTC has been designed such that it produces high $V_2$ when $V_{\text{gout}}$ exceeds 90\% of $V_{\text{dd}}$. Both $V_1$ and $V_2$ are fed into the XOR gate inputs. The interval between $V_1$ and $V_2$ low-to-high transitions is obtained from the active high duration of the XOR output.

The functionality of the TTC1, TTC2 and XOR gate is verified through timing simulations using HSPICE. The 45nm PTM transistor models [21] are used to synthesize the comparators and XOR gate. A $V_{\text{gout}}$ with $T_{\text{rise}}$ of 0.7\textit{ns} was applied to the TTC pair. The simulation results are shown in Fig. 5(b). In the absence of NBTI, $V_{\text{gout}}$ takes $T_1=0.59\text{ns}$ to proceed from $V_{\text{ref1}}$ to $V_{\text{ref2}}$. Under this condition, the interval between low-to-high transitions of $V_1$ and $V_2$ is 0.74\textit{ns} (the extra time is due to the internal delays of the comparators) as shown in the top part of Fig. 5(b). The XOR gate converts this interval to a active high logical value with a duration of 0.66\textit{ns} (see the bottom part of Fig. 5(b)). On the other hand, in the presence of NBTI, the transition time of $V_{\text{gout}}$ to proceed from $V_{\text{ref1}}$ to $V_{\text{ref2}}$ increases up to $T_2=0.64\text{ns}$ as shown in top part of Fig. 5(c), about 9\% higher. The increment extends the interval between low-to-high transitions of $V_1$ and $V_2$ that approaches 0.92\textit{ns}. Now the active high duration of XOR gate is 0.84\textit{ns} as shown in the bottom part of Fig. 5(c), i.e., 27\% more than the previous case.

\section*{C. Time-to-Voltage Converter (TVC)}

The active high duration of XOR gate (i.e. $V_{\text{XOR}}$ in Fig. 4(a)) represent $T_{\text{rise}}/T_{\text{drise}}$ of the gate. Time-to-Voltage Converter (TVC) converts this representation into a voltage. Fig. 6(a) shows an implementation of a simple charge pump based TVC that comprises two NMOS transistors $N_1$ and $N_2$, and a capacitor $C_{\text{int}}$. $N_1$ acts a control switch that controls voltage build across $C_{\text{int}}$. $N_2$ is used to discharge $C_{\text{int}}$ before initiating NBTI measurement. $C_{\text{int}}$ is main entity of the TVC that produces the TVC output voltage (i.e. $V_{\text{out}}$). $V_{\text{out}}$ depends upon $V_{\text{XOR}}$ high duration, $C_{\text{int}}$ capacitance and time constant of $N_1$. W/L of $N_1$ are adjusted to get smaller time constant and $C_{\text{int}}$ is kept such that the voltage developed is substantial yet not so high to saturate to the $V_{\text{dd}}$.

Before asserting \textit{Init} signal (see Fig. 6) to measure NBTI impact, $V_{\text{Reset}}$ in the control circuit is set to high. The signal turns on the transistor $N_2$ and discharge $C_{\text{int}}$ to the ground. $V_{\text{Reset}}$ is kept high for a longer duration to ensure full discharge of $C_{\text{int}}$. Once the capacitor is fully discharged, \textit{Init} signal is set high and the output of the XOR gate ($V_{\text{XOR}}$ in Fig. 4) is applied to $N_1$ that acts as a control switch. The high value of $V_{\text{XOR}}$ will allow charge pumping from $V_{\text{dd}}$ that builds a voltage across $C_{\text{int}}$. The amplitude of the voltage across $C_{\text{int}}$ depends on $V_{\text{XOR}}$ high duration.

The TVC is synthesized with 45nm NMOS transistor PTM models [21] with $C_{\text{int}}=0.62\text{pF}$. Fig. 6(b) shows that the amplitude of the TVC output ($V_{\text{out}}$) has almost a linear relationship with XOR output ($V_{\text{XOR}}$) high duration width. The figure suggests that 24\% increment in $V_{\text{XOR}}$ high duration causes 25\% increment in the $V_{\text{out}}$ voltage with a sensitivity of 0.50mV/psec.

At this point it can be observed that NBTI induced $T_{\text{rise}}$ increment of the gate is represented by the increment in voltage, i.e. TVC output voltage $V_{\text{out}}$. The $V_{\text{out}}$ can be used directly or indirectly to initiate an NBTI tolerating scheme. In this paper, the $V_{\text{XOR}}$ is used to modify substrate (body) bias voltage of the PMOS transistors as will be discussed in the next section.

![Fig. 6. (a) Schematics of TVC, (b) Output characteristics of TVC](image-url)
D. Control Circuit

Control circuit decides the initiation and termination of the monitoring. There are many ways of implementing the circuitry to initiate monitoring, but optimally the circuit should periodically reset the TVC and then initiate the comparison and monitoring. Due to space constraints, the complete design and operating principle of the control circuit is omitted from the paper and only its signals used for the monitoring are discussed.

V. PROPOSED DESIGN FOR RELIABILITY TECHNIQUE

This section proposes a technique to improve the reliability in the NBTI effected circuits. It starts by illustrating that dynamic body biasing is an effective technique for redressing NBTI induced $V_{th}$ increment of PMOS transistors. Thereafter, it proposes a Self Adjusting Threshold Voltage (SATV) technique that applies body biasing to redress the NBTI impact.

A. Adaptive Body Biasing

Transistor can be body biased by applying a voltage between the source/drain and the substrate. The body bias affects $V_{th}$ and therefore the speed and leakage current of the transistor. A negative body biasing increases $V_{th}$ causing a slower and less leaky transistor. On the other hand, a positive body biasing decreases $V_{th}$ resulting in faster and more leaky transistor [29]. Body bias can be applied in two difference ways: (a) all the transistors on a chip have the same bias voltage and (b) transistors are grouped in different groups and each particular group has the same bias voltage. Note that the second method ensures different but optimum $V_{th}$ for all transistors on the chip.

Body biasing is an effective industrial technique to mitigate process variations of transistors within the same die or in different dies across the wafer. After fabrication, transistors in same/different dies may have different $V_{th}$. Applying body bias voltage to the transistors shifts the $V_{th}$ of the transistors to an acceptable margin [28]. Similarly, body biasing the PMOS transistors can be used to redress NBTI induced $V_{th}$ increment. As illustrated in section II, NBTI causes 47.81mV $V_{th}$ increment to the PMOS transistors. For this reason, applying a positive bias to the PMOS is considered to redress the increment.

As NBTI in the PMOS transistors anneals during positive gate stress, it is desirable to have a dynamic bias voltage that redresses NBTI impact yet ensure minimum leakage currents in the circuit. Applying dynamic bias voltage is common in modern chips; e.g., Narendra et al. [27] proposed a dynamic biasing scheme that produced 24 different biasing voltages based on the results of monitoring circuits. Next, we propose a Self Adjusting Threshold Voltage (SATV) technique to adjust body bias voltage according to the output of the monitoring scheme.

B. Self Adjusting Threshold Voltage (SATV)

The main idea of SATV is to redress NBTI induced $V_{th}$ increment. In presence of NBTI in the circuit, SATV lowers $V_{th}$ by body biasing. However, in absence of NBTI, SATV applies no body biasing to the circuit. Fig 7(a) shows the proposed SATV scheme for a circuit consisting of an inverter that represents a gate in the circuit. The inverter output is monitored by the NBTI monitoring scheme proposed in the previous section. The monitoring circuit senses NBTI in the gate in terms of $V_{out}$ increment. In absence of NBTI, $V_{out}$=0.32V and it increases with NBTI as shown in Fig. 6. The $V_{out}$ is applied to SATV that produces the modified body bias voltage ($V_{bb}$) when $V_{out}>0.32V$. Fig. 7(b) shows that the modified $V_{bb}$ has a linear relationship with $V_{out}$. The modified $V_{bb}$ is applied to the substrate of the PMOS transistor that decreases its $V_{th}$.

The inverter shown in Fig. 7(a) was synthesized using 45nm transistor models [21] and simulated for an operation time of 10 years. NBTI monitoring circuit measures the NBTI impact and SATV produces the corresponding body bias voltage. To

![Fig. 7. (a) Schematic of the self adjusting threshold voltage scheme (b) The modified $V_{bb}$ due to the TVC output ($V_{out}$) variation (c) $\Delta T_{rise}$ increment due to NBTI with and without SATV](image)
show effectiveness of the method, the NBTI indicator (i.e. rise transition time) $T_{\text{rise}}$ is measured under two conditions: (a) no body bias was applied to the PMOS transistor, and (b) body bias was applied to PMOS transistor. Fig 7(c) shows $T_{\text{rise}}$ increment due to NBTI under these two cases. The figure shows that when no body bias was applied, NBTI causes 8.16% increment to the rise transition time. However, when body biasing was applied, the increment in $T_{\text{rise}}$ reduces to only 6.20%. Therefore, it can be deduced that the proposed technique reduces the NBTI impact by 31%.

VI. EXPERIMENTAL RESULTS AND ANALYSIS

This section gives the simulation results of the proposed NBTI monitoring scheme and the design for reliability technique. As body bias may impact the leakage current of a transistor, the introduced design for reliability technique will be evaluated for leakage current overhead.

A. Simulation results

As a case study, a 33-stage ring oscillator is chosen as a test circuit to illustrate the effectiveness of the monitoring scheme and the design for reliability technique. The monitor circuit is attached to the last inverter of the oscillator. 45nm Predictive Technology Model (PTM) technology nodes are used to synthesize the circuit. The NBTI degradation is injected only into the oscillator circuit by using a Verilog-A module [23]. The module injects degradation during negative gate stress and anneals the degradation during positive gate stress. The degradation follows $t^{-1/6}$ time dependency presented in Eq. 1 and reported in [4]. The circuit is simulated for 10 years operation under three different cases:

- No NBTI: The impact of NBTI is not considered and hence no body biasing is applied.
- With NBTI: NBTI is considered and no body biasing is applied.
- With NBTI and BB: NBTI is considered and body biasing based on a design for reliability technique is applied.

Fig. 8(a) show the samples of the oscillation input control signal ($Osc_{\text{Ctr}}$) and the ring oscillator frequency output ($Osc_{\text{Freq}}$). The $Osc_{\text{Ctr}}$ runs at 10MHz and the $Osc_{\text{Freq}}$ oscillates at 70 MHz when $Osc_{\text{Ctr}}$ signal is set high. Fig. 8(b) depicts the ring oscillator frequency degradation for the three considered cases. One can observe that in absence of NBTI (i.e. no NBTI case), the frequency remains the same for the entire simulation time. On the other hand, the case when NBTI affects the ring oscillator and body biasing is not applied, the frequency degrades with time. As expected from the analysis of our $T_{\text{rise}}$ increment model of Section III, the oscillator frequency decreases by 9.00%. This degradation is in accordance to the observation presented in [14] and the experimental results reported [24]. Finally, when body biasing is applied to reduce the NBTI impact, the frequency degradation is only 6.70%; this means that the design for reliability technique is able to reduce NBTI impact by 34%. This improvement proves the effectiveness of the introduced design for reliability technique.

B. Leakage Current Overhead

As mentioned in the previous section, applying positive body biasing to a transistor increases its leakage current. Therefore, it is expected that our design for reliability technique will increase the leakage current of the PMOS transistors. On the other hand, in [15] Paul et al. has argued that NBTI causes exponential reduction in the leakage current. To verify the argument, a single stage of the ring oscillator is considered for the leakage current analysis. Fig. 9(a) shows leakage current reduction - in %- due to NBTI during 10 years operation. The figure shows that the reduction approaches 4.50% at the end of the operation time. This leakage reduction follows the trend presented in [15]. Therefore, the leakage current reduction caused by NBTI will automatically compensate for the leakage current increment caused by body biasing. The question is now what the overall balance of the leakage is. To answer this question, we performed simulations in one of the oscillator stage for two cases (see Fig. 9(b)): 

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Fig. 8. (a) Samples of $Osc_{\text{Ctr}}$ and $Osc_{\text{Freq}}$ waveforms (b) Frequency degradation due to NBTI with and without body biasing
Leakage with NBTI
Leakage with no NBTI
Leakage reduction (%)
Time (years)
Leakage with BB & No NBTI
Leakage with BB & NBTI
Biasing voltage (V)
(a)                                                                                           (b)

Fig. 9. (a) Leakage current reduction in absence and presence of NBTI (b) Leakage current increment due to body biasing in presence and presence of NBTI

- Leakage with BB and no NBTI: when body biasing is applied in absence of NBTI, the leakage current increment approaches 8.63%.
- Leakage with BB and NBTI: when NBTI is considered and body bias is applied to the PMOS transistor, the leakage current increment becomes only 4.09%.

Fig. 9 shows that the NBTI induced leakage reduction compensates 52.60% of the leakage current increment due to body biasing. As a consequence, the overall leakage increment due to the proposed design for reliability is not more than 4.09%.

VII. CONCLUSION

This paper has presented a scheme to monitor NBTI impact in nanoscale circuits and proposed a design technique for the circuit reliability improvement. Firstly, the impact of NBTI on gate output transition time is modeled. The analysis of the model showed that NBTI causes up to 8.56% increment in the gate output transition time. Secondly, a technique to monitor the NBTI impact is proposed; the technique is based on the measurement of the gate output transition time delay. The proposed technique converts the transition time increment into a voltage with a sensitivity of 0.50 mV/ps. Thirdly, an NBTI mitigating technique that applies a dynamic biasing voltage to redress NBTI in the circuit is proposed. The technique ensures 34% reduction in NBTI impact on the circuit in 10 years operational life. Finally, it has been shown that the leakage current overhead of the proposed technique does not exceed 4.09% for an operational life of 10 years.

REFERENCES
