Leakage-enhanced 3D-Stacked NEMFET-based Power Management Architecture for Autonomous Sensors Systems

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***Abstract*— With the technology moving into the deep sub-100 nm region, the increase of leakage power consumption necessitates more aggressive power reduction techniques using emerging devices. Power gating with Nano-Electro-Mechanical Field Effect Transistors (NEMFET) is a promising avenue to reduce energy consumption of embedded autonomous sensor systems. Our research emphasizes that 3D Stacked hybrid circuits with NEMFET sleep transistors can be further enhanced to reduce leakage power by redesigning the entire power management circuitry with NEMFETs. To evaluate the practical implications of such an approach we implement NEMFET based power gating, which makes use of NEMFETs as sleep transistors, isolation cells, and components for power management controller design, on an embedded SoC platform running a bio-medical sensing application. Preliminary energy evaluations with Cadence EDI flow indicate that the enhanced architecture provides a reduction of 7% over the 3D Hybrid architecture at the expense of 4.7% area increase and of about 15% energy reduction with respect to the "classic" 2D CMOS counterpart . Furthermore, for applications with lower activity, the potential energy improvement the enhanced architecture could provide can reach up to 90% with respect to the 2D CMOS reference design.**

I. INTRODUCTION

CMOS technology is approaching its physical limits; hence emerging technologies have been investigated and proposed to supersede the basic CMOS device, i.e., the MOSFET. Examples of such devices are Nano-Electro-Mechanical FETs (NEMFETs), carbon nano tubes, quantum-dot cellular automata, single-electron devices [1], [2], [3], [4]. However, at this time, only low complexity circuits ware successfully designed with the above technologies.

On the other hand, scaling CMOS technology could still provide 30% improvement in performance at 28 nm node with respect to 40 nm node according to [5]. The price to be paid reflects also into the tremendously increase of power dissipation of digital CMOS. Hence, the life of the battery operated embedded systems with low activity, e.g., autonomous sensor systems, which is mostly determined by the standby leakage power dissipated by the circuit in sleep mode, is directly affected. Thus, the use of power gating technique in portable devices is vital in achieving long life, low energy implementation solutions.

Power gating works on the principle of using Sleep Transistors (STs) to cut off supply voltage to the circuit in standby mode thus cutting off leakage current path to ground. Various enhancements based on Multi-Threshold CMOS (MTCMOS) technologies have been proposed to suppress the sleep transistor leakage current [6], however the NEMFET based ST proved to be more effective when compared with High-V_T counterpart [7].

One solution that partially address the leakage issue by exclusively minimizing the leakage of the ST is a hybrid CMOS-NEMS 3D stacked chip architecture. Benefitting from the NEMS-based power management, the architecture proposed in [8], emphasizes the outstanding characteristics of NEMFET devices, i.e., "abrupt" switching and ultra low leakage. To validate this proposal and evaluate its performance in a real-life scenario a careful assessment of the implications of this hybrid power management architecture on the rest of the system was described in [9].

Since power gated circuits spend very long times in standby mode, one can essentially infer that the overall energy can be further substantially reduced when the overall OFF state power consumption mostly generated by the AO cells is mitigated. In this paper we propose a novel 3D power management approach that attempts to alleviate some leakage overhead associated with the use of CMOS devices as Always-On (AO) cells, in isolation (ISO) cells and in the Power Management (PM) controller. Our proposal relies on: (i) moving the ISO cells and the PM controller on the NEMS die, and (ii) redesigning them in the NEMS technology to take advantage of the NEMFET ultra low leakage power. Our goal is to explore these implications and evaluate the performance and the energy efficacy of this power management architecture in a real-life scenario.

Our experiments indicate that, due to the extreme low leakage and the "abrupt" switching of the NEMFET, the system idle energy is decreased by 6.35x at the expance of a 4.75% area overhead on the NEMS tier. Moreover, due to the leakage-enhanced 3D hybrid approach the energy-delay product of the embedded SoC platform is reduced by 7% with a potential improvement of up to 90% with respect to the 2D CMOS reference design.

Even though the NEMFET based AO cells add overhead to the total area, this does not affect the chip footprint since it is displaced to another tier (which contains NEMFET sleep transistors). Moreover, since the AO cells are not on the critical path, their replacement with the NEMFET-based cells,

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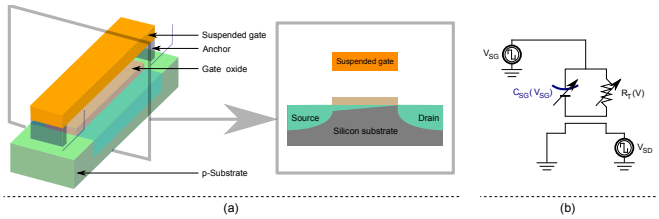

Fig. 1 (a) Schematic diagram of NEMFET. (b) Equivalent circuit model for the NEMFET.

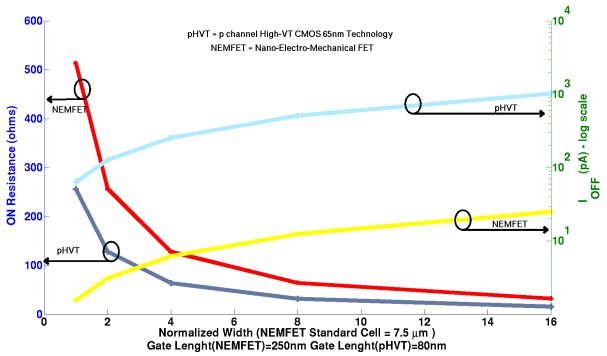

Fig. 2 R_{ON} and I_{OFF} for NEMFET and 65 nm High-V_t CMOS Switch Transistors.

which for the time being have a limited operation frequency of about 100 MHz, do not change the overall frequency of our approach. Exploiting 3D stacked hybrid integration, our approach can be applied directly on an industrial low power design which supports NEMS and CMOS technology.

The rest of the paper is organized as follows. First, in Section II, we give an overview of the 3D hybrid power management architecture and some relevant NEMFET background. Section III describes the enhanced-leakage architecture, which makes use of NEMFETs for the implementation of the entire power gating related infrastructure, i.e., sleep transistors, isolation cells, and power management controller. Section IV discusses the experimental results and finally, Section V presents the conclusions.

II. NEMFET BASED POWER MANAGEMENT ARCHITECTURE

A. NEMFET Background

The Nano-Electro-Mechanical FET (NEMFET) described in [10] is a rather complex device with a 3D geometry and cross-section as presented in Figure 1a.

Essentially speaking the device behaves like an electromechanical switch which responds to gate bias changes as follows. When the gate voltage V_G is low the gate-oxide capacitance is in series with the air-gap capacitance Figure 1b resulting in low electrostatic coupling of the gate to the channel thus in a negligible drain current I_D. If V_G increases the situation remains unchanged until it reaches a certain "ON" voltage case in which the electrostatic force cannot be compensated anymore by the mechanical restoring force and the suspended gate (beam) snaps onto the gate oxide, thus turning on the device. This is called pull-in effect and corresponds to a sudden I_D increase. After the pull-in, the I_D increase with V_G is comparable with the one of a standard MOSFET. On the other way around when V_G is decreased from some high value I_D starts decreasing until at a certain V_G value the system becomes unstable due to combined electro-mechanical force and the beam is pulled-out. This causes an abrupt I_D decrease due to a large decrease in capacitance and it is called pull-out effect.

As indicated by [7] NEMFET devices can potentially replace High-V_T sleep transistors due to their ultra low leakage characteristics. Note that for power gated designs two major features are desirable for the sleep transistors: (i) low sub-threshold leakage current to minimize the static power consumption, and (ii) low "ON" state resistance to minimize the voltage difference between the virtual and the real power supply nodes.

A comparison between the "ON" state resistance R_{ON} and "OFF" state leakage current I_{OFF} of NEMFET and 65 nm High-V_T CMOS based Sleep Transistors (STs) is presented in Figure 2 for different area in terms of standard cells. The R_{ON} values are computed for an IR-drop of 10 mV over the ST, and the I_{OFF} values consider a 1.2 V power supply. One can observe that when the ST area is increasing the NEMFET ST R_{ON} tends to become equal with the CMOS ST R_{ON}, while NEMFET ST I_{OFF} (leakage) is about 2 orders of magnitude smaller than the one of the CMOS counterpart.

B. 3D-Stacked Hybrid Power Management Architecture

In [9] the integration impact that a recent proposed 3D stacked power management architecture based on Nano-Electro-Mechanical FET power switches may have on a real-life embedded SoC design was described. The architecture relies on NEMS technology dies containing NEMFET STs placed on top of the die containing the actual power gated circuits, as in the two-tier stack test vehicle from Figure 3. The bottom CMOS tier comprises the active logic circuit, while the top tier incorporates the NEMFET STs. The dies are stacked using Through-Silicon Vias (TSVs), allowing for large density, high speed, and low power interconnect [11].

The approach has a number of advantages as follows: (i) it combines the appealing extremely low leakage currents of the NEMFETs with the versatility of CMOS technology by allowing for the power switches to be fabricated on a separate die, (ii) it simplifies the floorplanning in general, and can increase the computation platform performance because of extra area cleared by the switches on the CMOS tier, and (iii) it leverages the integration of other NEMS/MEMS devices, e.g., energy harvesters, sensors, on the same tier with the power management circuitry.

The test vehicle has three power domains (PD Core, PD DMem and PD PMem), which can be independently powered-off by the corresponding group of sleep transistor on top of the power domain. The Always-On (AO) power gating related blocks, contained in the PCM power domain are part of the bottom die. The next section presents a way to reduce the leakage power by the relocation of the

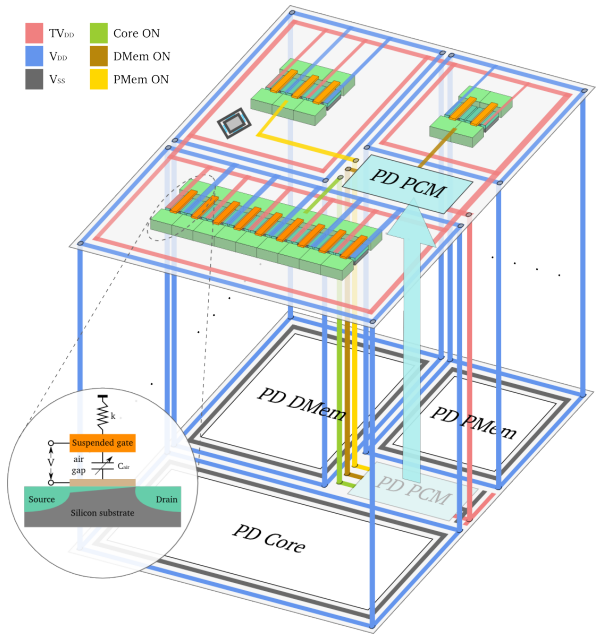

Fig. 3 Leakage-enhanced 3D Stacked NEMFET Power Management Architecture.

PCM power domain, as displayed by the light blue arrow in Figure 3.

III. LEAKAGE-ENHANCED 3D-STACKED NEMFET-BASED POWER MANAGEMENT ARCHITECTURE

We propose to enhance the above presented PM architecture by moving the Always-On (AO) power domain location to the NEMS die. This entails redesigning the isolation (ISO) cells and the PM controller in the NEMS technology. This translation alleviates part of the leakage overhead associated with the use of CMOS devices as AO cells by taking advantage of the NEMFET ultra low leakage power. The bottom CMOS tier comprises the active logic circuit, while the top tier incorporates the STs, ISO cells, and PM controller implemented with NEMFETs.

The Always ON cells include the following elements:

1) Isolation cells which controls the outputs of powered down blocks and clamp the outputs to a specific, legal value;
2) The Power Management Controller, which generates the control signals for the STs and the ISO cells in the appropriate sequence for shut-down and power-up transitions.

A. Isolation cells

Floating outputs of the power-down blocks altogether with crowbar currents during powering down may result in spurious behavior in the power-up blocks inputs [6]. Isolation cells are practically basic NAND/NOR gates, or even single pull-up/pull-down transistors with the gate input acting as the isolation signal generated by the PM controller that can hold the output to logic high/low.

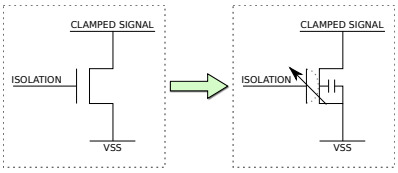

Fig. 4 Substitution of nMOS Pull-down Isolation cell with NEMFET cell.

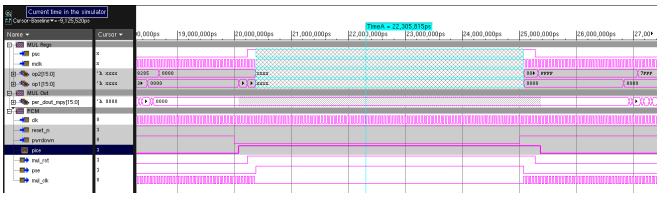

Fig. 5 Simulated waveform of Power Management Controller signals.

By replacing the isolation cells with NEMFET pull-up/pull-down transistors as indicated in Figure 4 we take advantage of the ultra-low leakage characteristic of the NEMFET to reduce with approximately two orders of magnitude the additional energy cost incurred by isolation. The twofold trade-offs are area and delay penalties. Taking into account that the operating frequency of a NEMFET based logic is currently limited to about 100 MHz and the parasitic TSV interconnect capacitance we can expect that the isolation sequence will increase from one to two clock cycles.

B. Power Management Controller

This module performs the following sequence of operations to power-down:

1) Stop the clock to minimize leakage into the power-gated region;
2) Assert the isolation control signal to park all outputs in a safe condition;
3) Assert reset to the block, so that it powers up in the reset condition;
4) Assert the power gating control signal to power down the block.

To restore power the same sequence is performed in the reversed order. The PM control signals for a complete power-down/power-up cycle simulated in Cadence LP-NCSim are depicted in Figure 5.

IV. PERFORMANCE EVALUATION

To evaluate the energy savings of the 3D stacked NEMFET based Power Management (PM) architecture an energy analysis was first performed on the Reference single-tier design with classic High-V_T sleep transistors. Subsequently, by moving the bulky STs to a different die, the Stacked design, precious area surrounding/inside the gated blocks previously allocated to them in the planar case can be reclaimed. Finally, by substituting the High-V_T STs with the equivalent area of NEMFET STs, the Hybrid implementation was analyzed.

Figure 6 presents the considered experimental platform. It consists of a typical SoC for low power embedded devices, based on the open-source 16-bit synthesizable processor core openMSP430 [12], a clone of the commercial Texas

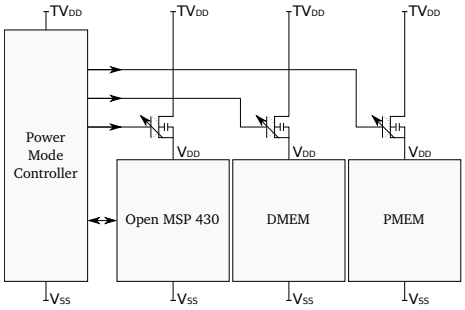

Fig. 6 System on Chip platform for autonomous sensors.

Instruments MSP430 microcontroller. The program memory (PMEM) and data memory (DMEM) sizes are 4 kB and 2 kB, respectively. Although not used by the reference application, all the peripherals of the openMSP430 core (16-bit multiplier, timer, 6 8-bit input/output ports) are part of the platform in order to account for their leakage power.

The reference application is a heart beat rate monitor which detects the QRS complex in an digitized electrocardiogram (ECG) signal. The QRS event corresponds to the depolarization of the ventricles, comprising a series of three deflections seen on a typical ECG signal. The middle one, i.e. the R wave, is the well-known "peak" of the ECG. The application program identifies the R peaks in the ECG signal and measures the interval between two consecutive R peaks. The algorithm we use is based on the open source arrhythmia detection software from EP Limited [13], which uses the filtering based Pan-Tomkins [14] method for R peak detection. For this method the input data are channeled through a five steps filtering process consisting of a low pass filter, a high pass filter, a derivative, an absolute value, and an integrator function, in this order. The utilized filter equations are valid for an ECG sample frequency of 200 Hz.

A. 3D-Stacked NEMFET-based Power Management Architecture evaluation

The reference platform was implemented using Cadence Encounter Digital Implementation [15] in a 65 nm commercial Low Power CMOS technology. A high operating frequency of the SoC means that it has to be synthesized with tighter timing constraints, which results in a design with faster and/or bigger cells. As a consequence leakage and dynamic power increase. For the presented SoC this effect limits the operating frequency to 150 MHz without causing a significant increase in the leakage power.

The obtained energy consumption values for the three designs mentioned at the beginning of this section are presented in Table I. One can observe that in spite of the reduced OFF leakage power the total improvement on the energy-delay product figure is only 9%. This happens because of two reasons: (i) the test application has a too high duty cycle, and (ii) the ON power term is dominant in the total energy equation.

The power consumption could be further reduced in two ways:

TABLE I Power and energy results

Implementation	ON power [mW]	STs	OFF power [nW] Always-on cells*	Total	Energy [µJ]
Reference	5.0340	56.28	26.02	81.28	9.05
Stacked	5.0343	900.44	26.02	925.44	9.46
Hybrid	5.0339	4.52	26.02	30.54	8.61

* Always-on cells = Power management controller and isolation cells

- addressing the OFF state power through implementing the PM controller and the isolation cells with NEMFET devices as discussed in Section III,
- optimizing the design in terms of ON state power and the software application to optimally utilize the hardware resources, hence reducing the run time.

B. Leakage-enhanced 3D-Stacked NEMFET-based Power Management Architecture evaluation

The proposed enhanced 3D power management hybrid approach makes use of the first option and redesigns the entire extra power gating logic using low-power NEMFET technology and place it on the different tier, taking advantage of the 3D stacking technology. We compare the enhanced architecture with the hybrid one and evaluate the overall energy gain from the embedded system running the biomedical application perspective. Using the same power analysis methodology we extracted the power and area values presented in Table II.

Even though the total area overhead due to logic implementation using NEMFETs is 4.75% of the design size, this does not affect the chip footprint since it is displaced to another tier (which contains NEMFET switch transistors). The prominent reduction of about two orders of magnitude in the OFF state power is due to the practical "zero-leakage" characteristic of NEMFET. Furthermore, the abrupt switching effect of the NEMFET causes a reduction in the dynamic power of PM controller and ISO cells, reducing the total ON state power. The changes in active and idle power are directly reflected in the energy figure, improving the energy consumption by 7% with respect to the hybrid design. Compared with the classic one-tier power-gated CMOS implementation Table I the overall energy saving could be up to 15%.

Figure 7 presents a comparison of the system idle power for the classic High-V_T Reference, i.e., the 3D Hybrid, and the proposed Leakage-enhanced architectures. The idle power is equal with the leakage power of the only active components in the idle state, the STs and the AO cells. A two-step approach to reduce the leakage power can be observed. Hybrid design implements in the first step only the STs in the NEMFET die, which results in a substantial reduction of the ST leakage but doesn't affect the AO cell figure of merit. In the second step, the Leakage-enhanced design contains all STs, AO cells and the complete PM circuit on the top die, implemented with NEMFETs. In total, by using the Leakage-enhanced architecture, we reduce the

TABLE II Leakage-enhanced architecture area, power and energy results

Implementation type	Area [% of die size]		ON power	OFF power [nW]			Total energy*
	ISO cells	PM Controller	[mW]	STs	ISO cells	PM Controller	[µJ]
Hybrid [9]	0.15	0.02	5.0339	4.52	18.01	8.01	8.61
Leakage-enhanced	3.75	1.17	4.7	4.52	0.289	0.075	8.00

* Active time=1.73 ms, Idle time=993.35 ms, Transition time=5.32 ms @ 150 MHz.

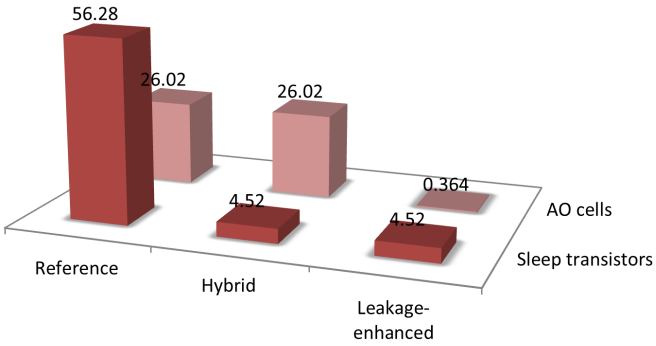

Fig. 7 Breakdown of leakage power (in nW) in an embedded processor for autonomous sensors.

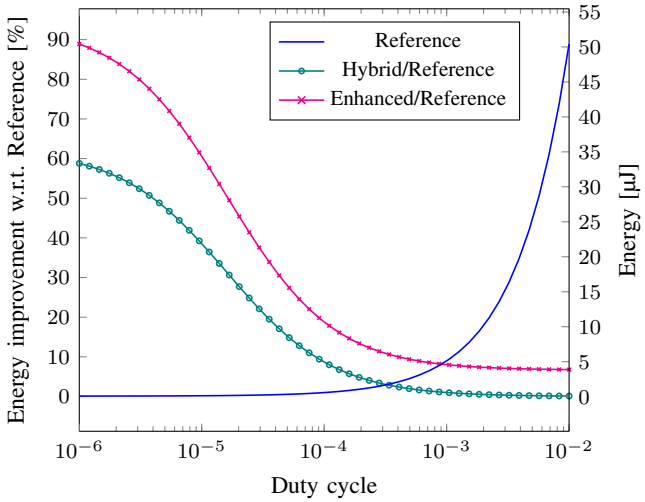

Fig. 8 Energy Consumption versus Duty-cycle.

leakage power in the idle state with 92%, from 82.3 nW in the 2D Reference design to 5.884 nW.

The ON state power consumption can be further reduced by optimizing the design in terms of power and the software application to optimally utilize the hardware resources, thus reducing the run time. To characterize the energy consumption efficiency versus various applications, we plot in Figure 8 the platform energy consumption for different operating duty cycles. We assume the same ON and OFF state power figures as for the bio-medical application. The duty-cycle is defined as: $T_{ON}/(T_{ON}+T_{OFF})$.

One can observe in the figure that the energy requirement has a steep decrease until the application duty-cycle reaches 0.0001. Optimizing and reducing the application duty-cycle lower than this does not bring much energy savings any longer. However, from this point further, for even lower activity applications the relative savings in energy consumption due to our power architecture when compared to High-V_T STs start to increase, reaching up to 90% lower energy consumption. Compared to the previous 3D-Stacked Hybrid PM architecture the overall energy improvement is about up to 50% higher.

V. CONCLUSIONS

In this paper, we diminished the leakage power of the NEMFET based 3D-stacked power management architecture by making use of NEMFETs also for the implementation of isolation cells, and power management controller design. We evaluated the practical implications of such an approach by implementing an embedded SoC platform running a bio-medical sensing application with NEMFET based power gating. We performed energy evaluation of the enhanced design and our results indicated a reduction of 7% over the 3D Hybrid architecture with the price of 4.7% increase in area and of about 15% energy reduction with respect to the "classic" 2D CMOS counterpart. Furthermore, for applications with lower activity, the potential energy improvement of the Leakage-enhanced architecture could deliver can reach up to 90%, with respect to the 2D CMOS reference design. Our results suggest that when utilized in conjunction with CMOS the NEMFETs can induce significant performance improvements over CMOS only approaches in terms of energy efficiency. This justifies the need for further efforts in evaluating other aspects of the novel power management architectures, such as reliability and technology integration issues.

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