A Low-Power Threshold Logic Family

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ABSTRACT

This paper presents a new low-power Threshold Logic family featuring self lock-out and run-time reprogrammability. The simulated results have shown that, the proposed Threshold Logic dissipates between 10% and 79% less power and between 57% and 71% less energy, at $V_{dd} = 5V$, when compared with previous similar Threshold Logic families. Moreover, at $V_{dd} = 3.3V$, it has between 12% and 48% less energy and between 34% and 60% less dissipated power in the worst case.

1. INTRODUCTION

Traditional digital IC implementations are based on Boolean theory. As the operands length is becoming larger and larger, Boolean implementation performance might be severely affected by a large circuit depth and alternative solutions are required. A potential alternative to Boolean Logic appears to be Threshold Logic (TL) [6] which makes use of a generalized basic building block named *Linear Threshold Gate* (LTG). Such an LTG is a multi-terminal device which performs two basic operations: input weighting and thresholding. The output is logic one if the weighted sum of the input values is greater than the threshold value, T, and zero otherwise.

More formally, the output of a linear threshold gate is given by:

$$F(X) = sgn\{\mathcal{F}(X)\} = \begin{cases} 0, & \text{if } \mathcal{F}(X) < 0 \\ 1, & \text{otherwise} \end{cases} \quad (1)$$

$$\mathcal{F}(X) = \sum_{i=0}^{n-1} \omega_i x_i - T \quad (2)$$

where the set of input variables and weights associated with the inputs are defined by $X = \{x_0, x_1, \ldots, x_{n-1}\}$ and $\Omega = \{\omega_0, \omega_1, \ldots, \omega_{n-1}\}$, respectively.

Given that LTGs are fundamentally more powerful than the conventional Boolean gates a number of theoretical investigations have been reported regarding the possibilities of such an approach in the design of useful Boolean functions [2], [6], [9]. Speaking from the device/circuitry point of view the main advantage of LTGs when compared to standard Boolean gates is the parallel processing due to internal multiple-valued computation of the weighted sum. However when compared to classical multiple-valued logic circuits LTG gates are more robust against parameter variation because the LTG inputs and output are still digital encoded. Consequently, TL implementations have received considerable attention in the early 90's [5], [8], [10] and later, with the technology advances, more LTG implementations have been proposed [1], [3], [7].

Although the so called Neuron MOS transistor (νMOS) [10] is very compact, it suffers from process dependence due to the unpredictable resolution and reprogramming relies ultimately on UV erasure. The implementations proposed in [5] and [8] although favorable in integration density, suffer from high nonlinearity and power consumption.

Capacitive Threshold Logic (CTL) [7] has a high fan-in capability but performs weighting using a capacitive bank which is prone to a high area in a typical CMOS technology. Moreover, thresholding is performed with a properly designed inverter chain, which suffers from a lower speed at higher fan-in. In addition, CTL gate exhibits DC power consumption in evaluation phase which restricts its utilization only for rather small designs.

Recently, two latch-based LTGs [1], [3] were disclosed. In contrast with previous LTGs, both feature only dynamic power consumption and are differential. The gates have in common two parallel connected sets of nMOS transistors implementing basically the weighting operation and a CMOS compara-

tor based on cross-coupled inverters.

The latch-type comparator TL (LCTL) [1], features an internal self-locking mechanism to cut-off the power supply current immediately after the evaluation but the internal latch has a high recovery time caused by a long feedback chain. While cross-coupled inverters with asymmetrical loads TL (CIALTL) [3] has the nMOS banks external to the CMOS latch, and thus reducing dynamic power consumption, it has a great amount of power dissipated in the internal clock front end.

In the present paper we propose a low-power latch-based LTG based on differential-current switch logic (DCSL) [11]. Compared with the LTGs presented above, our scheme has the following advantages:

- higher speed when compared with LCTL since the $Clk - Y$ delay is imposed by a simpler latch;

- less dissipated dynamic power when compared with CIALTL. This is both due to the true single phase clock operation and due to a more restricted voltage swings in the internal highly capacitive nodes.

The simulated results have shown the new LTG dissipates between 10% and 79% less power and between 57% and 71% less energy, at $V_{dd} = 5V$, when compared with previous similar LTGs. Moreover, at $V_{dd} = 3.3V$, it has between 12% and 48% less energy and between 34% and 60% less dissipated power in the worst case.

The paper is organized as follows. Section 2 presents the new LTG schematic and its mode of operation. Section 2 ends with a presentation of two features (re-programmability and symmetry). Section 3 presents the simulated conditions and comparison results followed by a brief conclusion in Section 4.

2. GATE DESCRIPTION AND OPERATION

The proposed LTG circuit is depicted in Figure 1. It will be recalled throughout this paper as Differential Current-Switch Threshold Logic (DCSTL)

The comparator is implemented with a strobed CMOS latch circuit while the analog computation blocks consist of two parallel connected sets of nMOS transistors, referred from this point as *nMOS banks*. In order to make a clear difference between both previous banks, we will recall the inputs assigned to the left bank as *data inputs* while the inputs assigned to the right bank as *threshold mapping*
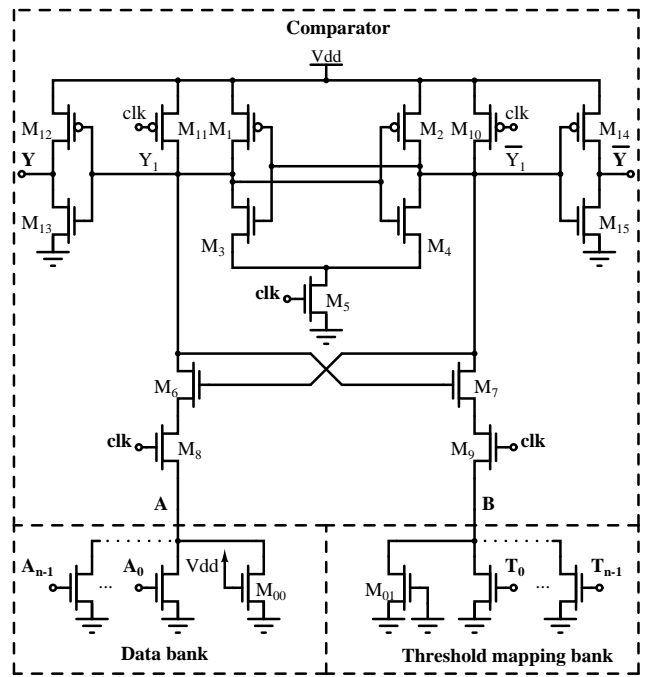

Fig. 1. Proposed DCSTL gate schematic

inputs. However, as it will be shown later in this section, there is no clear difference between data and threshold mapping inputs, since implementing negative weights will require to connect the corresponding transistor gates in the opposite bank. The comparator decides if the voltage level in Y_1 is greater than the voltage level in $\overline{Y_1}$. Those voltages are imposed by the currents generated in both nMOS banks.

The gate is in principle a clocked differential cascode voltage switch (DCVS) circuit, operated with a single phase clock. M_{10} and M_{11} are precharge transistors while CMOS inverters $M_{12} - M_{13}$, $M_{14} - M_{15}$ are provided for buffering to succeeding LTG stages. M_6 and M_7 are two transistors introduced to achieve both reduced voltage swing (and thus power dissipation) in the nMOS trees and automatic lock-out of inputs. The dynamic operation of this LTG is divided into a precharge phase and an evaluation phase.

During precharge phase, *clk* low switches on M_{10}, M_{11} precharging the parasitic capacitors from Y_1 and $\overline{Y_1}$. The evaluation phase starts with *clk* high, switching on the nMOS transistors M_5, M_8, M_9, and cutting off M_{10} and M_{11}. The currents flowing from the nMOS banks discharge the parasitic capacitors and the voltage difference between Y_1 and $\overline{Y_1}$ is amplified to a voltage swing nearly equal to the power supply voltages. The evaluation is performed in two steps. During the first step the dynamic latch don't regenerate because both Y_1 and $\overline{Y_1}$ node voltages are greater
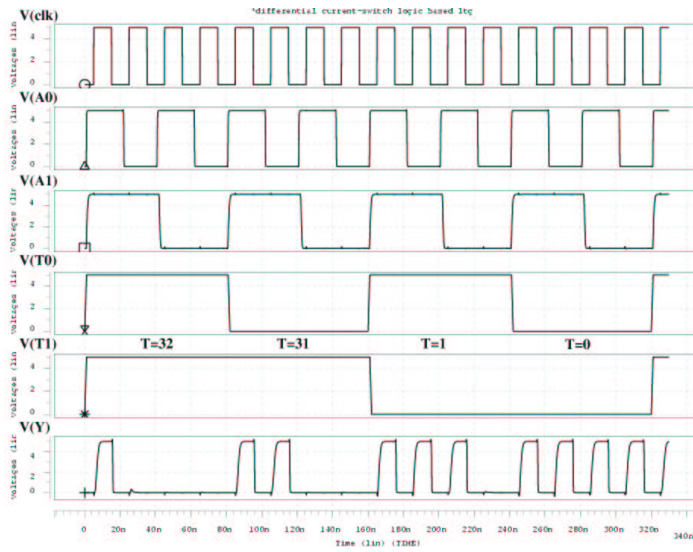
Fig. 2. Spice simulation results of a reconfigurable DCSTL gate

than inverter's threshold. During the second step, the latch rapidly regenerates according to the voltage difference between the nodes. Assuming the left bank current greater than the current in the right one, M_7 tend to switch off while M_6 progressively switches on and thus, the high going internal node is decoupled from being connected to ground, reducing power.

The presented gate features the interesting property of being *run-time re-programmable* since the Threshold Logic Function (TLF) can be changed dynamically between two evaluations. In order to have a clear view of the run-time re-programmability feature, in Figure 2 there are presented the Spice simulated waveforms of a DCSTL gate having $n = 32$. The gate has two data inputs (*A0, A1*) and two threshold mapping inputs (*T0, T1*). Both the data input *A0* and the corresponding threshold mapping input *T0* have identical weights ($\omega_0 = 1$) while *A1* and *T1* have the associated weight $\omega_1 = 31$. During the simulation, the inputs and threshold values were sweeped through all possible combinations such as four TL functions are possible. In two representative cases (*T0=1, T1=1* and *T0=1, T1=0*) the gate is configured as a 32-input AND/OR gate. It can be remarked that TL gate performs correctly with all applied input vectors.

Another interesting feature of this LTG is the capability to implement both positive and negative weights and thresholds. This comes from the symmetrical nature of the general structure presented above. For example, a LTG having an input with a negative weight, ω_k, can be easily derived from a LTG with identical absolute weight value, $-\omega_k$, by simply moving the corresponding data input, X_k, in the threshold-mapping block. Of course, the balancing condition (the total sum of transistor widths must be identical in both nMOS banks) must hold true and consequently ω_k dummy transistors must be added in the data bank.

3. PERFORMANCE EVALUATION

The proposed gate performance is compared with CIALTL [3] and LCTL [1]. To have a fair comparison, we used a 31-input AND function as a benchmark ($T = 31$) because it achieves the highest level of current generated by the threshold mapping block. Also, all three gates were simulated with an identical load of 100fF and the input signals were applied via minimum-sized inverters. The results were obtained in 1.6μ gate length CMOS technology using Philips MOS Level 9 models [4], at room temperature.

For all considered gates, the transistor's geometries were optimized to achieve the minimum gate power-delay-product using the HSpice optimizer. The power was computed as the sum between the power dissipated in the internal gate, necessary to switch the load capacitance and the power dissipated in the clock drivers. During the simulation-optimization cycle, 30 inputs of the gates are logic one and a single input switches. Since the CMOS latch has to evaluate correctly even in that case, with a small amount of voltage difference between the differential latch inputs, this is the worst case from the power dissipation point of view.

Table 1 summarizes the simulated characteristics of each LTG after power-delay product optimization. Note that, when compared with CIALTL, DCSTL exhibits an average delay penalty of at most 30%, given the higher strength of the nMOS trees but saves 60% power mainly due to the single phase clock operation and a lower voltage swing of the nodes A and B.

Conversely, LCTL is with 22% slower than DCSTL and has 10% more dynamic power dissipation. DCSTL and LCTL have lower power dissipation when compared with CIALTL because they present quite similar mechanisms of reducing the power supply currents by self-locking of the outputs and both are operated with a single-phase clock scheme. However, when compared with LCTL and CIALTL, in terms of power-delay-product, DCSTL has between 57% and 71% less energy, at $V_{dd} = 5V$, and between 12% and 48% less energy at $V_{dd} = 3.3V$.

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| | $V_{dd} = 5V$ | | | | $V_{dd} = 3.3V$ | | | | # of |
	Power [μW]	Delay [ps]	PDP [pJ]	Total Gate Width [μm]	Power [μW]	Delay [ps]	PDP [pJ]	Total Gate Width [μm]	Tran.
DCSTL	729	358	0.261	244	293	715	0.209	270	$17 + 2 \cdot n$
CIALTL	1325	288	0.381	218	468	505	0.236	245	$27 + 2 \cdot n$
LCTL	840	524	0.440	208	393	1793	0.704	190	$14 + 2 \cdot n$

Table 1. LTGs simulated characteristics @ $V_{dd} = 5V$ and $V_{dd} = 3.3V$; $n = 33$

4. CONCLUSIONS

In this paper a Differential Current-Switch Threshold Logic (DCSTL) for low-power was presented. The simulated results have shown that, the proposed Threshold Logic family dissipates between 10% and 79% less power and between 57% and 71% less energy, at $V_{dd} = 5V$, when compared with previous similar Threshold Logic families. Moreover, at $V_{dd} = 3.3V$, it has between 12% and 48% less energy and between 34% and 60% less dissipated power in the worst case.

5. REFERENCES

[1] M. Avedillo, J. M. Quintana, A. Rueda, and E. Jimenez, "Low-power CMOS threshold-logic gate", *Electric Letters*, Vol. 31, pp. 2157-2159, 1995;

[2] S. Cotofana, S. Vassiliadis, "Periodic Symmetric Functions, Serial Addition and Multiplication with Neural Networks", *IEEE Trans. on Neural Networks*, Vol. 9, no. 6, pp. 1118-1128, 1998;

[3] J. Fernandez Ramos, J. A. Hidalgo Lopez, M. J. Martin, J. C. Tejero, and A. Gago, "A threshold logic gate based on clocked coupled inverters", *International Journal of Electronics*, Vol. 84, no. 4, pp. 371-382, 1998;

[4] H.C. de Graaff, F.M. Klaassen, "Compact Transistor Modelling for Circuit Design", *Springer-Verlag*, 1990;

[5] C. L. Lee, C.-W. Jen, "Bit-sliced median filter design based on majority gate", *IEE Proceedings-G*, Vol. 139, no. 1, pp. 63-71, 1992;

[6] S. Muroga, "Threshold Logic and its Applications", *Wiley and Sons Inc.*, 1971;

[7] Y. Leblebici, H. Ozdemir, A. Kepkep, and U. Cilingiroglu, "A compact high-speed (31,5) parallel counter circuit based on capacitive threshold-logic gates", *IEEE Journal of Solid-State Circuits*, Vol. 31, no. 8, pp. 1141-1150, 1996;

[8] K. Schultz, R. Francis, and K. Smith, "Ganged CMOS: trading standby power for speed", *IEEE Journal of Solid-State Circuits*, Vol. 25, no. 3, pp. 870-873, 1990;

[9] K. Y. Siu, J. Bruck, "Neural Computing of Arithmetic Functions", *Proc. IEEE*, Vol. 17, no. 10, pp. 1669-1675, 1990;

[10] T. Shibata, T. Ohmi, "A functional MOS transistor featuring gate-level weighted sum and threshold operations", *IEEE Transactions on Electron Devices*, Vol. 39, no. 6, pp. 1444-1455, 1992;

[11] D. Somasekhar, K. Roy, "Differential current switch logic: a low power DCVS logic family", *IEEE Journal of Solid-State Circuits*, Vol. 31, no. 7, pp. 981-991, 1996.