DPM Reduction on Dual-Port Caches

Said Hamdioui[1,2] Ad J. van de Goor[2] Mike Rodgers[1]

[1]Intel Corporation, 2200 Mission College Boulevard, Santa Clara, CA 95052, USA
[2]Delft University of Technology, Faculty of Information Technology and Systems
Section of Computer Engineering, Mekelweg 4, 2628 CD Delft, The Netherlands
E-mail: said@ce.et.tudelft.nl

Abstract: *This paper presents two linear tests for unique faults in dual-port SRAMs: a single-addressing tests (March s2PF-), and a double-addressing test (March d2PF-). The faults for which the tests are designed are developed using defect injection and circuit simulation of all possible resistive defects at the electrical level. An analytical as well as an industrial evaluation of the two tests, together with other used dual-port tests will be presented. Although predicted by IFA, the production Defect per Million (DPM) screening of March s2PF- and March d2PF- on two different designs was surprising. The DPM was measured at 680 for one layout and at 141 for the other one. This calls for the necessity of considering March s2PF- and March d2PF-, or leaving substantial DPM on table.*

Key words: *dual-port/single-port SRAMs, fault models, march tests, fault coverage, DPM, IFA.*

1 Introduction

Multi-port (MP) memories are memories having multiple ports used to access the memory cells simultaneously and independent of each other. The rapid development in memory technology demands new test patterns not only to reduce the memory test costs, but also to enhance the defect detection capability. Many fault models and test algorithms have been proposed during the past ten years for MP memories. Most of these fault models and algorithms were written from a purely mathematical point of view and there is hardly any insight in their practical importance. In [16], an *ad hoc* test with no specific fault model was described. In [14], a BIST circuit, based on a serial interfacing technique for embedded dual-port (i.e, *two-port (2P)*) SRAMs, was reported. However, the used fault models were very *simplistic*. In [3, 15, 17, 6] *theoretical* fault models, together with their tests, were developed. However, the introduced fault models were *not* based on any experimental/industrial analysis; and the proposed tests have a time complexity which is *exponentially* proportional with the number of ports of the MP memory; that makes them not practical. In [7], port interferences in 2P memories were *experimentally* analyzed, based on an industrial design and SPICE simulation; however, the analysis was restricted only to the interference between the two ports. A similar, but theoretical work, has been reported in [18].

In our previous work [8], a *specific* Intel 2P cache *layout* has been analyzed using Inductive Fault Analysis (IFA). The defect analysis has been into two steps. First, the translation of the defect in the layout to defects in the electrical circuit diagram has been done. Second, the simulation of that defect has been performed. The found electrical faults have been translated into fault models, for which test algorithms have been introduced. However, these fault models and tests apply only to that layout (i.e., they are layout-dependent) since only defects occurring in that cache layout were considered. The found fault models are in fact a subset of the whole realistic fault model space for dual-port SRAMs. The complete set of fault models, based on defect injection and circuit simulation of *all* possible resistive defects, has been presented in [9, 10]; however, the tests were not presented.

This paper presents tests targeting the whole space of realistic faults in dual-port SRAMs, as introduced by [9, 10]. The paper is organized as follows: Section 2 lists an overview of realistic fault models for 2P memory cell arrays, as established in [9, 10]. Section 3 gives optimal march tests for detecting unique dual-port faults. Section 4 presents an analytical as well as an industrial evaluation of the new dual-port tests and the conventional ones; while Section 5 ends with conclusions.

2 Fault models for 2P-SRAMs

In [9, 10], a complete *experimental analysis* for resistive defects in a differential 2P SRAM (Intel design)

has been done. The SPICE simulation of all possible defects at the electrical level of the memory cell has been performed by examining the resistance range of each resistive defect from 0 to ∞. The used simulation methodology verifies all allowed operations in the analyzed 2P memory. During the simulation, any electrical faulty behavior (in the presence of a certain resistive defect) is reported in terms of a *fault primitive (FP)*; a FP is a compact notation describing a single fault behavior. The FPs are translated into *functional fault models (FFMs)*, whereby a FFM is defined as a non empty set of FPs. A detailed description of all FFMs is presented in [9, 10]. In this section a brief overview will be given.

The FFMs for 2P memories are divided into single-port faults and unique two-port faults.

2.1 Single-port faults

Single-port faults (denoted as $1PFs$) are divided into faults involving a *single-cell (1PF1s)* and faults involving *two-cell (1PF2s)*. The 1PF1s have the property that the cell used for sensitizing the fault is the same cell as where the fault appears. FFMs like *Stuck at Fault*, *Transition Fault*, and *Read Destructive Fault* [2] belong to this subclass. The 1PF2s represent the subclass of coupling faults involving an *aggressor cell (a-cell)* and a *victim cell (v-cell)*. FFMs like *State Coupling Fault* [5], *Disturb Coupling Fault* [19], *Read Destructive Coupling fault* [9, 10] belong to this subclass.

2.2 Unique two-port faults

Two-port faults (2PFs) cannot be sensitized using single-port operations. They require the use of the two ports *simultaneously*; and therefore they are unique for 2P memories. They are divided into *faults involving a single cell (2PF1s)* and *faults involving two cells (2PF2s)*; see Figure 1. A detailed description of such faults is given in [9, 10].

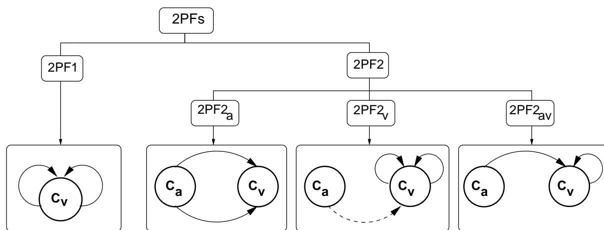

Figure 1: Classification 2PFs

1. *The 2PFs involving a single cell (2PF1s)*: They are based on a combination of two single-port operations applied simultaneously via two ports to a single cell; the cell accessed is the same cell as where the fault appears. E.g., applying two simultaneous read operations to the v-cell causes the v-cell to flip and the sense amplifiers return *correct* or *incorrect* values. This subclass consists of three functional fault models (FFMs), each with two fault primitives (FPs) [9]; see Table 1.
2. *The 2PFs involving two cells (2PF2s)*: Depending on to which cells the two simultaneous operations are applied (to the a-cell, and/or to the v-cell), the 2PF2s can be further divided into three types:
   (a) The $2PF2_a$: This fault is sensitized in the v-cell c_v by applying two simultaneous operations to the same a-cell c_a. E.g., applying two simultaneous operations to the a-cell will cause the v-cell to flip. This type consists of one FFM with eight FPs [9]; see Table 1.
   (b) The $2PF2_v$: This fault is sensitized in the v-cell by applying two simultaneous operations to the same v-cell (solid arrows in Figure 1), while the a-cell has to be in a certain state (dashed arrow in the figure). E.g., applying two simultaneous read operations to the v-cell will cause the v-cell to flip, *if* the a-cell is in a certain state; the read operations then return *correct* or *incorrect* values. This type consists of two FFMs, each with four FPs [9]; see Table 1.
   (c) The $2PF2_{av}$: This fault is sensitized in the v-cell by applying two simultaneous operations: one to the a-cell and one to the v-cell. E.g., a read operation applied to the v-cell changes the data in the v-cell, and returns a *correct* or *an incorrect* value on the output, *if simultaneously* an operation is applied to the a-cell. This type consists of two FFMs, each with four FPs [9]; see Table 1.

Table 1: Number of FFMs and FPs for 2PFs

Faults	# of FFMs	# of FPs
2PF1	3	$3 \times 2 = 6$
$2PF2_a$	1	$1 \times 8 = 8$
$2PF2_v$	2	$2 \times 4 = 8$
$2PF2_{av}$	2	$2 \times 4 = 8$
Total	8	30

3 Tests for two-port faults

The FFMs for 2P SRAMs are divided into 1PFs and 2PFs. Therefore, the test procedure can be divided into two parts:

a. Test(s) to detect 1PFs, and

b. Test(s) to detect 2PFs.

Tests for 1PFs are described in the literature like in [1, 5, 12, 19, 20]; while tests for 2PFs have to be derived. Below, tests for detecting all possible 2PFs will be given. However, first the march notation used for single-port memories has to be extended in order to specify tests for 2P memories.

3.1 Notation for March tests

The extension will be done as follows:

- A complete march test is delimited by the '{...}' bracket pair, while a march element is delimited by the '(...)' bracket pair. The march elements are separated by semicolons, and the operations within a march element are separated by commas.
- The operations applied in parallel to the ports are separated using colons, and the port number to which each of the set of the parallel operations is applied is determined implicitly. E.g., the march element $(r0 : w1)$ denotes two simultaneous operations: a 'read 0' operation applied to the first port (P1), and a 'write 1' operation applied to the second port (P2).
- The character 'n' denotes *no operation*, while the character '$-$' denotes *any allowed operation*. For example, $(r0 : n)$ denotes a $r0$ operation via P1, and no operation on P2.
- The cell to which the operation is applied can be specified explicitly by subscripting the corresponding operation. E.g., $(r0_{r,c})$ denotes a $r0$ operation applied to the cell in row r and column c.
- $\Updownarrow$: denotes an up addressing ($\Uparrow$), or a down addressing ($\Downarrow$) sequence. $\Uparrow_{c=0}^{C-1}\Uparrow_{r=0}^{R-1}$: denotes a nested addressing sequence, whereby c goes from 0 to $C-1$; and for each value of c, r goes from 0 to $R-1$.

3.2 March s2PF- and March d2PF-

By inspecting each subclass and fault type of the 2PFs, one can conclude that, depending on the type of addressing required in order to be sensitized, the 2PFs can be divided into two classes:

1. *Single-addressing 2PFs*: these are faults which can be sensitized by accessing one cell at a time (i.e., both ports use the same address simultaneously). They consist of 2PF1, $2PF2_a$ and $2PF2_v$ faults.
2. *Double-addressing 2PFs*: these are faults which can be sensitized by accessing two different locations at a time (i.e., two ports use two different addresses simultaneously). They consist only of the $2PF2_{av}$ faults.

Therefore, the test required for single-addressing 2PFs will be a single addressing test, while the test required for double-addressing 2PFs will be a double addressing test.

3.2.1 Single-addressing test: March s2PF-

In [11], a systematic way has been developed in order to establish a march test detecting all single-addressing 2PFs. First, the detection condition for each FFMs has been determined, and thereafter they have been compiled into a linear march test. The test, called *March s2PF-*, is given in Figure 2. ('-' is added to the name to denote the optimal version of March s2PF [11]). March s2PF- has a test length of $14n$, where n is the size of the memory. It detects all single-addressing 2PFs; i.e., 2PF1, $2PF2_a$ and $2PF2_v$ faults [11].

$$\{ \underbrace{\Updownarrow (w0:n)}_{M_0} ; \underbrace{\Uparrow (r0:r0, r0:-, w1:r0)}_{M_1} ; \underbrace{\Uparrow (r1:r1, r1:-, w0:r1)}_{M_2} ; \underbrace{\Downarrow (r0:r0, r0:-, w1:r0)}_{M_3} ; \underbrace{\Downarrow (r1:r1, r1:-, w0:r1)}_{M_4} ; \underbrace{\Downarrow (r0:-)}_{M_5} \}$$

Figure 2: March s2PF- for single-addressing 2PFs

For example the 2PF1s are detected as follows.

- M_0 of March s2PF- initializes all memory cells to 0.
- M_1 consists of three operations:
  - "$r0 : r0$": this operation sensitizes and detects the fault whereby two simultaneous "$r0$" operations applied to the v-cell cause the v-cell to flip and the sense amplifiers return *incorrect* values. In addition, it sensitizes the fault whereby two simultaneous "$r0$" operations applied to the v-cell cause the v-cell to flip and the sense amplifiers return *correct* values. The latter fault will be detected by the second operation of M_1; i.e., "$r1 : -$". Note the '$-$' can be replaced with the '$r1$' operation.
  - "$w1 : r0$": this operation sensitizes a fault whereby an up transition write operation fails

$$
\begin{array}{l}
\{ \Updownarrow (w0:n) \;;\; \Uparrow_{c=0}^{C-1} (\Uparrow_{r=0}^{R-1} (w1_{r,c} : r0_{r+1,c})) \;;\; \Uparrow_{c=0}^{C-1} (\Uparrow_{r=0}^{R-1} (w1_{r,c} : r1_{r+1,c})) \;; \\
\quad M_0 \qquad\qquad\qquad M_1 \qquad\qquad\qquad\qquad\qquad M_2 \\
\Uparrow_{c=0}^{C-1} (\Uparrow_{r=0}^{R-1} (w0_{r,c} : r1_{r+1,c})) \;;\; \Uparrow_{c=0}^{C-1} (\Uparrow_{r=0}^{R-1} (w0_{r,c} : r0_{r+1,c})) \;; \\
\qquad M_3 \qquad\qquad\qquad\qquad\qquad M_4 \\
\Uparrow_{c=0}^{C-1} (\Uparrow_{r=0}^{R-1} (w1_{r,c} : r0_{r,c+1})) \;;\; \Uparrow_{c=0}^{C-1} (\Uparrow_{r=0}^{R-1} (w1_{r,c} : r1_{r,c+1})) \;; \\
\qquad M_5 \qquad\qquad\qquad\qquad\qquad M_6 \\
\Uparrow_{c=0}^{C-1} (\Uparrow_{r=0}^{R-1} (w0_{r,c} : r1_{r,c+1})) \;;\; \Uparrow_{c=0}^{C-1} (\Uparrow_{r=0}^{R-1} (w0_{r,c} : r0_{r,c+1})) \; \} \\
\qquad M_7 \qquad\qquad\qquad\qquad\qquad M_8
\end{array}
$$

Figure 3: March d2PF- for double-addressing faults

if simultaneously a read operation is applied to the same location. This fault will be detected by first operation of M_2 (i.e., "$r1 : r1$"). Note that simultaneous write and read of the same location is assumed to be allowed[1]; while the read data will be discarded (i.e., the write operation has the high priority). If this is not supported, then the "$w1 : r0$" will be replaced with "$w1 : n$'.

- M_2 consists of three operations; a similar explanation can be given as that for M_1.

3.2.2 Double-addressing test: March d2PF-

It has been shown in [9, 11], by using the inductive fault analysis (IFA) and SPICE simulation, that the $2PF2_{av}$ can only be caused by defects between physical adjacent cells in the same row or column. That means that if the a-cell is $c_a = c_{r,c}$ (i.e., a cell in row r and column c), then the v-cell has to be $c_{r\pm1,c}$ or $c_{r,c\pm1}$; i.e., the distance between a-cell and v-cell is just 1.

The test shown in Figure 3, with a test length of $9n$, referred to as *March d2PF-*, detects all $2PF2_{av}$ faults [11]; R (C) represents the number of rows (columns) in the memory cell array. E.g., the operation"$w1_{r,c} : r0_{r+1,c}$" in M_1 will sensitize and detect the following faults:

- A fault whereby a "$r0$" operation performed on the v-cell (i.e., $c_{r+1,c}$) changes the data in the v-cell, and returns an *incorrect* value on the output, *if* simultaneously a write is applied to the a-cell (i.e., $c_{r,c}$). The a-cell and the v-cell are adjacent cells in the same column.
- A fault whereby a "$r0$" operation performed on the v-cell (i.e., $c_{r+1,c}$) returns an *incorrect* value on the output while the state of the v-cell does not change, *if* simultaneously a write is applied to the a-cell (i.e., $c_{r,c}$).

[1]this is allowed in some designs to reduce the control logic, and therefore facilitating the design

It should be noted that in case $r = R$ (or $c = C$), then $r + 1$ should be replaced with $(r + 1) mod^2 R$ (and $c+1$ with $(c+1) mod\, C$). Note also that March $2PF2_{av}$-requires the use of *topological* addressing rather than logical addressing, since it has to address adjacent cells in the same row and in the same column.

4 Evaluation of dual-port tests

In this section, first an analytical comparison of March s2PF- and March d2PF- with other industrial dual-port tests will be presented. Thereafter, some results of an experiment performed at Intel will be listed. In the experiment, the dual-port tests have been implemented and applied to real designs in order to industrially evaluate them.

4.1 Analytical evaluation of the tests

Most industrial dual-port tests are based on the extension of the conventional tests designed for single-port memories. Here, three single-port memory tests will be considered and extended to dual-port tests: Scan [1], March C- [13, 20], PMOVI [4]; these tests are extended by replacing the single read operation with two simultaneous read operations. For example:

Scan=$\{\Uparrow (w0); \Uparrow (r0); \Uparrow (w1); \Uparrow (r1)\}$

is changed into dual-port Scan (2P-Scan) as:

$\{\Uparrow (w0 : n); \Uparrow (r0 : r0); \Uparrow (w1 : n); \Uparrow (r1 : r1)\}$.

In addition, the two algorithms presented by [18] for dual-port memories will be considered; they are called MMCA and WIPD:

MMCA=$\{\Uparrow_{i=0}^{n-1} (w0_i);$
$\Uparrow_{i=0}^{n-1} (r0_i : rx_{i-2},\, w1_i : rx_{i+2});$
$\Uparrow_{i=0}^{n-1} (r1_i : rx_{i-2},\, w0_i : rx_{i+2});$
$\Downarrow_{i=0}^{n-1} (r0_i : rx_{i-2},\, w1_i : rx_{i+2});$
$\Downarrow_{i=0}^{n-1} (r1_i : rx_{i-2},\, w0_i : rx_{i+2});$
$\Updownarrow_{i=0}^{n-1} (r0_i : n)\}$

[2]a mod b= the remainder of dividing a by b

where 'rx' denotes a read data 'x" without observing it, and 'n' denotes no operation.

WIPD={$\Uparrow_{i=0}^{n-1}$ $(w0_i)$;
$\Uparrow_{i=2-1}^{n-1}$ $(w0_i : w1_{i-2},\ r0_{i-1} : n)$; $\Uparrow_{i=0}^{n-3}$ $(r1_{i-1} : n)$;
$\Uparrow_{i=2-1}^{n-1}$ $(w1_i : w0_{i-2},\ r1_{i-1} : n)$; $\Uparrow_{i=0}^{n-3}$ $(r0_{i-1} : n)$}

Table 2 summarizes the fault coverage of all the dual-port tests considered here; all tests have a linear time complexity. The test length (T.L.) of each test is also given; n denotes the size of the memory. In the table, "a/b" denotes that the test detects 'a' of the 'b' FPs of the correspondent fault subclass. E.g., 2P-March C- detects two FPs of the total of six FPs that 2PF1 fault class consists of; see also Table 1. The table clearly shows that using the first five tests (i.e., 2P-Scan, 2P-March C-, 2P-PMOVI, MMCA and WIPD), the fault coverage of the targeted unique 2PFs will be not 100%. This is well the case by using March s2PF- and March d2PF-.

Table 2: Comparison of the dual-port tests

Tests	T. L.	2PF1	$2PF2_a$	$2PF2_v$	$2PF2_{av}$
2P-Scan	$4n$	2/6	1/8	2/8	0/8
2P-March C-	$10n$	2/6	4/8	4/8	0/8
2P-PMOVI	$13n$	4/6	4/8	8/8	0/8
MMCA	$10n$	0/6	0/8	0/8	4/8
WIPD	$7n$	0/6	0/8	0/8	0/8
March s2PF-	$14n$	6/6	8/8	8/8	0/8
March d2PF-	$9n$	0/6	0/8	0/8	8/8

4.2 Industrial evaluation of the tests

In order to determine the importance of each functional model, their probabilities of occurrence have been calculated using two approaches [10, 11]: first by assuming that all resistive defects are equal likely (D E.L.) to occur; next, by using IFA. IFA has been performed for the two different dual-port cache layouts, say C1 and C2, with sizes of 32Kbits and 64 Kbits, respectively. They implement the same electrical memory circuit; i.e., a differential 2P SRAM.

Table 3: Fault probabilities

Class	Subclass	D E.L.	IFA C1	IFA C2
1PFs	1PF1	59.372	81.256	87.109
	2PF2	24.456	13.153	11.504
2PF2s	2PF1	2.498	4.483	1.292
	$2PF2_a$	2.234	0.000	0.010
	$2PF2_v$	0.749	0.002	0.085
	$2PF2_{av}$	10.691	1.106	0.000

Table 3 summarizes the fault probabilities [10, 11]; it clearly shows that the probability of occurrence of faults is layout dependent. A fault which is not realistic for a certain layout, can have a considerable probability for another one; e.g., the $2PF2_{av}$ has a probability of 1.106% for C1 and of 0% for C2. Therefore, one has to take all faults into consideration in order to obtain a very high fault coverage. Note that for C1, 94.409% of the faults are 1PFs and 5.591% are 2PFs; while for C2, 1.387% of the faults are 2PFs (i.e., $\simeq$ 4 times smaller than 2PFs for C1).

In an experiment, similar versions of the tests of Table 2 have been been implemented at Intel. The tests have been applied to dual-port memory dices (with C1 layout as well as with C2 layout) as follows:

- Step 1. Apply all single-port tests.
- Step 2. Apply 2P-Scan, 2P-March C-, 2P-PMOVI, MMCA and WIPD.
- Step 3. Apply March s2PF- and March d2PF-.

If the dices fail to pass Step 1 (i.e, single-port tests), then they will be not further tested in Step 2 and Step 3; and if they pass Step 1 and fail in Step 2, then they will not tested in Step 3. That means that March s2PF- and March d2PF- are applied to dices that pass all single-port tests and all conventional dual-port tests considered here.

The test results show that from 33830 C1 dices passing all tests of Step 1 and Step 2, 23 fail to pass March s2PF- and/or March d2PF- of Step 3: 7 fail to pass March s2PF-, and 21 fail to pass March d2PF-; note that 5 dices fail to pass both tests. That means that the tests detect 0.0678% of the dices passing all step 1 and step 2 tests; which corresponds with a level of 680 Defects per Million (DPM). Moreover, the test results show that from 2165868 C2 dices passing all tests of step 1 and 2, 305 fail to pass March s2PF- and/or March d2PF-; which corresponds with a level of 141 DPM. (that is $\simeq$ 4.8 times smaller than the DPM level for C1). It is interesting to note that the fault coverage of the 2P tests for C1 and C2 is proportional with the probabilities of occurrence of 2PFs, as predicted by IFA (with an accuracy of about 83%).

The analytical and the industrial evaluation of the discussed dual-port tests in this paper show clearly the superiority of March s2PF- and March d2PF-.

5 Conclusions

In this paper, a brief overview of realistic fault models for two-port memories has been presented. They

are divided into conventional single-port faults (1PFs) and unique two-port faults (2PFs), which require special tests. Thereafter, two optimal linear tests, March s2PF- and March d2PF-, to detect all targeted 2PFs have been derived. March s2PF- is a *single-addressing* test, with a test length of $14n$, to detect single-addressing 2PFs; i.e., faults which require the access of a single address (i.e., cell) via the two ports simultaneously in order to be sensitized. On the other hand, March d2PF- is a *double-addressing* test, with a test length of $9n$, to target double-addressing 2PFs; i.e., faults which require the access of two different addresses (i.e., locations) via the two ports simultaneously in order to be sensitized.

March s2PF- and March d2PF- have been evaluated analytically as well as industrially, together with other dual-ports tests, including those based on single port tests (like dual-port March C-) and other ones designed specificly for dual-port memories. Both evaluations show the superiority of March s2PF- and March d2PF- regarding the considered unique 2PFs.

The test results show that March s2PF- and d2PF- detect unique DPM that can not be detected with dual-port tests based on single-port tests, neither with other tests designed specific for dual-port memories like MMCA and WIPD [18]. The unique DPM was measured at 680 for one design and at 141 for another one. This makes March s2PF- and March d2PF- very attractive industrially; i.e., essential for any dual-ported array of significant size or area.

Acknowledgment

We express our gratitude to David Eastwick, Mike Spica, Scott Murray, Chris Sine, and Greg Tollefson from Intel corporation for providing extensive information regarding the tools as well as the SRAM designs. We also thank them for their helpful comments and suggestions.

References

[1] M.S. Abadir and J.K. Reghbati, "Functional Testing of Semiconductor Random Access Memories", *ACM Computer Surveys*, 15(3), pp. 175-198, 1983.

[2] R.D. Adams and E.S. Cooley, "Analysis of a Deceptive Read Destructive Memory Fault Model and Recommended Testing", *In Proc. IEEE North Atlantic Test Workshop*, 1996.

[3] V.C. Alves and M. Nicolaidis, "Detecting Complex Coupling Faults in Multi-Port RAMs", *IMAG Research Report No. RR978,* Feb. 1991.

[4] J.H. De Jonge and A.J. Smeulders, "Moving Inversions Test Pattern is Thorough, Yet Speedy", *In Comp. Design*, pp. 169-173, 1976.

[5] R. Dekker, F. Beenker, and H. Tijssen, "A Realistic Fault Models and Test Algorithms for Static random Access Memories", *IEEE Transactions on Computer-Aided Design,* Vol. 9, No. 6, pp. 567-572, June 1990.

[6] S. Hamdioui, and A.J. van de Goor, "Consequences of Port Restrictions on Testing Two-Port Memories", *In Proc. of International Test Conference ITC'98*, Washington, USA, pp. 63-72, Oct. 1998.

[7] S. Hamdioui, and A.J. van de Goor, "Port Interference Faults in Two-Port Memories", *In Proc. of International Test Conference ITC'99*, NJ, USA, pp. 1001-1010, Sep. 1999.

[8] S. Hamdioui, A.J. van de Goor, M. Rodgers, and D. Eastwick, "March Tests for Realistic Faults in Two-Port Memories", *Records of the IEEE Int. Workshop on Memory Technology, Design and Testing*, San Jose, CA., pp. 73-78., 2000.

[9] S. Hamdioui, A.J. van de Goor, M. Rodgers, and D. Eastwick, "Realistic Faults Models and Test Procedure for Multi-Port SRAMs", *Records of the IEEE Int. Workshop on Memory Technology, Design and Testing*, San Jose, CA., pp. 65-72, 2001.

[10] S. Hamdioui, A.J. van de Goor, M. Rodgers, and D. Eastwick, "Impact of Spot Defects on Fault Modeling and Tests in Dual-Port Memories", *In Proc. of the IEEE European Test Workshop*, pp. 19-21, 2001.

[11] S. Hamdioui, "Testing Multi-Port Memories: Theory and Practice", *PhD Thesis*, Delft University of Technology, Faculty of Information Technology and Systems, Section of Computer Engineering, Delft, The Netherlands, 2001.

[12] S. Hamdioui, and A.J. van de Goor, "An Experimental Analysis of Spot Defects in SRAMs: Realistic Fault Models and Tests", *In Proc. of the Ninth Asian Test Symposium*, pp. 131-138, Taipei, Taiwan, 2000.

[13] M. Marinescu, "Simple and Efficient Algorithms for Functional RAM Testing", *In Proc. of Int. Test Conference*, pp. 236-239, 1982.

[14] B. Nadeau-Dostie, A. Sulburt and V.K. Agrawal, "Serial Interfacing for Embedded Memory Testing", *IEEE Design and Test of Computers,* **7**(2), pp. 52-63, 1990.

[15] M. Nicolaidis, V.C. Alves and H. Bederr, "Testing Complex Coupling Faults in Multi-Port Memories", *IEEE Transactions on VLSI Systems,* **3**(1), pp. 59-71, March 1995.

[16] M.J. Raposa, "Dual Port Static RAM Testing", *In Proc. IEEE International Test Conference,* pp. 362-368, 1988.

[17] A.J. van de Goor, and S. Hamdioui, "Fault Models and Tests for Two-Port Memories", *In Proc. of* 16th *IEEE VLSI Test Symposium*, pp. 401-410, Monterey, CA., USA, April 1998.

[18] J. Zhao, S. Irrinki, M. Puri, and F. Lombardi, "Detection of Inter-Port Faults in Multi-Port Static RAMs", *In Proc. of VLSI Test Symposium*, Montreal, Canada, pp. 297-302, 2000.

[19] A.J. van de Goor, et al, "March LR: Test for Realistic Linked Faults, *In Proc. of* 14th *IEEE VLSI Test Symposium*, Princeton, NJ, pp. 272-280, April 28- May 1, 1996.

[20] A.J. van de Goor, "Testing Semiconductor Memories, Theory and Practice", *ComTex Publishing, Gouda, The Netherlands*, 1998. Web: http://ce.et.tudelft.nl/˜ vdgoor