Modeling Techniques and Tests for Partial Faults in Memory Devices

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Abstract: *It has always been assumed that fault models in memories are sufficiently precise for specifying the faulty behavior. This means that, given a fault model, it should be possible to construct a test that ensures detecting the modeled fault. This paper shows that some faults, called partial faults, are particularly difficult to detect. For these faults, more operations are required to complete their fault effect and to ensure detection. The paper also presents fault analysis results, based on defect injection and simulation, where partial faults have been observed. The impact of partial faults on testing is discussed and a test to detect these partial faults is given.*

Key words: *partial faults, DRAMs, fault models, defect simulation, memory testing, completing operations.*

1 Introduction

In order to test memory devices for possible faults, deviations from the expected memory behavior are modeled using what is called *functional fault models (FFMs)*. FFMs are used to describe the faulty behavior of the memory in a way that reduces the complexity of the faulty behavior and limits attention to those behavioral deviations that are important from a testing point of view.

FFMs are composed as sets of *fault primitives (FPs)* [vdGoor00]. FPs are defined as $<S/F/R>$, where S stands for the *sensitizing operation sequence (SOS)*, F for the state of the faulty cell and R for the output on a read operation. In this paper, we restrict ourselves to single-cell faults with at most one operation. This implies that $S \in \{0, 1, 0w0, 0w1, 1w0, 0r0, 1r1\}$, where, for example, the 0 in $0w1$ represents the initial value of the cell before the $w1$ is applied. $F \in \{0, 1\}$, and $R \in \{0, 1, -\}$, where $-$ denotes the fact that the SOS does not end with a read operation to the victim. For example, the FP $<0w1/0/->$ represents the up-transition fault (TF↑). $S = 0w1$ denotes that the cell contains the value 0, after which a $w1$ operation is applied to perform an up-transition in the cell. $F = 0$ means that the cell remains in state 0, and $R = -$ means that there is no read result on the output since S does not apply a read operation to the victim.

This paper shows that some FPs depend on the initial voltages within the memory. It is shown that the voltages in a defective memory are not always normalized by precharging at the beginning of every memory operation, but remain floating to some extent. As a result of these floating voltages, memory operations may only partially sensitize the faulty behavior and need extra operations to ensure that the fault is always sensitized. Partially sensitized faults are called *partial faults*, their SOSes are called *partial SOSes*, and the extra operations needed to ensure sensitizing partial faults are called *completing operations*.

As an example of partial faults, consider Figure 1 where an open defect with resistance R_{def} is present on the bit line (BL) of a DRAM, between the memory cell and the precharge devices, dividing BL into two parts: BLa and BLb. The open prevents proper precharging of BL at the beginning of every operation, which results in improper memory functionality that is particularly difficult to sensitize and detect. For high values of R_{def} and with an initial 0 volts on BLb (from a previous write 0 operation, for instance), the memory would be unable to properly precharge BLb which prevents sensing a stored 1 in the cell. Therefore, the sense amplifier senses a 0 in the cell and the restore cycle replaces the stored 1 with a stored 0. This type of faulty behavior is known as a read destructive fault (RDF_1) [Adams96] which is represented as $<1r1/0/0>$ in the FP notation.

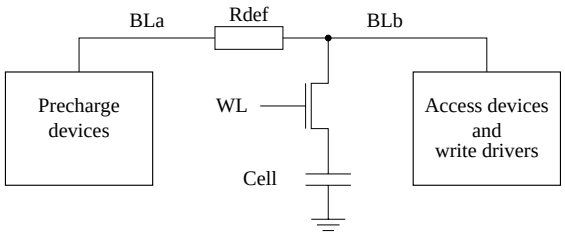

Figure 1. Bit line with an open between cell and precharge devices.

Describing the faulty behavior by the FP $<1r1/0/0>$ implies that it should be possible to sensitize and detect this faulty behavior using the march test $\{\Updownarrow(w1, r1)\}$ [vdGoor98]. Supposedly, this test would initialize the faulty cell to 1, then a following read would sensitize and

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detect the fault as indicated by the FP. However, this is not the case in our example. Performing the $w1$ on the defective memory of Figure 1 results not only in initializing the cell to 1, but also in preconditioning the voltage on BLb to a high voltage. Performing a subsequent $r1$ detects the proper stored 1 and forwards it to the output. The condition needed to sensitize the faulty behavior is to pull down the voltage on BLb *after* the $w1$ and *before* the $r1$ operation. This can be achieved by performing a *completing* $w0$ *operation* to a cell on the same BL of the faulty cell. The completing $w0$ operation completes the fault effect from partial to full and is shown in square brackets in the fault $<1_v[w0_{BL}]\ r1_v/0/0>$. Note that the $w0$ operation has ***BL*** as subscript, which means that the operation should be performed to any cell on the same BL as the victim cell (denoted by the subscript v).

This paper starts with a description of possible causes of partial faults in Section 2. Then, Section 3 gives ways to be used in fault analysis to identify partial faults. Section 4 discusses some properties of partial faults. Section 5 presents the results of the fault analysis performed on a DRAM using defect injection and simulation where partial faults have been observed. Finally, Section 6 ends with the conclusions.

2 Causes of partial faults

Partial faults take place when an operation in a defective memory fails because the preceding operation fails to leave the memory in its proper state (i.e., the operation did not set the different signal lines to their proper voltages). In order to inspect the faulty behavior for possible partial faults, it is important to know the floating signal lines that result from a given defect in the memory. Three classes of defects are usually considered when memory fault analysis is performed: opens, shorts and bridges. The discussion in this paper is limited to opens, which represent resistive elements inserted on a signal line. Opens restrict current flow through the memory and result in floating voltages. Shorts and bridges are not expected to result in partial faults since they do not restrict current flow and do not result in floating voltages.

These floating signal lines that result from memory opens depend on the specific design of the memory under analysis. In this paper, we will describe the floating signal lines and the opens based on the DRAM design shown in Figure 2. The relation between specific floating voltages and inserted opens is described next.

Open 1: This open is in the memory cells, which leads to floating voltages in the defective cell and prevents the proper setting of stored voltages to a strong 1 or 0. When simulating the memory for faulty behavior by performing fault analysis of this defect, the analysis should include modifying the stored voltage within the defective cell.

Open 2: This open is in the reference cells, which results in an improper setting of the voltage within the reference cells. Fault analysis of this defect should include modifying the stored voltage within the reference cell.

Open 3 & 4 These opens prevent proper precharging of the BLs at the beginning of each operation, which results in floating BL voltages. In this case, fault analysis should consider modifying the floating BL voltage at the beginning of each operation.

Open 5: This open prevents precharging of the BL part on the right side of the defect, while isolating the BL part on the left side from sensing and writing. This results in floating BL voltages, in addition to floating cell voltages. Analyzing this defect should consider modifying BL and cell voltages.

Open 6: This open prevents BL precharging and proper cell sensing and writing. It also prevents proper setting of reference cell voltages since they depend on the proper functionality of the sense amplifier. Fault analysis of this defect should include modifying BL and cell voltages, in addition to reference cell voltages.

Open 7: This open prevents proper sensing of memory cells. This results in floating voltages within memory cells and reference cells when read operations are performed. Moreover, the inability of proper sensing results in improper operation of the read output buffer. Therefore, the analysis of this defect should consider modifying memory cell and reference cell voltages, in addition to the state of the output buffer.

Open 8: This open results in floating BL voltages, improper memory cell writing and improper forwarding of the sensed memory cell state to the output buffer. Analyzing this defect should include modification of BL voltages, memory cell voltages and the state of the output buffer.

Open 9: This open disconnects the pass transistor of the cell from the word line (WL). This results in floating WL voltages and floating cell voltages. Analyzing this defect should include modification to WL and memory cell voltages.

3 Identifying partial faults

This section shows a fault analysis method that makes it possible to identify partial faults. Consider the example shown in Figure 1 which shows a BL open between the memory cells and the precharge devices (also shown as Open 4 in Figure 2). According to the rules described in Section 2, the fault analysis should consider modifying the BL voltage. The results for this type of fault analysis are represented as FP regions in the (R_{def}, U_{init}) plane,

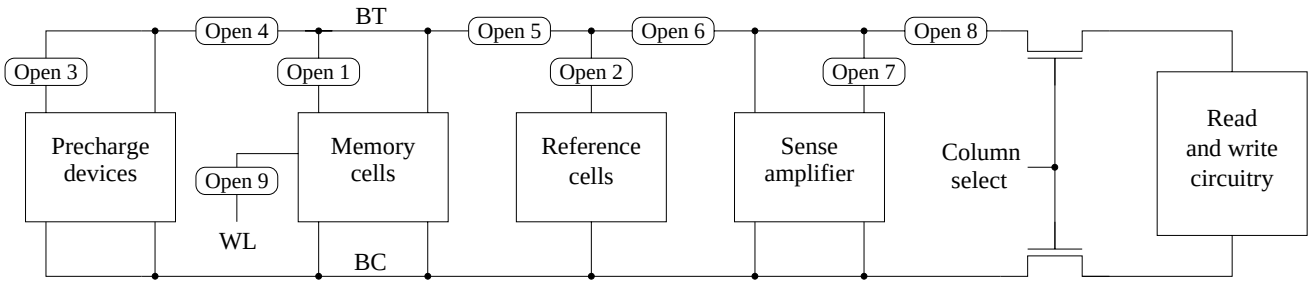

Figure 2. Open defects on a DRAM cell array column causing floating voltages.

as shown in Figure 3(a) [Al-Ars99]. The figure shows the value of the open defect resistance (R_{def}) versus the initial voltage (U_{init}) on the floating BL part. The only FP observed in the figure is RDF_1, which indicates a failing $r1$ operation ($<1r1/0/0>$).

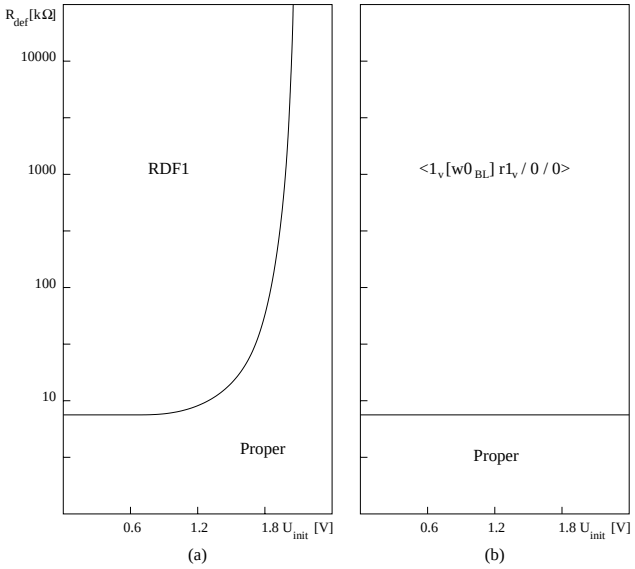

Figure 3. Analysis results of a bit line open in the (R_{def}, U_{init}) plane applying (a) $S = 1r1$ and (b) $S = 1_v[w0_{BL}]r1_v$.

In order to identify partial faults, the faulty behavior should be inspected for changes as the floating BL voltage is modified. It is clear in the figure that the observed RDF_1 is only present for low voltages of the floating BL. Above a BL voltage of about 2 V, no fault can be observed. This means that the floating BL voltage plays a significant role in the observation of this fault, and in order to ensure that the fault is sensitized and detected, the BL should be kept at a low voltage when the $r1$ operation is performed. As discussed in the introduction, this can be achieved by performing a completing $w0$ operation to a different cell on the same BL before performing the $r1$, resulting in the fault $<1_v[w0_{BL}]\ r1_v/0/0>$.

Figure 3(b) shows the fault analysis results in the (R_{def}, U_{init}) plane when performing the SOS $1_v[w0_{BL}]r1_v$. The figure shows that the resulting faulty behavior does not depend anymore on the floating BL voltage. The faulty behavior can now be sensitized for any initial BL voltage.

The following general rule helps identify partial faults in the performed fault analysis. Assume that a given memory defect results in a floating voltage V_f on some signal line in the memory. Assume further that the defect results in observing the fault FP_1.

> If FP_1 is only observed for a limited range of V_f values, then completing operations should be added to FP_1 to ensure it is sensitized.

As a second example of partial faults, consider the faulty behavior resulting from an open within the memory cell (Open 1 in Figure 2). According to the rules described in Section 2, the fault analysis should consider modifying the voltage of the defective cell. The results of this type of fault analysis are represented as FP regions in the (R_{def}, U_{init}) plane, as shown in Figure 4(a). The figure shows the value of the open defect resistance (R_{def}) versus the initial voltage (U_{init}) within the defective cell. For reasons of clarity, the shown results are simplified and truncated to show the fault region of interest only. The actual unsimplified results can be found in the literature [Al-Ars01a]. The FP region shown in the figure is RDF_0, which indicates a failing $r0$ operation ($<0r0/1/1>$).

The figure shows that RDF_0 is present for a larger range of R_{def} values when the floating cell voltage is high. The fault can be sensitized with R_{def} values as low as 150 kΩ for an initial cell voltage of 1.6 V. When U_{init} is decreased to 0 V, the fault can only be sensitized with R_{def} values above 300 kΩ. As a result, if the cell has a defect with 150 kΩ $< R_{def} <$ 300 kΩ then it can only be sensitized when $U_{init} \approx 1.6$ V. In order to ensure sensitizing this fault, the cell voltage should be kept at approximately 1.6 V when the $r0$ is performed. Simulations have shown that this can be achieved by performing the completing opera-

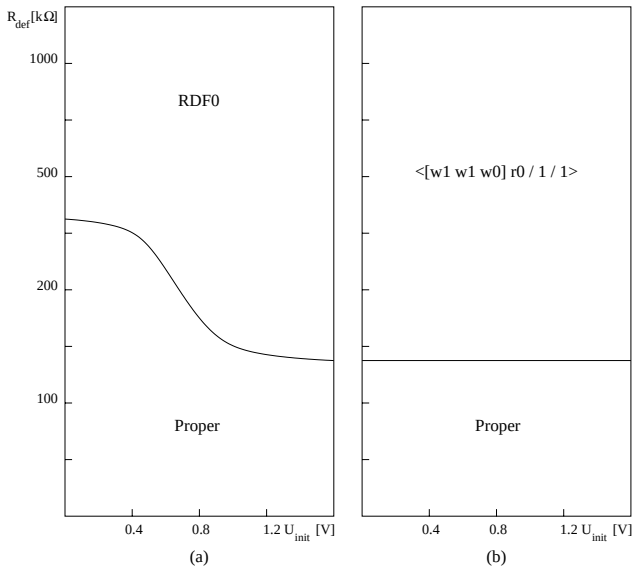

Figure 4. Analysis results of a cell open in the (R_{def}, U_{init}) plane applying (a) $S = 0r0$ and (b) $S = [w1w1w0]r0$.

tions $[w1\ w1\ w0]$ before performing the $r0$, resulting in the fault $<[w1\ w1\ w0]\ r0/1/1>$.

Figure 4(b) shows the fault analysis results in the (R_{def}, U_{init}) plane when performing the SOS $[w1\ w1\ w0]$ $r0$. The figure shows that the resulting faulty behavior is not any more dependent on the floating cell voltage, but can now be sensitized with $R_{def} = 150$ kΩ for any initial cell voltage. This is also reflected in the SOS itself by dropping the 0 initialization of the cell since the SOS constitutes sufficient initialization to sensitize the fault.

4 Properties of partial faults

Fault models can be classified according to their SOS, either with respect to the number of different cells accessed ($\#C$) or the number of performed operations ($\#O$). For example, if the SOS is $0_a0_vw1_ar1_ar0_v$ then $\#C = 2$, since two different cells (cell a and cell v) are accessed by this sequence. On the other hand, $\#O = 3$ for this SOS since cell v is accessed once and cell a is accessed twice.

It is possible to use the definitions of $\#C$ and $\#O$ to derive relations between partial and the resulting completed faults. First, note that the task of the completing operations included in partial faults is to set the initial memory voltages in such a way that would always enable sensitizing a fault. Now assume that a memory defect results in the floating memory voltage V_f, and results in a minimized partial FP$_p$ (with $\#C_p$ and $\#O_p$) that is observed for a limited voltage range of V_f. As a result, if a set of completing operations could be found resulting in a completed FP$_c$ (with $\#C_c$ and $\#O_c$) to sensitize the partial FP for all V_f values, then one of the following relations is correct:

1. $\#C_c \geq \#C_p$
2. $\#O_c \geq \#O_p$
3. $\#C_c \geq \#C_p$ and $\#O_c \geq \#O_p$

For example, Open 4 of Figure 2 results in the partial fault RDF$_1$ (with $\#C_p = 1$ and $\#O_p = 1$), as shown in Figure 3(a). Completing operations used to sensitize this faulty behavior for every initial BL voltage result in FP$_c$ = $<1_v\ [w0_{BL}]\ r1_v/0/0>$ with $\#C_c = 2$ and $\#O_c = 2$, which satisfies Relation 3.

These relations indicate that a completed fault has at least as many cell initializations and/or operations as its partial counterpart. As a result, a test constructed to sensitize and detect a completed fault is expected to have a higher complexity than a test for its partial counterpart.

These relations also show that completed FPs can also be considered as regular FPs if a fault analysis is performed using FPs with at least $\#C_c$ and $\#O_c$. Yet, any increase in $\#C$ or $\#O$ translates into an exponential increase in the number of analyzed FPs, which in turn exponentially increases the fault analysis effort. This can be clearly seen in the following relation for the number of single-cell FPs ($\#C = 1$) as a function of $\#O$ [Al-Ars99]:

$$\#\text{ single-cell FPs} = \begin{cases} 2 & : \#O = 0 \\ 10 \cdot 3^{(\#O-1)} & : \#O \geq 1 \end{cases}$$

So for example, the fault analysis results in Figure 4(a) of Open 2 in Figure 2 has been performed using $\#C = 1$ and $\#O = 0$ and 1, which means that $2 + 10 \cdot 3^0 = 12$ FPs have been analyzed. The corresponding completed fault has $\#C = 1$ and $\#O = 4$, which means that it requires analyzing $2+10+90+270 = 372$ FPs to be found through straight-forward fault analysis and without the use of the concept of partial faults.

In conclusion, identifying partial faults represents a new fault analysis method that helps performing *directed* or *smart* analysis using higher order FPs without the need to inspect the faulty behavior for each of these FPs.

5 Fault analysis results

A fault analysis has been performed on a DRAM using defect injection and SPICE electrical simulation to establish the notion of partial faults [Al-Ars99]. The DRAM used in the analysis has the structure shown in Figure 2, and it is modeled based on a 0.35 μm technology. A number of opens have been injected into the DRAM model, and for each open, specific floating memory voltages have been

initialized to a number of different values during the analysis. Because of analysis complexity, only the following subset of the floating voltages described in Section 2 have been analyzed through simulation:"

- Open 1 in memory cell: floating voltage within cell
- Open 2 in reference cell: not simulated
- Open 3 in precharge circuits: floating voltage on BL
- Opens 4, 5 & 6 on bit line: floating voltage on BL
- Open 7 in sense amplifier: floating reference cell voltage and state of output buffer
- Open 8 on BL: floating BL voltage and state of output buffer
- Open 9 on word line: floating word line voltage

The results show that partial faults do take place with most of the analyzed defects. Table 1 summarizes the results acquired from the fault analysis process on all simulated defects. The column "Sim. FFM" lists the partial faults observed in the electrical simulation of the defects. The column "Com. FFM" lists the partial faults that would result from simulating the complementary defects [Al-Ars00]. The column "Initialized volt." indicates the signal voltage that results in the partial faults.

Table 1. Partial faults observed in DRAM simulation.

FFM		Open	Completed FP	Initialized volt.
Sim.	Com.			
RDF_0	RDF_1	Open 1	$<[w1\ w1\ w0]\ r0/1/1>$	Memory cell
		Open 5	$<0_v\ [w1_{BL}]\ r0_v/1/1>$	Bit line
		Open 8	$<0_v\ [w1_{BL}]\ r0_v/1/1>$	Output buffer
RDF_1	RDF_0	Open 3 – 5	$<1_v\ [w0_{BL}]\ r1_v/0/0>$	Bit line
		Open 8	$<1_v\ [w0_{BL}]\ r1_v/0/0>$	Output buffer
		Open 7	$<1_v\ [w0_{BL}]\ r1_v/0/0>$	Reference cell
$DRDF_1$	$DRDF_0$	Open 4	$<1_v\ [w1_{BL}]\ r1_v/0/1>$	Bit line
IRF_0	IRF_1	Open 8	$<0_v\ [w1_{BL}]\ r0_v/0/1>$	Output buffer
		Open 9	Not possible	Word line
IRF_1	IRF_0	Open 5	$<1_v\ [w0_{BL}]\ r1_v/1/0>$	Bit line
WDF_1	WDF_0	Open 4	$<1_v\ [w0_{BL}]\ w1_v/0/->$	Bit line
TF↑	TF↓	Open 1	Not possible	Memory cell
TF↓	TF↑	Open 5	$<1_v\ [w1_{BL}]\ w0_v/1/->$	Bit line
		Open 9	Not possible	Word line
SF_0	SF_1	Open 9	Not possible	Word line

It is interesting to note that some partial faults cannot be initialized using memory operations to ensure they are sensitized. The "Completed FP" entry of these faults is listed in the table as "Not possible", since there is no SOS that ensures sensitizing these faults for any initial voltage. An example of these faults is the state fault (SF_0) resulting from an open on the WL. When the floating WL voltage is high, the cell becomes connected to the BL and gets charged up during the BL precharge cycle. This fault does not take place when the floating WL voltage is low (cell is disconnected from the BL). Since it is not possible to manipulate floating WLs by memory operations, it is also not possible to ensure the sensitizing these faults for all initial floating voltages.

The table shows that all simulated FPs can become partial for some memory defect. In addition, it is possible to use completing operations to ensure sensitizing all types of partial faults, with the exception of state faults SF_0 and SF_1. Yet, there is no theoretical reason why this should not be possible for some partial state faults. Also note that all modified initial voltages result in at least one partial fault. Furthermore, there is no rule for generating the completing operations needed to sensitize partial faults.

Using the completed FPs listed in the table, a test may be constructed that ensures detecting all partial FPs we are able to detect. The following march test, March PF, ensures detecting both simulated and complementary partial FPs [Al-Ars01b]: $\{\Updownarrow(w0,\ w1);\ \Updownarrow(r1,\ w1,\ w0,\ w0,\ w1,\ r1);\ \Updownarrow(w1,\ w0);\ \Updownarrow(r0,\ w0,\ w1,\ w1,\ w0,\ r0)\}$.

6 Conclusions

This paper introduced the notion of partial faults, where floating memory voltages due to a defect may prevent sensitizing a given fault. The paper discussed the reasons such faults may take place and described a fault analysis method that helps identify these faults. The paper also presented fault analysis results, based on defect injection and simulation, where partial faults have been observed. The impact of partial faults on testing was discussed and a test to detect them was given.

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