NBTI-Aware Nanoscaled Circuit Delay Assessment and Mitigation

Seyab Khan Said Hamdioui

Delft University of Technology, Computer Engineering Laboratory
Mekelweg 4, 2628 CD, Delft, The Netherlands
{M.S.K.Seyab, S.Hamdioui}@tudelft.nl

Abstract. As semiconductor manufacturing entered into nanoscale era, performance degradation due to Negative Bias Temperature Instability (NBTI) became one of the major threats to circuits reliability. In this paper, we present a model and analysis of NBTI impact on circuit delays. First, we model NBTI impact on gate intrinsic delay and output transition delay. The insights of our models reveal that NBTI causes additional 6.7% intrinsic and 3% output transition delays to a gate. Second, we analyze delays in the gates at the inputs and outputs of a circuit. Simulation results from several benchmark circuits show that under a given condition identical gates at the circuit outputs suffer from 3.33% additional delays as compared to gates at the circuit inputs. Third, we analyze different techniques at transistor and circuit levels to mitigate NBTI. From the analysis of mobility increment, gate oversizing, temperature reduction, and supply voltage increment techniques, we conclude that temperature reduction is the most effective to mitigate NBTI.
Keywords: Negative Bias Temperature Instability, Intrinsic delay, Front-end delay, NBTI mitigation.

1 Introduction

With the relentless pursuit for smaller CMOS process technologies, failures due to aging mechanisms have become a limiting factor for transistor/circuit reliability [1]. Industrial data reveal that as oxide thickness reached 4nm, Negative Bias Temperature Instability (NBTI) has become one of the most significant aging mechanisms [2, 3]. NBTI degrades performance of a PMOS transistor under a negative gate stress. The effects of NBTI on a PMOS transistor include: (a) threshold voltage increment, (b) drain current degradation, and (c) delay increment [4, 5]. These effects show off themselves at circuit level by increasing circuit delays, or in extreme cases causing circuit timing/functional failures.

The delay due to NBTI is a growing problem for nanoscaled gates and circuits. The amount of delay depends on variables such as temperature, voltage and switching activities of transistors. Therefore, an accurate estimation of the delay is a tremendous challenge. In the work done so far, the delay due to NBTI is modeled in two distinct ways:

- Gate delay modeling [6–8]: in which NBTI impact on delays of individual gates are calculated. The delay models are generally derived analytically or constructed from circuit simulations.
- Circuit delay modeling [7, 10]: in which gate delays of *individual isolated gate* are lumped to get circuit delay models.

There are few research works on NBTI induced delay modeling at gate level [6–8]. Paul et al. in [6] initiated NBTI delay modeling and analysis. However,

the analysis is pessimistic as they consider only the worst case, i.e. static stress conditions. In [7] NBTI impact on gate delay have been analyzed under dynamic stress conditions. However, the analysis focuses on the NBTI induced delay of the isolated gate and does not consider its impact on the gate output transition that affects input transition to the next gates in the circuit. In [9] it has been argued that variations in input transition can cause up to 31% additional delay to a gate. Therefore, NBTI impact on the output transition must be incorporated in the gate delay models.

Apart from the above mentioned initial works at gate level delay modeling, circuit level delay modeling due to NBTI is still at its infancy stage and demands more attention from the research community. The circuit delay models proposed so far [7, 10] suffer from inaccuracy as they only consider NBTI impact on intrinsic delays of the gates. These models ignore the impact on the gate input transition. NBTI affects the input transition of a gate due to degradation of the previous gates in a circuit. Therefore, an accurate gate level NBTI model suitable for circuit delay assessment is needed.

In this paper, we present a novel NBTI aware circuit delay model, which embodies transistor level NBTI induced degradation, gate level delay and circuit level delay. Thereafter, we analyze different techniques to mitigate NBTI at transistor and circuit levels. The contributions of this paper are the following.

- It models gate the intrinsic delay increment due to NBTI induced threshold voltage shift. Magnitude of the delay is a function of supply voltage, temperature and switching activity of the gate.
- It models NBTI impact on the output transition of a gate. Furthermore, it models the impact of the input transition on the gate delay.
- It presents NBTI induced circuit delay modeling and analysis; magnitude of the delay depends on the switching activities, types of the gates and nature of the correlation among the gates.
- It analyzes different techniques to mitigate NBTI at transistor and circuit levels. The analysis reveals that at circuit level, temperature reduction is the most suitable technique to mitigate NBTI.

The rest of the paper is organized as follows. Section 2 describes NBTI mechanism under dynamic stress. Section 3 proposes an NBTI induced gate delay model; the model considers NBTI impact on intrinsic delay and output transition of a gate. Section 4 extends the gate delay model to model circuit delay due to NBTI. Section 5 discusses simulation results of several benchmark circuits. Section 6 analyzes different techniques to mitigate NBTI. Finally, Section 7 concludes the paper.

2 NBTI Mechanism

The Reaction-Diffusion (R-D) model [11] has been widely used to explain NBTI mechanism of PMOS transistors. The model can be divided in two phases i.e. stress and recovery phases.

Stress Phase: According to the model, during stress phase (V_{gs}=-V_{dd}), NBTI degradation originates from Silicon Hydrogen bonds (≡Si-H) breaking at Silicon-Silicon dioxide (Si-SiO_2) interface of a PMOS transistor as shown in Fig.1(a). The broken Silicon bonds (≡Si-) act as interface traps that cause NBTI degradation. The number of interface traps (N_{IT}) depends on ≡Si-H bond breaking

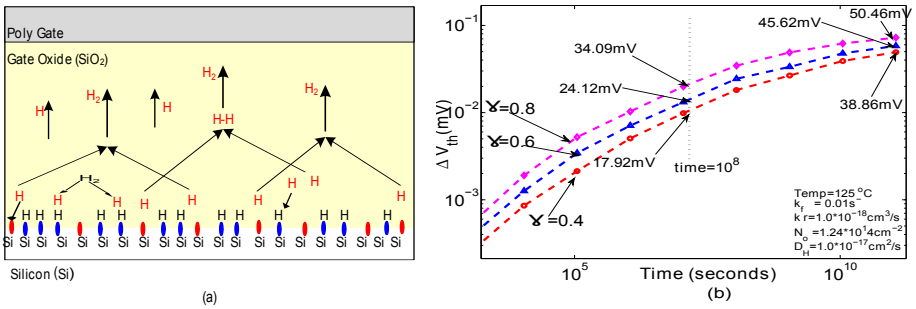

Fig. 1. (a) Schematic view of NBTI mechanism (b) V_{th} with time for various γ values

rate (k_f) and ≡Si- bond recovery rate (k_r). The N_{IT} generation rate is given by [4]:

$$\frac{dN_{IT}}{dt} = k_f(N_o - N_{IT}) - k_r N_{IT} N_H^0 \tag{1}$$

where N_o and N_H^0 denote initial bond density and atomic Hydrogen density at the Si-SiO_2 interface respectively. The H atoms released from ≡Si-H bond breaking contribute to three sub-processes including: (a) diffusion towards the gate, (b) combination with other H atoms to produce H_2, or (c) recovery of the broken bonds. Similar to H atoms, H_2 molecules participate two sub-processes: (a) diffusion towards gate, and (b) dissociation to produce H atoms. All these sub-processes are schematically shown in Fig.1(a). The N_{IT} generation rate is limited by the sub-processes related to H and H_2 and is given by [4]:

$$\frac{dN_H}{dt} = D_H \frac{d^2 N_H}{dx^2} - k_H N_H^2 + k_{H_2} N_{H_2} \tag{2}$$

$$\frac{dN_{H2}}{dt} = D_{H2} \frac{d^2 N_{H2}}{dx^2} + \frac{1}{2} k_H N_H^2 - k_{H2} N_{H2} \tag{3}$$

where N_H and N_{H_2} are densities, D_H and D_{H_2} are diffusion rates of H and H_2, while k_H and k_{H_2} are interconversion rates of H and H_2 respectively.

Initially, the bond breaking and bond recovery sub-processes dominate at the Si-SiO_2 interface; the diffusing entities in SiO_2 layer are mainly atomic H. However, if the stress is maintained for longer time, most of the H atoms are converted to H_2, which in turn dominate the diffusion inside SiO_2 layer. Under such conditions N_{IT} at time t is obtained by solving Eq.1 and Eq.3 [4]:

$$N_{IT}(t) = \left(\frac{k_f N_o}{k_r}\right)^{2/3} \left(\frac{k_H}{k_{H_2}}\right)^{1/3} (6 D_{H2} t)^{1/6} \tag{4}$$

Recovery Phase: Once the gate stress is removed (i.e. V_{gs}=V_{dd}), the Si-H bond breaking at Si-SiO_2 interface no longer exists. Now the H and H_2 entities diffuse back and recover the interface traps. The recovered interface traps (N_{IT}*) can be written as [4]:

$$N_{IT}* = N_{IT}\left(1 - \sqrt{\frac{\xi . t}{t + t_o}}\right) \tag{5}$$

where ξ is the diffusion dependent recovery constant, t_o is the cycle duration, and t is the recovery duration. The equation shows that $N_{IT}*$ increases with t; and that at t=t_o, the recovered interface traps reach $N_{IT}*$=0.3×N_{IT} for ξ=1.

Eq. 4 and Eq. 5 give the generated N_{IT} and the recovered $N_{IT}*$ during stress

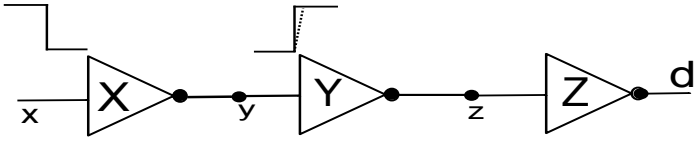

Fig. 2. An example circuit to illustrate NBTI impact on delays

and recovery phases respectively. N_{IT} causes threshold voltage shift (ΔV_{th}) of PMOS transistor, which can be written as:

$$\Delta V_{th} = (1+m)\frac{q.N_{IT}}{C_{ox}} \tag{6}$$

where m, q, and C_{ox} represent hole mobility degradation, electron charge and oxide capacitance of the transistor respectively. During recovery phase, $N_{IT}*$ presence means a reduction in N_{IT}. As a consequence, V_{th} shift will be reduced during the recovery phase.

The N_{IT} generated and the consequent ΔV_{th} strongly depend on stress and recovery durations ratio (γ) of transistor in a gate. Fig.1(b) shows the ΔV_{th} increment with time for different γ values. The figure shows that for a given γ, the ΔV_{th} increases with the stress time and intends to saturate at longer stress time. In addition, the analysis of data in the figure reveal that ΔV_{th} is linearly proportional to γ i.e.

$$\Delta V_{th} \propto \gamma \tag{7}$$

The relation is evident from the figure. For instance, at t=10^8sec, ΔV_{th} =17.92mV for γ=0.4, ΔV_{th}=24.12mV for γ=0.6, and ΔV_{th}=34.08mV for γ=0.8.

3 Proposed Gate Delay Model

Traditionally, the circuit delay due to NBTI is modeled in two phases: (a) the delay is modeled for an isolated gate, and (b) the isolated gate delays are added to get the circuit delay model [6, 10]. Clearly, the isolated gate delay model used is not accurate for circuit delay modeling since NBTI impact on gate delay in a circuit is not isolated. Instead, a gate delay model should account for the correlation between gates. The correlation exists because the output of one gate can be the input of the next gate in a circuit. NBTI increases the output transition of a gate to increases the input transition of the next gate and consequently its delay.

Fig.2 will be used to illustrate how ΔV_{th} of transistors in inverter Y and delay of inverter X influence the delay of inverter Y. Without considering aging, the delay of inverter Y is:

$$D = D_{th} + D_{st} + D_{cl} \tag{8}$$

where D_{th}, D_{st} and D_{cl} are delays due to transistor's V_{th}, input Signal Transition and Capacitive Load of the gate respectively. For simplicity, we assume that third term is not affected by aging. The first and second terms degrade with aging. Suppose a falling transition is applied to the input of inverter X. By considering aging, ΔV_{th} of transistors in X will increase output signal transition of the inverter X. As a consequence, this will cause an additional delay to the input signal transition of inverter Y. Obviously, aging will also cause an additional

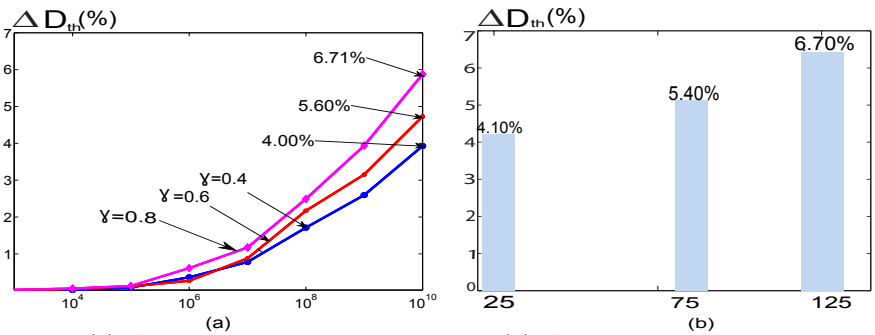

Fig. 3. (a) ΔD_{th} with time under different γ, (b) ΔD_{th} at different temperatures

delay due to ΔV_{th} of transistors in Y. Hence, the total additional delay of inverter Y due to aging is:

$$\Delta D = \Delta D_{th} + \Delta D_{st} \tag{9}$$

where ΔD_{th} and ΔD_{st} are the delays due to ΔV_{th} of transistors in Y and input delay respectively. Henceforth, we will refer to ΔD_{th} as *intrinsic delay* and ΔD_{st} as *Front-end delay*. It is important to note that for gates at the circuit inputs ΔD_{st}=0 and ΔD is only due to ΔD_{th}.

In the rest of the section, we develop a gate delay model due to NBTI; The model takes both intrinsic delay model and the front-end delay into consideration.

Intrinsic Delay Model: The nth power law model [12] offers a simple yet accurate empirical formulation of the gate intrinsic delay (ΔD_{th}). The ΔD_{th} dependence on V_{th} is given by:

$$D_{th} = \frac{A}{(V_g - V_{th})^n}$$

where V_g is the gate voltage, n is a constant, and A is a technology dependent constant. The delay due to NBTI induced ΔV_{th} can be obtained by taking the differential of the above equation w.r.t. V_{th}. Thereafter, applying Taylor series expansion and neglecting the higher order terms, the ΔD_{th} obtained is [6]:

$$\Delta D_{th} = \frac{n.\Delta V_{th}}{(V_{gs} - V_{th})} \tag{10}$$

In the above formulation, we introduce the variable γ of Eq.7. With this variable, we express the distribution of stress and recovery durations of the PMOS transistor in the gate. The stress/recovery distribution aware ΔD_{th} of the gate is given by:

$$\Delta D_{th} = \gamma.\frac{n.\Delta V_{th}}{(V_{gs} - V_{th})} \tag{11}$$

The equation shows that the ΔD_{th} is γ dependent. Additionally, it is important to point out here, that the ΔD_{th} varies with temperature due to ΔV_{th} dependence on temperature. The 45nm PMOS transistor model's [15] parameters are used to simulate ΔD_{th} of a gate. Fig.3 shows the gate ΔD_{th} for various γ and temperature values. The key insights from the figure are:

– NBTI induced ΔD_{th} increases with γ and follows the same trend as ΔV_{th} with γ. Figure 3(a) shows that the delay increment for γ=0.4 is 4.00%, while for γ=0.80 the increment approaches 6.71%.

– Temperature affects NBTI induced ΔV_{th} and hence the gate ΔD_{th}. Figure 3(b) shows the correlation between temperature and ΔD_{th}. The simulation is done for γ=0.8; the results show that ΔD_{th} is 4.10% at 25^{o}C, and 6.70% at 125^{o}C.

Front-end Delay Model: In order to complete our gate delay model suitable for circuit delay modeling, we model NBTI impact on output transition (τ_o) of a gate. It has been argued that at constant load capacitance (C_L) and supply voltage (V_{dd}), τ_o of a gate depends on the saturation drain current (I_{dsat}) of the active transistor (i.e. τ_o=$C_L.V_{dd}/I_{dsat}$) [13]; the I_{dsat} is given by:

$$I_{dsat} = \mu.B.(V_{gs} - V_{th})^n \tag{12}$$

where μ is the hole mobility and B is a technology dependent constant. NBTI increases V_{th}, reduces μ that results in lower I_{dsat} and hence increase τ_o of a gate. For an intermediate gate in a circuit, we assume that τ_o of the gate is equivalent to the input transition (τ_i) of the next gate (i.e. $\tau_0 = \tau_i$). For a given value of velocity saturation index (α) and voltage gain of the active transistors (ν_t) in a gate, we model the gate delay as a function of τ_i in accordance with [12]. Henceforth, we will call it front-end delay (D_{st}). After simplification, we conclude that the ΔD_{st} increases with τ_i, and can be written as:

$$D_{st} = \left(\frac{\alpha + \nu_t}{1 + \alpha}\right) \tau_i.\kappa \tag{13}$$

where κ is an indicator variable for delay propagation. If the input transition τ_i will cause a transition at the gate output its value is 1, otherwise it is zero. The increase in τ_i due to NBTI induced degradations of the previous gates and their impact on gate ΔD_{st} is achieved by solving Eq. 12 and Eq. 13. After simplification, the front-end delay is:

$$\Delta D_{st} = \left(\frac{\alpha + \nu_t}{1 + \alpha}\right) \Delta\tau_i.\kappa \tag{14}$$

To illustrate the front-end delay model we consider the circuit in Fig.2. We assume that inverter X suffers from NBTI, and Y does not have intrinsic delay and its delay is only affected by input transition. The 45nm PMOS transistor model's [15] parameters are used to simulate NBTI impact, (a) on τ_o of a inverter X, (b) on τ_i of inverter Y, and (c) on ΔD_{st} of inverter Y. Fig.4(a) shows NBTI impact on the τ_o of inverter X. The figure shows that τ_o of inverter X increases with time due to NBTI. τ_o increment of inverter X increases τ_i inverter

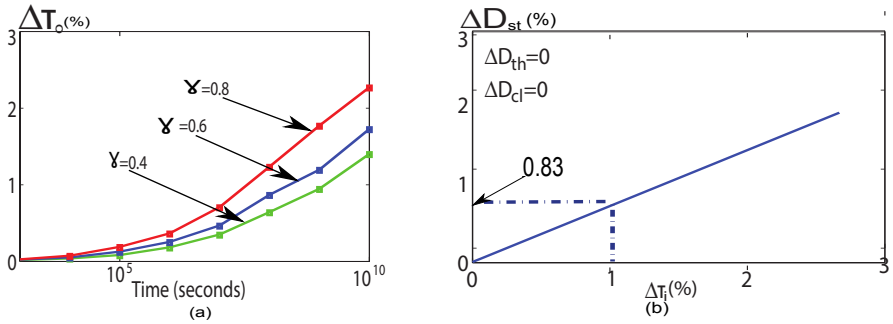

Fig. 4. (a) $\Delta\tau_o$ under NBTI degradation at γ=0.4, 0.6 and 0.8(b) ΔD_{st} variation with $\Delta\tau_i$

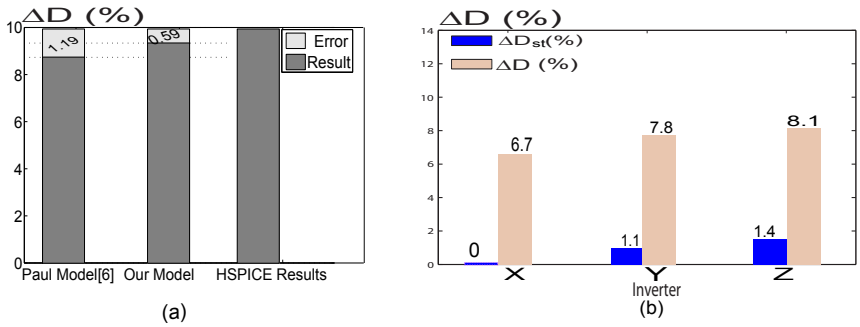

Fig. 5. (a) Comparison of models with HSPICE simulation,(b) ΔD of inverters and ΔD_{st} caused by the previous inverters

Y. Fig.4 (b) shows the percent ΔD_{st} of Y against the percent $\Delta\tau_i$. The figure shows that ΔD_{st} increases monotonically with $\Delta\tau_i$. However, the sensitivity to τ_i is less then unity. For example, 1% variation in the $\Delta\tau_i$ causes 0.83% additional ΔD_{st}. The magnitude of this difference depends on the C_L and other transistors parameters. However, they are beyond the scope of this paper.

Gate Delay Model: Equations 11 and 14 give the impact of NBTI on ΔD_{th} and ΔD_{st} delays. Substituting these terms in Eq. 9, we obtain the gate delay ΔD as:

$$\Delta D = \alpha.\frac{\Delta V_{th}}{(V_{gs} - V_{th})} + \left(\frac{\alpha + \nu_t}{1 + \alpha}\right).\kappa.\Delta\tau_i \tag{15}$$

The model presented in the equation is suitable for the circuit delay modeling. Fig.5(a) shows a comparison of Paul's model [6] and our model with the HSPICE simulation. The figure shows that our proposed model have error less than 0.59%, while in case of [6] model the error approaches 1.19%.

4 Circuit Delay Model

In conventional NBTI induced circuit delay models, NBTI impact on circuit delay is considered to be just a sum of delay increments of isolated gates [6, 7]. The correlation among gates and its impact on circuit delay is ignored.

Let us consider a circuit with n gates in a circuit. The circuit delay (ΔD_{circ}) consists of: (a) summation of the delays caused by intrinsic degradations of the gates, (b) summation of delays caused by correlation among gates (front-end delays). That is:

$$\Delta D_{circ} = \sum_{i=1}^{n} \Delta D_{th(i)} + \sum_{i=1}^{n-1} \Delta D_{st(i)} \tag{16}$$

where $\sum_{i=1}^{n} \Delta D_{th(i)}$ and $\sum_{i=1}^{n-1} \Delta D_{st(i)}$ are the summation to representing intrinsic delays and front-end delays respectively. To demonstrate the situation we consider the example circuit shown in Fig.2; run HSPICE simulation using 45nm PMOS transistor model and 1.0V supply voltage. Fig.5(b) shows the simulation results for the three inverters of Fig.2 at γ=0.8 for 10 years of operation. The figure reveals that:

– Inverter X have a constant τ_i that results in zero $\Delta D_{st(X)}$. However, it suffers from additional ΔD=ΔD_{th} =6.7%.

Table 1. Delays at input gates, output gates and paths in benchmark circuits

Circuit(a,b,c)*	no of Trans.	Delay at t=0	Percent Gate and Circuit Delay increments								
			10^5sec			10^7sec			10^8sec		
			ΔD_1	ΔD_n	ΔD_{circ}	ΔD_1	ΔD_n	ΔD_{circ}	ΔD_1	ΔD_n	ΔD_{circ}
C432(36,7,11)	996	11.68ns	1.37	3.09	2.25	2.98	5.5	5.04	4.41	11.99	7.43
C499(41,32,7)	1316	14.68ns	1.61	1.71	2.91	4.06	4.37	6.17	6.13	6.48	9.01
C880(60,26,5)	2118	16.75ns	1.98	2.78	4.43	3.79	6.08	10.32	3.78	9.18	10.53
C1355(41,32,16)	2484	9.58ns	1.20	2.96	1.21	2.71	6.44	2.48	4.01	7.34	5.90

a*=# of inputs, b=# of outputs, c=# of gates in the path,

ΔD_1=Delay of the gate at a primary input, ΔD_n =Delay of the gate at a primary output, ΔD_{circ}=Delay of a path in benchmarks.

– Inverter Y suffers from 7.8% delay due to NBTI. The additional 1.1% is due to $\Delta \mathrm{D_{st}}$ degradation that constitute 14% of . Similarly, the delay increment of inverter Z approaches 8.1% with a share of 17% from τ_i degradation.

The measurements showed that $\Delta \mathrm{D_{th}}$ in X causes an additional 3.0% delay to output transition $\tau_{o(X)}$. This increases $\tau_{i(Y}$ of Y that casues more ΔD (i.e. 7.8%) to Y than X. The higher delay of Z than Y have also the same reason.

5 Benchmark Simulations and Analysis

In this section, we present simulation results and their analysis for several benchmark circuits. We have modeled the impact of NBTI using a time dependent external voltage source. Behavior of the source is defined using Verilog-A module. Voltage across the module represent NBTI induced $\Delta \mathrm{V_{th}}$ that causes ΔD and consequently $\Delta \mathrm{D}_{circ}$. We simulated several ISCAS benchmark circuits to analyze NBTI impact on their delays. We have particularly focused on the following analysis: (a) delay of gates at primary input, (b) delay of gates at primary output, and (c) delay of complete paths in a circuit. Since γ of all the gates depend on the circuit topology so it extremely time consuming to determine γ of all the gates. We keep γ of all the primary input gates 0.8 and assume that it will remain same for all the gates.

Table 1 shows the simulation results for the delay of several benchmark circuits. From the table, we have the following observations:

– Delay of paths in the benchmarks circuits increase with increase in stress time. For instance, delay increment of the critical path in C432 for γ=0.8 is 2.25% after 10^5sec stress time, while it is 5.04% after 10^7sec and approaches 7.43% after 10^8sec stress. Other benchmarks also follow the same trend in their delay increment.
– In a given benchmark circuit and under identical γ values the path delay depend on topology of the circuits. For example, C499 and C1355 have same number of inputs and outputs. However, C499 suffers from 7.43% delay while C1355 suffers from 5.90% delay.
– Generally it is claimed that identical gates have similar delay increment under a given γ values. However, we observed that the claim is not true. For example, the primary input gate in C1355 have a delay increment of 4.01% after 10^8sec of stress, while an identical gate at the primary output have a delay increment of 7.34% after the same stress time. The additional 3.33% delay of the output gate is due to the effect of degradation of the previous gates that propagates to the final output gate in the benchmark.

6 NBTI Mitigation Techniques

So far we have investigated the root causes of NBTI mechanism at device level, its impact on gate delay and finally, on circuit delay. From the analysis, we conclude that the delays due to NBTI depend on: (a) Holes mobility degradation in the PMOS transistor inversion layer, (b) γ of the gates, (c) operational temperature, (d) supply voltage, and (d) locations of the gates in a circuit. Now we will describe some techniques at transistor level, gate level, and circuit level to mitigate the delays.

Holes Mobility Increment: NBTI can be mitigated at the transistor level by, (a) increasing robustness of the holes mobility against the N_{IT} at Si-SiO_2 interface, and (b) improving the interface structure between Si and SiO_2. In [17] Islam suggested that the mobility robustness can be achieved by using strained silicon (SiGe source/drain and contact etch stop layer) transistor. Although the scheme is expensive and dictates changes in fabrication process, it ensures minimum circuit delay under NBTI effect.

Temperature Reduction: The electrochemical reactions at Si-SiO_2 interface that cause NBTI degradation are thermally activated. Therefore, by tuning temperature to a lower value, we can reduce NBTI degradation at transistor level that will reduce delay increment at circuit level. Table 6 shows the impact of temperature reduction on the delay. The table shows that the delay of C880 for γ=0.8 is 10.53% at 125^{o}C. However, by reducing temperature to 75^{o}C the delay is only 6.63% (37% less than at 125^{o}C).

Supply Voltage Tunning: The exact impact of supply voltage tunning on NBTI is not clear and there are contradictory arguments. In [18], suggested lower V_{dd} to mitigate the delay increment, while in [7] negated the argument and favored higher V_{dd}. Our observation from the simulation affirmed the latter argument. Table 6 shows the simulation results for the voltage reduction. The table shows that supply voltage increment in C432 results in 6.95% (0.62% reduction) delay. We observed that supply voltage have a smaller impact than temperature. It is due to the fact only bond breaking sub-process (k_f in section II-A) is voltage/field dependent. All the other sub-processes are voltage independent [4]. Additionally, voltage increment shold be in limit as it will cause higher leakage currents.

Table 2. NBTI mitigation by temperature and voltage supply

Circuit	Temperature			Supply voltage		
	125^{o}C	75^{o}C	ΔD_t	1.1V	1.2V	ΔD_v
C432	7.43	5.60	34	7.43	6.95	0.62
C880	10.53	6.63	37	10.53	9.76	0.67

ΔD_t= % delay improvement by temperature reduction, ΔD_v = % delay improvement by voltage tuning.

Transistor Oversizing: Transistor oversizing is an effective way to reduce NBTI affects. In [6], the authors suggested 8.7% oversizing of the whole circuit to mitigate NBTI at circuit level. However, we observed that gates at the

primary output have more delay increment than gates at the primary input. Therefore, we choose to increase size of the gates at primary output.

7 Conclusion

In this paper we proposed a new NBTI induced gate delay model. Unlike traditional models that only considers NBTI impact on intrinsic delay of an isolated gates, we also consider the impact on output transition to show the delay correlation among gates. From the model demonstration, we found that depending on the activity ratio of a gate NBTI can cause up to 6.7% intrinsic delay and 3.0% output transition delay. The transition delay increase delay of the next gates as a result gates at outputs of a circuit suffer from more delays than gates at the inputs. Finally, we analyzed different techniques to mitigate NBTI. The analysis concluded that temperature reduction can mitigate 37% of NBTI induced delay. In future, we plane to use the delay model for developing NBTI induced delay testing schemes at circuit level.

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