Compact delay modeling of Latch-based Threshold Logic gates

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Abstract

In this paper we propose a new compact static delay model for latch-based CMOS Threshold logic gates. The particular effects captured by the model are: the dependency of the delay on threshold (data) values and the dependency of the delay vs. capacitive loading. The model parameters were extracted from several Threshold logic gate setups and the delay predicted by the model for a computer arithmetic basic circuit fully agree with circuit simulations.

1 Introduction and previous work

Threshold logic (TL) originally emerged in the early 60's as a generalized theory of logic gates, which includes conventional switching logic as its subset. A Threshold Logic Gate (LTG) is defined as an n-input processing element which basically perform the following Boolean function:

$$F(X) = sgn\{\mathcal{F}(X)\} = \begin{cases} 0, & if \ \ \mathcal{F}(X) < 0 \\ 1, & if \ \ \mathcal{F}(X) \geq 0 \end{cases} \quad (1)$$

$$\mathcal{F}(X) = \sum_{i=0}^{n-1} \omega_i \cdot x_i - T \quad (2)$$

where $X = \{x_0, x_1, \ldots, x_{n-1}\}$, $\Omega = \{\omega_0, \omega_1, \ldots, \omega_{n-1}\}$ and T are the set of Boolean input variables, the set of fixed signed integer weights associated with data inputs and the fixed signed integer threshold respectively. Please note in Equation (2), all the operators are algebraic.

TL is fundamentally more powerful that Boolean logic since the TL gate can perform more complex and wider functions (in terms of number of input variables) than the usual Boolean CMOS gates can. Several recent theoretical results confirmed the above potential advantages of TL over Boolean logic [7] especially in highly regular digital computer arithmetic building blocks. Moreover, several research investigations were carried in the mid and late 90's, with specific emphasis on TL gates implementations [1, 2, 4, 5]. In order to validate TL as a potential candidate for high-speed arithmetic there is a need for a rapid estimation of TL-specific circuits (and algorithms) speed when compared with Boolean counterparts performing the same function.

A fair comparison between Boolean and Threshold logic, in terms of delay, can be made only using real circuits, usually large enough to address by time-expensive circuit simulations. Another alternative is to use a fast, but less accurate, *static timing analysis*. Although there is a large number of static timing models (for Boolean CMOS) available in nowadays static timing analyzers, there is a lack of similar models for LTGs. In order to close this gap between Boolean CMOS and TL CMOS the goal of this paper is to investigate the specifics of a TL gate static delay model. Moreover, the aim of the proposed TL delay model is to capture the upper and lower TL gate delay bounds. Our model is targeted only for latch-based TL gates [3]. Although different CMOS TL gates with different circuit styles may have rather different delay models, we believe our delay model can be straightforward adopted for an entire class of so-called latch-based TL gates.

The paper is structured as follows: Section 2 reviews the latch-based TL gate the delay model is targeted for; Section 3 addresses several preliminary assumptions; the extraction of the new model parameters, the model errors involved and an application example are presented in Section 4; Section 5 presents some concluding remarks.

2 TL gate description

The TL gate under study [3] has the schematic presented in Figure 1. The gate is in principle a ratioed clocked differential cascode voltage switch (DCVS) circuit, operated with a single phase clock. It comprises a fast latched comparator and two parallel-connected sets of unit NMOS transistors, referenced herein as input data bank and threshold mapping bank. The gate pre-

sented in Figure 1 has $\omega_i = 1$ for every input while the same applies for every threshold mapping input (T_i). The total conductance of both transistor banks are compared by the latched comparator and the Y output is logic one if the current (conductance) generated by the data bank is greater than the current generated by the threshold mapping bank. Please note that, by design, the data bank is prevented to have similar conductance with threshold mapping bank, when the threshold is reached since an NMOS transistor with weight 0.5 is always on. This prevents the latch comparator entering in metastable state. After the gate have been regenerated the outputs, further changing of the data inputs will not be propagated to the outputs. This is since always only one of the M_6 or M_7 NMOS transistors are off, preventing the rising internal node from being connected to ground. Thus, the latch is an edge-triggered element.

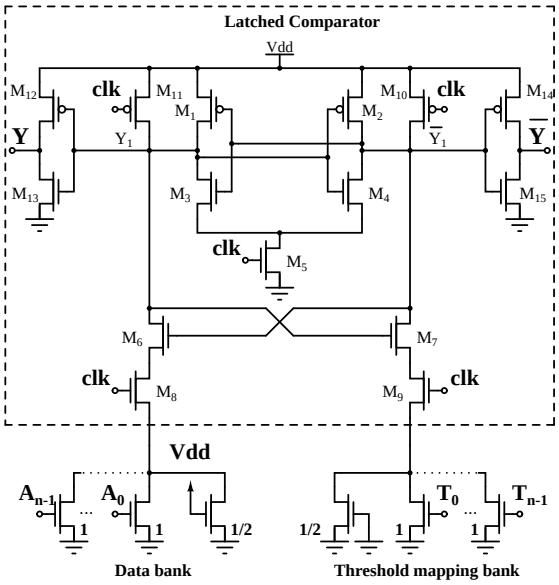

Figure 1: TL gate schematic

During the next section we use the following notations: $T = \Sigma_{i=0}^{n-1} T_i$, the total number of threshold mapping inputs assigned with logic one value; $N = \Sigma_{i=0}^{n-1} A_i$, the total number of logic one inputs in the input vector (assuming, as in Figure 1, $\omega_i = 1$) and $\Delta_{NT} = N - T$. Since $n = 32$ during the next sections, the following obvious conditions hold true: $T \leq 32$ and $N \leq 32$.

3 Preliminary assumptions

Since the gate under discussion is *clocked*, we capture in our model only $clk - Y$ delay dependencies. More in particular we will study $t_{d,clk-Y}$ as a function of N, Δ_{NT} and loading. Moreover, since the TL gate is a large fan-in device (e.g. $n = 32$ inputs accommodated in a single gate), deriving such a delay model would require too much computational resources in order to explore exhaustively the entire number of possible input vectors and threshold values. Thus, we make several simplifying assumptions regarding the possible combinations of input data vector and threshold values:

1. We assume in our models $\omega_i = 1$, similar with the gate from Figure 1. Different weight values may be possible in a more real TL circuit but $clk - Y$ delay is dependent only on the total number of data/threshold mapping inputs on logic one (N, T).
2. We assume only TL gates with $T > 0$ and $N > 0$. Since TL gate under discussion is differential, in Equation (2), we can consider the threshold mapping inputs as data inputs. The reverse holds true as well. Therefore, the cases $T < 0$ or $N < 0$ can be treated in a similar way, without loosing the generality of the problem.
3. We assume only the particular cases when a given input data generate a rising Y output. This implies $N \geq T$. Similar approach can be applied to the cases $N < T$ but the rising edge of $\overline{Y}$ should be taken into account now on.

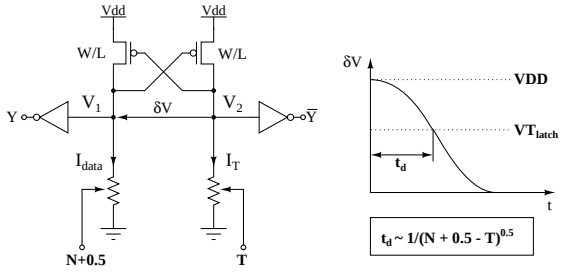

Figure 2: Conceptual diagram of the TL gate during evaluation

As mentioned in the above paragraphs, our model captures two effects. We describe them shortly in the following paragraphs.

1) delay dependency on T, Δ_{NT}

A conceptual diagram of how the model is derived from the real circuit is presented in Figure 2. A good preliminary assumption regarding the delay vs. T model is that $t_{d,clk-Y}$ is inversely proportional with the difference of currents generated by data bank and threshold mapping bank respectively. Thus: $t_{d,clk-Y}\,(T, \Delta_{NT}) \sim \frac{1}{\sqrt{I_{data} - I_T}}$. The rationale behind previous relation is the square dependency of V_1 and V_2

on the current generated by the MOS banks (assuming PMOS transistors in saturation during evaluation).

Since the NMOS transistors from both banks are operated in linear region (strong inversion), we may state that $I_{data} \sim N$, $I_T \sim T$ and consequently:

$$t_{d,clk-Y}(T, \Delta_{NT}) = a/\sqrt{N-b} + c, \qquad (3)$$

with parameter b dependent only on T. Please note again that always $I_{data} > I_T$ because there is always an open transistor in the data bank having $1/2$ aspect ratio for preventing metastabillity.

Since the regeneration phase delay is dependent on the current difference between the NMOS banks, it is expected a greater Δ_{NT} to imply a lower $clk-Y$ delay. Consequently, the lower T is, the slower TL gate it is. At the limit, the case $T = 1$, $N = 1$, is the worst case in terms of $clk - Y$ delay. In the next section we use that remark when we design the circuit benchmarks used to derive the lower and upper bounds for $t_{d,clk-Y}$ delay.

2) delay dependency on loading

When connected in a real circuit, a TL gate is always loaded with another gate. Therefore, similar with CMOS, the gate has a delay which depends on the number of TL data inputs connected to the output, h, on a simple linear relation [6]. Thus:

$$t_{d,clk-Y}(T, \Delta_{NT}, h) = g(T, \Delta_{NT}) \cdot h + p(T, \Delta_{NT}) \qquad (4)$$

with $g(T, \Delta_{NT})$ and $p(T, \Delta_{NT})$ describing the logical effort and the parasitic delay [6]. As expected, g and p depend not only on threshold T (the TL function it performs), but on the difference between the number of data inputs on logic one and threshold (Δ_{NT}). This increases the amount of simulation runs and complicates the analytical modeling of all the above factors as well. However, these particular differential TL gates have critical delay attained when $\Delta_{NT} = 0$. Thus, in next section we address the issue of g and p parameters extraction only in that critical case. Moreover, we show in the next section the upper $clk - Y$ delay bound is attained for every latch-based TL gate when $\Delta_{NT} = 0$.

4 Model parameters extraction and simulation results

In order to extract the model parameters we used several TL gate simulation setups. They have been simulated with Hspice. The results are provided using a TL gate designed in $.25\mu m$ feature size CMOS technology. We used BSIM3v3 models, typical corner, at 27° and $2.5V$ power supply. All tested inputs were buffered in order to provide real rising/falling voltage edges. Since the amount of simulation data was large, the model parameters were extracted and analyzed from the simulation output using productivity Perl scripts. The model functions (Equations (3), (4)) were then fitted using a numerical package.

1) delay dependency on T, Δ_{NT} (Equation 3)

There are many possible (T, Δ_{NT}) simulations points for a corresponding monotonically rising Y output. Based on preliminary assumptions from the previous section, only two representative data/threshold configuration scenarios were envisioned:

- **Scenario 1:** $T = ct.$ and Δ_{NT} sweeped in the range $[0, n-T]$;
- **Scenario 2:** $\Delta_{NT} = ct.$ and T sweeped in the range $[1, n]$.

These two scenarios are representative since they provide the upper and lower bounds for $clk - Y$ delay of a latch-based TL gate having a particular optimized transistor sizing. Figure 3 presents the simulated $t_{d,clk-Y}$ delay data sets vs. Δ_{NT} for several T values. The functions obtained from fitting are plotted on the same graph as well. Please note the simulation data were obtained with a single TL gate load ($h = 1$).

It can be remarked that the gate is, as expected, faster as the difference between the number of inputs on logic 1 and threshold T (Δ_{NT}) increases. We found the fastest switching point of our gate to be $(1, 31)$. Moreover, keeping $\Delta_{NT} = ct.$ and changing T, we found the gate has the worst case delay when $\Delta_{NT} = 0$ and $T = 1$. Thus, the lower and upper bounds for $t_{d,clk-Y}$ are the simulated curves in the following conditions: 1) $T = 1$, Δ_{NT} variable and 2) T variable, $\Delta_{NT} = 0$. The extracted values for parameters a, b, c for several representative cases are presented in Table 1. The maximum absolute error between the estimated and circuit simulation data is 7.3%. A remarkable result of our preliminary assumptions from previous section is the parameter b has the extracted value $T - 0.5$, which fully agrees with the fact N is internally shifted with 0.5 to avoid metastability.

Table 1: Extracted a, b, c parameters, $T = 1, 8, 16, 24$; Δ_{NT} variable, $h = 1$

Case	a (ps)	b	c (ps)	$\lvert\varepsilon\rvert_{max}$ (%)
T=1	220	0.5	83	7.35
T=8	86	7.5	115	5.89
T=16	63	15.5	131	4.30
T=24	44	23.5	150	2.97

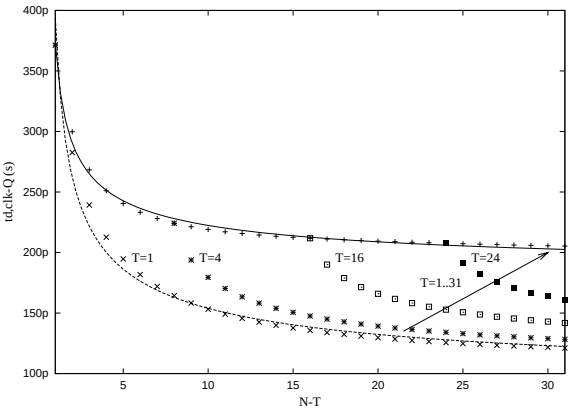

Figure 3: Plots of simulated $t_{d,clk-Y}$ delay sets vs. Δ_{NT}; $T = 1, 8, 16, 24$, $h = 1$

2) delay dependency on loading (Equation 4)

When considering the capacitive loading effect, the simulated TL gate was loaded with a similar gate, having variable multiplicity. The delay was plotted for various loading factors and we found that a simple linear relation holds true, similar with static CMOS [6]. The g and p parameters were obtained by linear regression for several particular cases ($T = 1, 8, 16, 24$, $\Delta_{NT} = 0$) and they are presented in Table 2. The maximum absolute error between estimated and simulated data is no greater than 6%.

Table 2: Extracted g and p parameters, h variable; $T = 1, 8, 16, 24$, $\Delta_{NT} = 0$

Case	g (ps)	p (ps)	$\lvert\varepsilon\rvert_{max}$ (%)
T=1	1.9	372	0.85
T=4	1.6	253	1.46
T=8	1.7	228	2.46
T=16	2.1	219	4.21
T=24	2.5	217	5.61

Example: In order to present the model utilization, we designed and simulated a TL gate computing the *carry-force* [7] of a group of $k = 4$ bits in real loading conditions ($h = 32$). The gate has the following Threshold function:

$$\alpha = sgn\{\sum_{i=0}^{3} 2^i (A_i + B_i) - 2^4\}.$$

According to the analysis presented in previous paragraphs we can state the critical delay occurs when $\sum_{i=0}^{3} 2^i (A_i + B_i) = 16$ since $\Delta_{NT} = 0$. Such a critical delay situation is attained when $A_3 = 1$, $B_3 = 1$ for example. The estimated maximum $clk - Y$ delay of the gate is $2.1 \cdot 32 + 219 = 286.2ps$ (see Table 2) and the simulated delay is $282ps$. The delay predicted by the model is overestimated with only 1.4%.

5 Conclusions

In this paper we presented a novel static delay model for latch-based TL gates. The particular effects captured by the model are: the dependency of the delay on threshold (data) values and the dependency of the delay vs. capacitive loading. The model parameters were extracted from several Threshold logic gate setups and the delay predicted by the model for a computer arithmetic basic circuit fully agree with circuit simulations. Although not complete the delay model presented in this paper will allow us to explore the effectiveness, in terms of speed, of specific TL circuits (e.g high-performance computer arithmetic). Further developments will target a more refined model that will capture the dependency of $clk - Y$ delay on data setup and hold.

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