Realistic Fault Models and Test Procedure for Multi-Port SRAMs

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Abstract: *This paper presents realistic fault models for multi-port memories with p ports, based on defect injection and SPICE simulation. The results show that the fault models for p-port memories consist of p classes: single-port faults, two-port faults,..., p-port faults. In addition, the paper discusses the test procedure for such memories. It shows that the time complexity of the required tests is not exponentially proportional with p, as published by different authors, but it is linear; irrespective of the number of ports the multi-port memory consists of.*

1 Introduction

In spite of the growing use of *Multi-port (MP)* memories, little *experimental* work has been published about their fault modeling and tests. In [1], an *ad hoc* test with no specific fault model was described. In [2], a BIST circuit for embedded *two-port (2P)* memories based on a very *simplistic* fault models was reported. For the same fault models, modified march tests and BIST circuits were reported in [3, 4, 5]. In [6, 7, 8, 9] *theoretical* fault models, together with their tests were developed. However, the introduced models are *not* based on any experimental/industrial analysis, and the proposed tests have a time complexity which is exponentially proportional with the number of ports; that makes them not practical. In [10], port interferences in 2P memories were *experimentally* analyzed, based on SPICE simulation; however, the analysis was restricted to only the interference between the bit lines and the word lines of the two ports. A similar, but theoretical work, has been reported in [11].

It can be seen from the above that little *experimental* research has been done on testing MP memories. In this paper, a complete analysis of spot defects in MP memories will be presented, resulting in realistic fault models requiring only linear tests. The paper is organized as follows. Section 2 establishes an inventory of all possible spot defects in the memory cell array. Section 3 derives the functional fault models based on the simulation results. Section 4 discusses the test procedure; while Section 5 ends with conclusions.

2 Classification of spot defects

Many faults in memory circuits are caused by undesired particles called *spot defects (SDs)*. A SD is thus a randomly occurring region of an extra or missing material in the layers used for the fabrication process. Since this work concerns with electrical simulation, the physical SDs should be electrically modeled. The missing material will be modeled as disconnections, while the extra material will be modeled as undesired connections. These disconnections and undesired connections can be electrically divided into three groups: *opens*, *shorts* and *bridges*; whereby an open is an extra resistance within a connection, a short is an undesired resistive path between a node and V_{cc} or V_{ss}, while a bridge is an undesired resistive path between two connections, which are not V_{cc} or V_{ss}. From now on, the term SD will used to mention an open, a shorts or a bridge.

Figure 1 shows a differential access *p-port* (pP) memory cell with p *read-write* ports, that will be the subject of this paper.

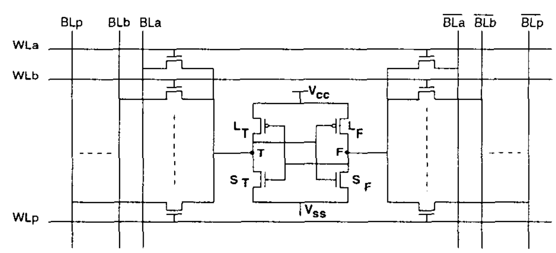

Figure 1. A differential p-port memory cell

In [12], all opens, shorts and bridges have been defined and located for a differential pP memory, similar to [14] for a *single-port (SP)* memory. The results show that there are $\frac{19p^2+67p+74}{2}$ possible SDs: $11p + 20$ opens, $6p + 4$ shorts, and $\frac{19p^2+33p+26}{2}$ bridges. For the bridges, the assumption is made that the nodes have to be located close to each other, such that a bridge only can occur within a singe cell or be-

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tween adjacent cells. The SPICE simulation of all possible SDs will require a significantly long time due the total number of SDs that needs to be simulated. However, the total of $\frac{19p^2+67p+74}{2}$ SDs can be placed into 49 groups [12], whereby only one SD from each group needs to be simulated; the behavior of other SDs within a group can be derived from the simulated one. The grouping is based on the fact that the memory cell has a symmetrical structure with p similar ports.

Table 1 shows the minimal set of opens that needs to be simulated [12] (see also Figure 1). They are divided into opens within a cell (OC), opens at bit lines (OB), and opens at word lines (OW). The third column in the table classifies the opens into *Single-port Fault Defects (SFDs)* and *Multi-port Fault Defects (MFDs)*. The SFDs are SDs that *only* can cause SP faults; i.e., faults that can be sensitized using a single port. The MFDs are defects that can cause SP faults as well as MP faults; the latter requires the use of multiple ports simultaneously in order to be sensitized. This classification is based on the simulation results done for a differential 2P memory [12, 15]: the SDs causing only SP faults are considered as SFDs, while SDs causing SP faults as well as two-port faults (i.e., faults requiring the use of two ports simultaneously in order to be sensitized) are considered as MFDs.

Table 1. List of opens

Open	Description	Class
OC1	Source of pull-up at true side	SFD
OC2	Drain of pull-up at true side	SFD
OC3	Drain of pull-down at true side	**MFD**
OC4	Source of pull-down at true side	**MFD**
OC5	Gate of pull-up at true side	SFD
OC6	Cross coupling at true side	SFD
OC7	Gate of pull-down at true side	SFD
OC8	Connection of the pass transistors	SFD
OC9	Pass transistor connection to T	SFD
OC10	Pass transistor connection to bit line	SFD
OC11	Gate of pass transistor at true side	SFD
OC12	V_{cc} path of the cell	SFD
OC13	V_{ss} path of the cell	SFD
OC14	V_{cc} path shared by adjacent cells	SFD
OC15	V_{ss} path shared by adjacent cells	SFD
OB_w	the bit line BL_i at the write side	SFD
OB_r	the bit line BL_i at the read side	SFD
OW	the word line WL_i	SFD

The shorts are divided into shorts within a cell (SC), shorts at bit lines (SB) and at word lines (SW). The minimal set of shorts required for the simulation is shown in the first column of Table 2 [12]. Each short is defined as a pair of nodes in which one node is V_{cc} or V_{ss}. In the table, the shorts which are MFDs are given in *bold*; i.e, SC2 is the only MFD.

On the other hand, the bridges have been divided into two groups:

• *Bridges within a cell (BC):* All bridges connecting two nodes of the same cell, including the two pairs of bit lines and the two word lines to which it is connected. The second column of Table 2 gives the minimal set of BCs required for the simulation [12]; see also Figure 1. Note that BC6 and BC7 are MFDs.

• *Bridges between cells (BCC):* All bridges connecting nodes of adjacent cells, including the bit lines and the word lines to which the cells are connected. For establishing all possible BCCs, the configuration shown in Figure 2 has to be considered. Note that the adjacent cells can belong to the same column, the same row, or to the same diagonal. Therefore, the BCCs are further divided into BCCs between cells in the same *row* (*r*BCCs), BCCs between cells in the *column* (*c*BCCs), and BCCs between cells in the same *diagonal* (*d*BCCs). The third, the fourth and the fifth column of Table 2 show the minimal set of BCCs that needs to be simulated [12]. In the table, e.g., T1 (F1) denotes the true (false) node of cell C_1, see also Figure 2. Note that all BCCs are MFDs, except cBCC4 and cBCC5.

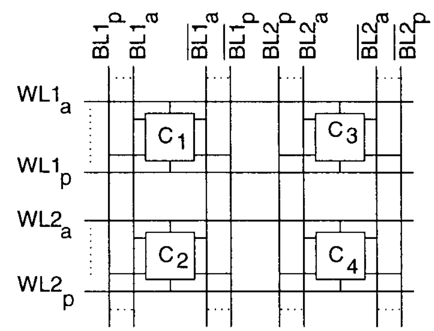

Figure 2. Four cell configuration

3 Functional Fault Models

The simulation has been done for all 49 SDs, which represent all possible SDs, by examining the resistance range from 0Ω to ∞Ω, for a 2P SRAM as well as for a 3P SRAM using Intel designs. Each faulty behavior is reported in terms of a *fault primitive (FP)*; i.e., a compact notation describing the faulty behavior. It should be noted that after the simulation has been done for 2P SRAMs [12, 15], the simulation has been redone only for MFDs for the 3P SRAM design [12].

In order to design memory tests for detecting faults, the electrical faults caused by the SDs (expressed in terms of FPs) have to be translated into *functional fault models (FFMs)*, whereby a FFM is defined as a non empty set of FPs. The FFMs for 2P SRAMs, which can be considered as a subset of the FFMs for *p*P SRAMs, are described in [12, 13, 15]. In this section, the FFMs for a differential *p*P SRAM will be presented based on: a) the simulation results

Table 2. Minimal set of shorts and bridges to be simulated

Shorts		Bridges	BCs	Bridges	rBCC	Bridges	cBCCs	Bridges	dBCCs
SC1	T-V_{cc}	BC1	T-F	**rBCC1**	T1-T3	**cBCC1**	T1-T2	**dBCC1**	T1-T4
SC2	T-V_{ss}	BC2	$T\text{-}BL_a$	**rBCC2**	T1-F3	**cBCC2**	T1-F2	**dBCC2**	T1-F4
SB1	$BL_a\text{-}V_{cc}$	BC3	$T\text{-}\overline{BL}_a$	**rBCC3**	T1-$BL2_a$	**cBCC3**	T1-$WL2_a$		
SB2	$BL_a\text{-}V_{ss}$	BC4	$T\text{-}WL_a$	**rBCC4**	T1-$\overline{BL2}_a$	cBCC4	$WL1_a\text{-}WL2_a$		
SW1	$WL_a\text{-}V_{cc}$	BC5	$BL_a\text{-}\overline{BL}_a$	**rBCC5**	$BL1_a - BL2_a$	cBCC5	$WL1_a\text{-}WL2_b$		
SW2	$WL_a\text{-}V_{ss}$	**BC6**	$BL_a\text{-}BL_b$	**rBCC6**	$BL1_a - BL2_b$				
		BC7	$BL_a\text{-}\overline{BL}_b$	**rBCC7**	$BL1_a - \overline{BL2}_a$				
		BC8	$BL_a\text{-}WL_a$	**rBCC8**	$B1_a - \overline{BL2}_b$				
		BC9	$BL_a\text{-}WL_b$						
		BC10	$WL_a\text{-}WL_b$						

for 2P SRAM and 3P SRAM, and b) the extension of the results for any MP memory with p ports.

Based on the number of ports required in order to sensitize the faults, FFMs for *memory cell array faults (MCAFs)* in pP memories can be classified into p classes: *single-port faults (1PFs)*, *two-port faults (2PFs)*, and *three-port faults (3PFs)*, ..., and *p-port faults (pPFs)*; see Figure 3. The 1PFs are faults that can be sensitized using SP operations; they are divided into 1PFs involving a single cell (1PF1s) and 1PFs involving two cells (1PF2s). The 2PFs are faults that can not be sensitized using SP operations; they require the use of the two ports of the memory simultaneously. On the other hand, pPFs are faults that can only be sensitized by acting on the p ports of the memory simultaneously. In the following, the classes will be discussed in detail.

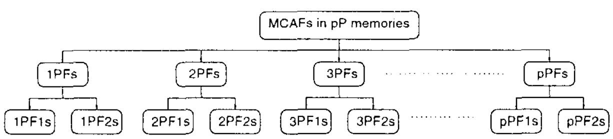

Figure 3. Classification of MCAFs in pP memories

3.1 Single-port faults (1PFs)

Single-port faults ($1PFs$) are divided into faults involving a *single-cell (1PF1s)* and faults involving *two-cells (1PF2s)*; see Figure 4. The 1PF1s consist of single-cell FPs; they have the property that the cell used for sensitizing the fault is the same cell as where the fault appears. The 1PF2s have the property that: (a) the application of a single-port operation (solid arrow in Figure 4) to the *aggressor cell (c_a)*, (b) the state of the cell c_a (dashed arrow in the figure), or (c) the application of a single-port operation to *the victim cell (c_v)* with cell c_a in certain state, has as a consequence that a fault will be sensitized in the cell c_v.

3.1.1 The 1PF1 fault subclass

To denote a 1PF1 fault, the following precise compact notation, referred to as a *fault primitive (FP)*, which will prevent

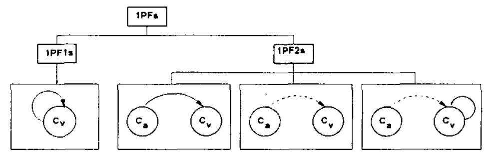

Figure 4. Classification of 1PFs

ambiguities and misunderstandings, will be used:

$< S/F/R >$ (or $< S/F/R >_v$): denotes an FP involving a single-cell (a 1PF1); the cell c_v (victim cell) used to sensitize a fault is the same as where the fault appears. S describes the value/operation *sensitizing* the fault; $S \in \{0, 1, w0, w1, w\uparrow, w\downarrow, r0, r1, \forall\}$, whereby 0 (1) denotes a *zero* (*one*) value, $w0$ ($w1$) denotes a write 0 (1) operation, $w\uparrow$ ($w\downarrow$) denotes an up (down) transition write operation, $r0$ ($r1$) denotes a read 0 (1) operation, and $\forall$ denotes any operation ($\forall \in \{0, 1, w1, w0, w\uparrow, w\downarrow, r1, r0\}$). If the fault effect of S appears after a time T, then the sensitizing operation is given as S_T. F describes the value of the *faulty* cell (v-cell); $F \in \{0, 1, \uparrow, \downarrow, ?\}$, whereby $\uparrow$ ($\downarrow$) denotes an up (down) transition, and ? denotes an undefined state of the cell (e.g., the true and the false node of the cell have the same voltage). R describes the logical value which appears at the output of the SRAM if the sensitizing operation applied to the v-cell is a *read* operation: $R \in \{0, 1, ?, -\}$, whereby ? denotes a random logical value (e.g., the voltage difference between the bit lines, used by the sense amplifier, is very small). A '$-$' in R means that the output data is not applicable; e.g., if $S = w0$, then no data will appear at the memory output, and for that reason R is replaced by a '$-$'.

The 1PFs consist of nine FFMs [12, 14]; see Table 3. The first column gives the abbreviation of the FFM, while the second column shows the FPs the FFM consists of:

1. *Stuck-at Fault (SAF)*: the logic value of a cell is always '0' ($< \forall/0/- >$) or '1' ($< \forall/1/- >$); see Table 3.
2. *Transition Fault (TF)*.
3. *Read Destructive Fault (RDF)* [19].
4. *Deceptive Read Destructive Fault (DRDF)* [19].
5. *Incorrect Read Fault (IRF)*.

6. *Random Read Fault (RRF).*
7. *Data Retention Fault (DRF)* [20].
8. *No Access Fault (NAF).*
9. *Undefined State Fault (USF).*

Table 3. List of 1PF1s; $x \in \{0, 1\}$

FFM	Fault primitives
SAF	$<\forall/0/->, <\forall/1/->$
TF	$<w\uparrow/0/->, <w\downarrow/1/->$
RDF	$<r0/\uparrow/1>, <r1/\downarrow/0>$
DRDF	$<r0/\uparrow/0>, <r1/\downarrow/1>$
IRF	$<r0/0/1>, <r1/1/0>$
RRF	$<r0/0/?>, <r1/1/?>$
DRF	$<1_T/\downarrow/->, <0_T/\uparrow/->, <x_T/?/->$
NAF	$<w\uparrow/0/->, <w\downarrow/1/->, <rx/x/?>$
USF	$<wx/?/->, <rx/?/?>$

3.1.2 The 1PF2 fault fault subclass

The 1PF2 faults are FFMs consisting of single-port FPs which involve two cells. To denote such faults, the following FP notation is used:

$<S_a; S_v/F/R>$ (or $<S_a; S_v/F/R>_{a,v}$): denotes an FP involving two cells (a 1PF2); S_a describes the sensitizing operation or state of the *aggressor cell (a-cell)*; while S_v describes the sensitizing operation or state of the *victim cell (v-cell)*. The a-cell (c_a) is the cell sensitizing a fault in an other cell called the v-cell (c_v). The set S_i is defined as: $S_i \in \{0, 1, w1, w0, w\uparrow, w\downarrow, r1, r0\}$ $(i \in \{a, v\})$.

The 1PF2s consist of seven FFMs [12, 14]; see Table 4.

1. *Disturb Coupling Fault (CF_{ds})* [18]: a *Disturb Coupling Fault* is defined as a fault whereby the v-cell undergoes a transition due to a write or a read operation applied to the a-cell. It consists of eight FPs : $<wx; 0/\uparrow/->$, $<wx; 1/\downarrow/->$, $<rx; 0/\uparrow/->$, and $<rx; 1/\downarrow/->$, whereby $x \in \{0, 1\}$.
2. *State Coupling Fault (CF_{st})* [20].
3. *Incorrect Read Coupling Fault (CF_{ir}).*
4. *Random Read Coupling Fault (CF_{rr}).*
5. *Deceptive Read Destructive Coupling Fault (CF_{dr}).*
6. *Read Destructive Coupling Fault (CF_{rd}).*
7. *Transition Coupling Fault (CF_{tr}).*

3.2 Two-port faults (2PFs)

To represent MP faults (e.g., two-port faults), the following terminology will be (re)introduced [6, 7, 8, 9]:

• *Strong fault:* This is a memory fault that can be **fully** *sensitized* by an operation; e.g., an SP write or read operation fails, two simultaneous read operations fail, etc. That means that the state of the v-cell is incorrectly changed, can not be changed, or that the sense amplifier(s) return(s) an incorrect result(s).

• *Weak fault:* This is a fault which is **partially** sensitized by an operation; e.g., due to a defect that creates a small disturbance of the voltage of the true node of the cell. However, a fault can be *fully sensitized* (i.e., becomes strong) when two (or more) weak faults are sensitized simultaneously, since their fault effects can be additive. This may occur when a pP operation is applied. Note that in the presence of a weak fault, all SP (read and write) operations pass correctly, and that the pP operations may pass correctly if the fault effects of the weak faults are not sufficient to fully sensitize a fault.

Table 4. List of 1PF2s; $x \in \{0, 1\}$

FFM	Fault primitives
CF_{ds}	$<wx; 0/\uparrow/->, <wx; 1/\downarrow/->,$ $<rx; 0/\uparrow/->, <rx; 1/\downarrow/->$
CF_{st}	$<1; 1/0/->, <1; 0/1/->,$ $<0; 1/0/->, <0; 0/1/->$
CF_{ir}	$<0; r0/0/1>, <0; r1/1/0>,$ $<1; r0/0/1>, <1; r1/1/0>$
CF_{rr}	$<0; r0/0/?>, <0; r1/1/?>,$ $<1; r0/0/?>, <1; r1/1/?>$
CF_{dr}	$<0; r0/\uparrow/0>, <0; r1/\downarrow/1>,$ $<1; r0/\uparrow/0>, <1; r1/\downarrow/1>$
CF_{rd}	$<0; r0/\uparrow/1>, <0; r1/\downarrow/0>,$ $<1; r0/\uparrow/1>, <1; r1/\downarrow/0>$
CF_{tr}	$<0; w\downarrow/1/->, <0; w\uparrow/0/->,$ $<1; w\downarrow/1/->, <1; w\uparrow/0/->$

The terminology of weak and strong faults is used in representing the MP faults as follows:

• F denotes a *strong fault* F, while wF denotes the *weak fault* F. For example, RDF denotes a strong Read Destructive Fault, while $wRDF$ denotes a weak Read Destructive Fault.

• $<fault_1>$ & $<fault_2>$ ...& $<fault_p>$: denotes a pPF consisting of p weak faults; '&' denotes the fact that the p faults *in parallel* (i.e., simultaneously) form the pPF. E.g., the wRDF&wRDF denote a 2PFs based on two weak RDFs.

Two-port faults (2PFs) can be considered as a combination of *two weak faults*, and divided into *faults involving a single cell (2PF1s)* and *faults involving two cells (2PF2s)* [12, 13, 15]; see Figure 5. A taxonomy of all realistic 2PFs is given also in the same figure; while Table 5 shows the FPs of which each 2PF is composed. They will be explained below.

3.2.1 The 2PF1 fault subclass

The 2PF1s are based on a combination of *two single-cell weak faults*. In addition, the two a-cells are the same as the

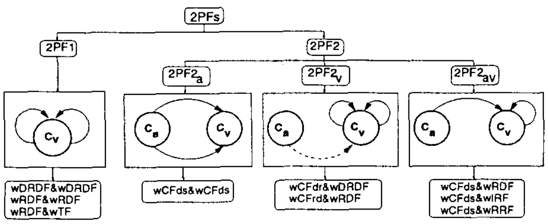

Figure 5. Classification and taxonomy of 2PFs

v-cell; see Figure 5. In order to sensitize a 2PF1, the same cell has to be acted upon simultaneously via the two ports. The following FP notation will be used for 2PF1s:

$< S_1 : S_2/F/R >_v$. It denotes a two-port FP involving a single cell (v-cell). This FP requires the use of the two ports *simultaneously*. S_1 and S_2 describe the sensitizing operations or states of the cell; ":" denotes the fact that S_1 and S_2 are applied *simultaneously* through the two ports. F describes the value of the v-cell. R is the read result of S_1 (and/or S_2) if it is a read operation.

The 2PF1 fault subclass consists of single-cell FPs, involving two simultaneous operations in order to be sensitized. They consist of three FFMs [12, 15]; see Table 5.

- $wDRDF\&wDRDF$: Applying two simultaneous read operations to a single cell causes the cell to flip, while the sense amplifiers return the *correct values*; see Figure 5. This is because the flipping of the cell happens relatively slowly. The wDRDF&wDRDF consists of two FPs: $< r0 : r0/ \uparrow /0 >_v$ (i.e., applying two simultaneous $r0$ operations to cell c_v will flip the cell to 1, and the sense amplifiers return the correct values), and $< r1 : r1/ \downarrow /1 >_v$. It can be caused by the following defects: OC3, OC4, SC2, and cBCC3; see Table 1 and Table 2.
- $wRDF\&wRDF$: Applying two simultaneous read operations to a single cell causes the cell to flip and the sense amplifiers return *incorrect* values. The wRDF&wRDF consists of two FPs (see Table 5) and can be caused by the same defects as those causing the wDRDF&wDRDF, but with different resistance values of the defect.
- $wRDF\&wTF$: A cell fails to undergo a write transition if a read operation is applied to the same cell simultaneously. The wRDF&wTF consists of two FPs (see Table 5) and can be caused by BC6; see Table 2.

3.2.2 The 2PF2 fault subclass

The 2PF2s are based on a combination of weak single-cell faults and weak faults involving two cells. Depending on to which cells the two simultaneous operations are applied (to the a-cell and/or to the v-cell), the 2PF2s are divided into three types (see Figure 5).

The $2PF2_a$ faults (the subscript a indicates that the sensitizing operations has to be applied to the a-cell): These faults are sensitized in cell c_v by applying two simultaneous operations to the same *a-cell* c_a (solid arrows in the Figure 5). The following FP notation is used to denote $2PF2_a$ faults:

$< S_a : S_a; S_v/F/R >_{a,v}$. It denotes an FP whereby both sensitizing operations, S_a, are applied simultaneously to the a-cell. S_v denotes the state of the v-cell. F denotes the value of the faulty cell c_v. Note that in that case R will be replaced with '$-$' since S_v can not be a read operation.

The $2PF2_a$ consists only of one FFM: $wCF_{ds}\&wCF_{ds}$ with eight FPs (see Table 5): $< w0 :rd; 0/ \uparrow /- >$, $< w0 :rd; 1/ \downarrow /- >$, $< w1 :rd; 0/ \uparrow /- >$, $< w1 :rd; 1/ \downarrow /- >$, $<rx :rx; 0/ \uparrow /- >$, and $<rx :rx; 1/ \downarrow /- >$; whereby $x \in \{0, 1\}$, and d denotes the *don't care value*. Note that the $< w0 :rd; 1/ \downarrow /- >$ denotes only one FP since the read value is irrelevant; the read *operation*, rather than the read *value*, is used to sensitize the fault. Note also that $<rx :rx; 0/ \uparrow /- >$ denotes two FPs since $x \in \{0, 1\}$. The $2PF2_a$ can be caused by rBCC1, rBCC2, rBCC3, rBCC4, rBCC5, rBCC6, rBCC7, and rBCC8; see Table 2.

The $2PF2_v$ faults: These faults are sensitized in cell c_v by applying two simultaneous operations to the same cell c_v (solid arrows in the Figure 5), while the a-cell has to be in certain state (dashed arrow in the figure). The following FP notation is used for $2PF2_v$ faults:

$< S_a; S_v : S_v/F/R >_{a,v}$. It denotes an FP whereby both sensitizing operations, S_v, are applied simultaneously to the v-cell. S_a describes the state of the a-cell.

The $2PF2_v$, which can be caused by rBCC1, rBCC2, cBCC1, cBCC2, dBCC1, and dBCC2 (see Table 2), consists of two FFMs:

- $wCF_{dr}\&wDRDF$: Applying two simultaneous read operations to cell c_v will cause the cell to flip if cell c_a is in a certain state. The read operations return *correct* values. The $wCF_{dr}\&wDRDF$ consists of four FPs; see Table 5.
- $wCF_{rd}\&wRDF$: Applying two simultaneous read operations to cell c_v will cause the cell to flip if cell c_a is in a certain state. The read operations than return *wrong* values. This FFM consists of four FPs; see Table 5.

The $2PF2_{av}$ faults: This fault type is sensitized by applying two simultaneous operations: one to cell c_a and one to cell c_v; see Figure 5. The following FP notation is used to denote the $2PF2_{av}$:

$< S_a : S_v/F/R >_{a,v}$. It denotes an FP whereby the sensitizing operation S_a is applied to the a-cell, and the sensitizing operation S_v is applied to the v-cell.

The 2PF2$_{av}$, caused by BC6, BC7, rBCC6, and rBCC8, consists of three FFMs; see Table 5.

• $wCF_{ds}\&wRDF$ with four FPs: A read operation applied to cell c_v flips the cell and the sense amplifier returns an incorrect value *if* a write operation is applied to cell c_a *simultaneously*.

• $wCF_{ds}\&wIRF$ with four FPs: A read operation applied to cell c_v returns an incorrect value *if* a write operation is applied to cell c_a *simultaneously*. It should be noted that the state of cell c_v does not change.

• $wCF_{ds}\&wRRF$ with four FPs: A read operation applied to cell c_v returns a random value *if* a write operation is applied to cell c_a *simultaneously*.

Table 5. List of 2PFs; $x \in \{0,1\}$, $d = don't\ care$

FFM	Fault primitives
wDRDF&wDRDF	$< r0 : r0/\uparrow/0 >, < r1 : r1/\downarrow/1 >$
wRDF&wRDF	$< r0 : r0/\uparrow/1 >, < r1 : r1/\downarrow/0 >$
wRDF&wTF	$< r0 : w\uparrow/0/- >, < r1 : w\downarrow/1/- >$
wCF$_{ds}$&wCF$_{ds}$	$< w0 : rd; 0/\uparrow/- >, < w0 : rd; 1/\downarrow/- >,$ $< w1 : rd; 0/\uparrow/- >, < w1 : rd; 1/\downarrow/- >,$ $< rx : rx; 0/\uparrow/- >, < rx : rx; 1/\downarrow/- >$
wCF$_{dr}$&wDRDF	$< 0; r0 : r0/\uparrow/0 >, < 0; r1 : r1/\downarrow/1 >,$ $< 1; r0 : r0/\uparrow/0 >, < 1; r1 : r1/\downarrow/1 >$
wCF$_{rd}$&wRDF	$< 0; r0 : r0/\uparrow/1 >, < 0; r1 : r1/\downarrow/0 >,$ $< 1; r0 : r0/\uparrow/1 >, < 1; r1 : r1/\downarrow/0 >$
wCF$_{ds}$&wRDF	$< w0 : r0/\uparrow/1 >, < w0 : r1/\downarrow/0 >,$ $< w1 : r0/\uparrow/1 >, < w1 : r1/\downarrow/0 >$
wCF$_{ds}$&wIRF	$< w0 : r0/0/1 >, < w0 : r1/1/0 >,$ $< w1 : r0/0/1 >, < w1 : r1/1/0 >$
wCF$_{ds}$&wRRF	$< w0 : r0/0/? >, < w0 : r1/1/? >,$ $< w1 : r0/0/? >, < w1 : r1/1/? >$

It should be noted that the above 2PFs are valid for 2P memories which support simultaneous reading and writing of the same location, whereby the read data is discarded. If this is not supported, then the FFM: wRDF&wTF will not be realistic. In addition, the FFM: wCF$_{ds}$&wCF$_{ds}$ will consist only of the FPs sensitized by simultaneous read operations to the same location.

3.3 Three-port faults

The simulation results found for 3P SRAMs show that in addition to 1PFs and 2PFs, three-port faults (3PFs) can also be sensitized; the latter requires the use of the three ports simultaneously. The 3PFs can be considered as a combination of *three weak faults*; they divided into faults involving a single cell (3PF1s) and faults involving two cells (3PF2s) (see Figure 6). A taxonomy of all realistic 3PFs is given in the same figure; while Table 6 shows the FPs of which each 3PF is composed. The FP notation for 3PFs is similar (but extended) to that for 2PFs; see Section 3.2. A similar explanation can be given for 3PFs as that for 2PFs; see also Figure 5 and Table 5.

It should be noted that the 3PFs discussed above are valid for memories allowing for two simultaneous reads

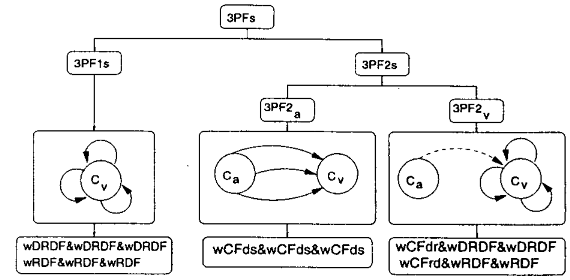

Figure 6. Classification and taxonomy of 3PFs

and a write of the same location (i.e., 'wx_c:ry_c:ry_c', $x, y \in \{0,1\}$). If this is not supported, then the FFM: $wCF_{ds}\&wCF_{ds}\&wCF_{ds}$ will consist only of the FPs sensitized by three simultaneous read operations to the same location; i.e., '$<rx :rx :rx; 0/\uparrow/- >_{a,v}$' and '$<rx :rx :rx; 1/\downarrow/- >_{a,v}$'.

Table 6. List of 3PFs; $x \in \{0,1\}$, $d = don't\ care$

FFM	Fault primitives
wDRDF&wDRDF&wDRDF	$< r0 : r0 : r0/\uparrow/0 >,$ $< r1 : r1 : r1/\downarrow/1 >$
wRDF&wRDF&wRDF	$< r0 : r0 : r0/\uparrow/1 >,$ $< r1 : r1 : r1/\downarrow/0 >$
wCF$_{ds}$&wCF$_{ds}$&wCF$_{ds}$	$< w0 : rd : rd; 0/\uparrow/- >,$ $< w0 : rd : rd; 1/\downarrow/- >,$ $< w1 : rd : rd; 0/\uparrow/- >,$ $< w1 : rd : rd; 1/\downarrow/- >,$ $< rx : rx : rx; 0/\uparrow/- >,$ $< rx : rx : rx; 1/\downarrow/- >$
wCF$_{dr}$&wDRDF&wDRDF	$< 0; r0 : r0 : r0/\uparrow/0 >,$ $< 0; r1 : r1 : r1/\downarrow/1 >,$ $< 1; r0 : r0 : r0/\uparrow/0 >,$ $< 1; r1 : r1 : r1/\downarrow/1 >$
wCF$_{rd}$&wRDF&wRDF	$< 0; r0 : r0 : r0/\uparrow/1 >,$ $< 0; r1 : r1 : r1/\downarrow/0 >,$ $< 1; r0 : r0 : r0/\uparrow/1 >,$ $< 1; r1 : r1 : r1/\downarrow/0 >$

The 3PFs, which are divided into 3PF1s and 3PF2s, can be considered as an extension of the 2PFs; see Figure 5 and Figure 6. The 3PF1s, which consist of two FFMs, can be considered as an extension of the 2PF1s. For instance, the 3PF1, wRDF&wRDF&wRDF, is an extension of the 2PF1 wRDF&wRDF. On the other hand, the introduced 3PF2s are divided into the fault types 3PF2$_a$ and 3PF2$_v$, which are extensions of the 2PF2$_a$, respectively, the 2PF2$_v$. By inspecting the two figures, one can see that there is no 3PF that can be considered as an extension of the 2PF1, wRDF&wTF, neither of the 2PF2$_{av}$ (i.e., 2PF2 sensitized by applying the two simultaneous sensitizing operations to two different cells: a-cell and v-cell). Such faults are caused by bridges between bit lines belonging to two different ports [12, 15]. It has been shown with Inductive Fault Analysis that a bridge only occurs between physically adjacent lines, and that the occurrence probability of bridges involving *at the most* two nodes is very large (96.6% on the average) compared with bridges involving more than two nodes

[12, 15]. Therefore the assumption can be made that the $2PF2_{av}$ can only be caused by bridges involving at most two bit lines (belonging to different ports) that are physically adjacent to each other. That means that, irrespective of the number of ports the MP memory consists of, the bridges between two bit lines belonging to any two different ports can only cause a $2PF2_{av}$. Therefore, this is a unique 2PF that can not be extended. A similar explanation can given for the 2PF1: wRDF&wTF.

Based on the above discussion, the pPFs ($p > 2$) can be derived, and are described below.

3.4 p-port faults (pPFs)

The pPFs are faults that can only be sensitized by applying p simultaneous operations; they are divided into faults involving a single-cell (pPF1s) and faults involving two cells (pPF2s); see Figure 7.

The pPF1s are based on a combination of *p single-cell weak faults*. The pPF2s are divided into two types: (a) The $p\text{PF2}_a$ which is based on a combination of p weak faults involving two cells; i.e., a fault is sensitized in cell c_v by applying p simultaneous operations to the same cell c_a; and (b) The $p\text{PF2}_v$ which is based on a combination of $(p-1)$ single-cell weak faults and one weak fault involving two cells, that requires the operation to be performed to the v-cell while the a-cell is in a certain state; i.e., the fault is sensitized by applying p simultaneous operations to the v-cell *and* the a-cell is in a certain state. A taxonomy of all realistic pPFs is also given in Figure 7; a similar explanation can be given for pPFs as that given for 2PFs and 3PFs.

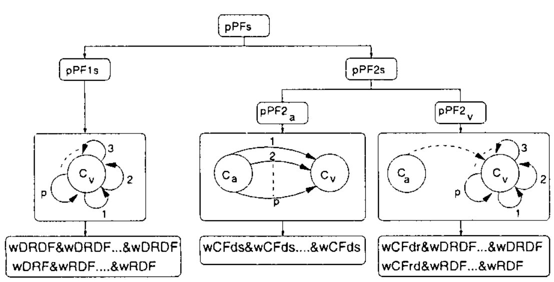

Figure 7. Classification and taxonomy of pPFs

4 Test procedure

As mentioned in Section 3, memory cell array faults for a p-port memory are divided into p classes: 1PFs, 2PFs, 3PFs, ..., and pPFs.

For the detection of 1PFs (i.e., conventional faults occurring in SP memories), a test such as MATS+, March C-, etc. [14, 16, 17, 18] can be used. The test has to be applied in *the worst case* p times: once via each port.

For the detection of pPFs with $p > 1$ (i.e., 2PFs, 3PFs, etc.) special tests are required. By inspecting the pPFs introduced in Section 3, it can be seen that the pPF1, $p\text{PF2}_a$ and $p\text{PF2}_v$ faults require p simultaneous operations to the same location in order to be sensitized; therefore the required tests for such faults will be single addressing (i.e., both ports use the same address). If we assume that the memory cell array consists of n locations, then the time complexity of such tests will be $\theta(n)$.

On the other hand, the $2PF2_{av}$ faults require the access of two different locations at a time in order to be sensitized (i.e., one operation to the a-cell and one to the v-cell); therefore the test for such faults requires double addressing (i.e., it accesses two different addresses at a time). It has been shown with IFA that the SDs can only occur between physical adjacent cells [12, 15]. Therefore, for a given v-cell, the test only has to access the limited number of v-cell's neighbors, which are the possible a-cells. As a consequence, the required test has a worst time complexity of $\theta(n)$. However, the test requires the use of topological addressing, rather than logical addressing.

The question that arises now is the following: In order to test a p-port memory, do we need to test each pPF class (i.e., 1PF, 2PF, 3PF, etc) separately? That is apply:

1. Test(s) to detect 1PFs p times.
2. Test(s) to detect 2PFs $C_2^p = \frac{p^2-p}{2}$ times.
3. Test(s) to detect 3PFs C_3^p times.

.. ..

p. Test(s) to detect pPFs once.

The answer to the above question is "*no*". The above test procedure can be optimized by taking into consideration the nature of each pPF class; this will be discussed below.

The pPF class consists of pPF1 and pPF2. The pPF1s for $p > 2$ consists of two FFMs that are extensions of two FFMs of 2PF1s; see Figure 5 and Figure 7. The sensitization of the pPF1s for $p > 2$ requires the application of p simultaneous read operations to the same location. This will also sensitize 2PF1s, 3PF1s, ... , and $(p-1)$PF1s; except the 2PF1, wRDF&wTF, since that fault is a unique 2PF and has no extension for pPFs with $p > 2$. Therefore, a test detecting pPF1s will also detect all $(p-1)$PF1s, ..., 3PF1s, and 2PF1s; except wRDF&wTF. That fault, caused by bridges between bit lines belonging to the same column and to *two different ports* [12, 15], is sensitized by applying a simultaneous read and write to the same location using the two ports; the write operation will fail due to the defect. The first assumption is to apply a test for such faults C_2^p times. However, this can be reduced to only p times as follows:

1. Apply a test detecting wRDF&wTF by performing a write operation via the first port (P_a), and read operations via the other $(p-1)$ ports. In that case, the fault

will be detected if it is caused by a bridge between the bit lines of port P_a and P_i; $P_i \neq P_a$.

2. Apply a test detecting wRDF&wTF by performing a write operation via P_b, and read operations via the other $(p-1)$ ports. In that case, the fault will be detected if it is caused by a bridge between the bit lines of P_b and P_i; $P_i \neq P_b$.

...

p. Apply a test detecting wRDF&wTF by performing a write operation via P_p, and read operations via the other $(p-1)$ ports. In that case, the fault will be detected if it is caused by a bridge between the bit lines of P_p and P_i; $P_i \neq P_p$.

On the other hand, pPF2s for $p > 2$ are divided into pPF2$_a$ and pPF2$_v$; both are extensions of 2PF2$_a$ and 2PF2$_v$ (see Figure 5 and Figure 7). The sensitization of the pPF$_a$ requires the application of p simultaneous operations to the a-cell. This will also sensitize 2PF2$_a$, 3PF2$_a$, ... , and $(p-1)$PF2$_a$. A similar explanation can be given for pPF2$_v$. Therefore, a test detecting pPF2$_a$ will also detect all $(p-1)$PF2$_a$, ..., 3PF2$_a$, and 2PF2$_a$s; while a test detecting pPF2$_v$ will also detect all $(p-1)$PF2$_v$, ..., 3PF2$_v$, and 2PF2$_v$. Since the 2PF2$_{av}$ faults have no extension for pPFs (see Figure 5 and Figure 7); they are unique 2PFs and for testing they have to be considered separately . Such faults are caused by bridges between bit lines belonging to *two different ports*, to the same (or adjacent) column(s) [12, 15]. Their detection requires the application of a write operation to the a-cell and a read operation to the v-cell simultaneously [13]. In order to detect the 2PF2$_{av}$ faults in a p-port memory, the first assumption is to apply a test for such faults C_2^p times. However, this can be reduced to p times; this can be done in a similar way as for wRDF&wTF.

Based on the above, one can conclude that testing a p-port memory can be done by applying:

1. A test(s) to detect 1PFs p times.
2. A test(s) to detect pPFs $(p > 1)$ one time; this include pPF1s (except wRDF&wTF), pPF2$_a$s and pPF2$_v$s.
3. A test(s) to detect the wRDF&wTF faults p times
4. A test(s) to detect the 2PF2$_{av}$ faults p times.

It should be clear from the above that the tests for a MP memory have a time complexity of $\theta(p.n)$, whereby p is the number of ports and n is the size of the memory cell array.

5 Conclusions

In this paper a complete analysis of all spot defects in an p-port SRAM design has been performed, based on circuit simulation, resulting in realistic functional fault models (FFMs). The results show that the fault models for p-port memories consist of p classes: single-port faults (1PFs), two-port faults (2PFs), ..., p-port faults (pPFs). The 1PFs are faults that can be sensitized using single-port operations. On the other hand, pPFs are faults that can *not* be sensitized using single-port operations; they require the use of the p ports of the memory *simultaneously*. A precise notation for all faults has been presented, such that ambiguities and misunderstandings will be prevented.

The test procedure for p-port memories has been presented. The time complexity of the tests required for the detection of the introduced realistic pPFs are of $\theta(n)$ in the worst case, whereby n is the size of the memory; irrespectively the number of ports the multi-port memory consists of. This is very attractive industrially.

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