Transient Faults in DRAMs: Concept, Analysis and Impact on Tests

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Abstract: *Memory fault models have always been considered not to change with time. Therefore, tests constructed to detect sensitized faults need not take into consideration the time period between sensitizing and detecting the fault. In this paper, a new class of memory fault models is presented, where the time between sensitizing and detection should be considered. The paper also presents fault analysis results, based on defect injection and simulation, where transient faults have been observed. The impact of transient faults on testing is discussed and new detection conditions, in combination with a test, are given.*

Key words: *transient faults, functional fault models, DRAMs, defect simulation, detection conditions, memory testing.*

1 Introduction

One of the basic assumptions about *functional fault models (FFMs)* in memories is that they are constant in time. That is, once an FFM is sensitized, the fault effect remains present, unless a subsequent operation is performed that results in eliminating the sensitized fault effect (either by directly overwriting the fault effect, or as a result of sensitizing a different FFM that is linked to this sensitized FFM). As a result of this assumption, tests constructed to detect sensitized FFMs need not take into consideration the time period between sensitizing and detecting the FFM, as long as precautions are taken so that the sensitized FFM is not eliminated [vdGoor98].

FFMs are represented as sets of *fault primitives (FPs)* [vdGoor00]. An FP is a simple, compact and unambiguous way to associate the faulty behavior exhibited by a given memory cell as a result of a given *sensitizing operation sequence (SOS)*. FPs are defined as $<S/F/R>$, where S stands for the SOS, F for the state of the faulty cell and R for the output on a read operation. In this paper, $S \in \{0, 1, 0w0, 0w1, 1w0, 0r0, 1r1, 0w0r0, 0w1r1, 1w0r0, 1w1r1\}$, where, for example, the 0 in $0w1$ represents the initial value of the cell before the $w1$ is applied. $F \in \{0, 1, ?\}$, where ? denotes the unknown or random state. $R \in \{0, 1, ?, -\}$, where ? means an unpredictable read result, and $-$ denotes the fact that the SOS does not end with a read operation to the victim. For example, the FP $<0w1/0/->$ represents the up-transition fault (TF↑). $S = 0w1$ denotes that the cell contains the value 0, after which a $w1$ operation is applied to perform an up-transition in the cell. $F = 0$ means that the cell remains in state 0, and $R = -$ means that S does not apply a read operation to the victim.

Previous work has shown that a special variant of an FP exists: $<S_T/F/R>$, whereby the faulty behavior, sensitized by the SOS S_T, occurs only after a given time period T. An example of such an FP is a Data Retention Fault (DRF) $<1_T/0/->$ [Dekker90]. This fault causes the cell to loose its value (the value changes from 1 to 0) after a time period T. However, the other two components of an FP have, until now, been thought to have a permanent nature that is not time dependent.

Here, we show that some FFMs may, in fact, change in time without the need to perform any external memory operation at all. This change results sometimes in *hiding* the sensitized faulty behavior. In terms of FPs, we show that under some circumstances the faulty state of the cell (F) may have a limited *lifetime* L. Such a time dependent faulty state is denoted by F_L. For example, the defective DRAM cell shown in Figure 1, where a resistive element (R_{def}) is inserted between the pass transistor and the cell capacitor. If R_{def} has a high enough resistance, the cell would be partially disconnected from the bit line (BL). As a result, a $0w1$ operation would not be able to charge the cell up to 1, resulting in a TF↑ = $<0w1/0/->$. Yet, the $0w1$ *only partially* charges the cell, thereby resulting in a weak stored 0. Since the cell has a PMOS pass transistor, leakage currents charge the cell up to 1. Therefore, the stored weak 0 is lost before it is possible to refresh the cell back to its incorrect 0 value. Since TF↑ is restored after some period of time L, this FFM is called *transient* and is

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denoted as TF↑ = $<0w1/0_L/->$. The actual value of the lifetime L depends on two basic factors:

- the amount of leakage current into the cell, and
- the initial voltage of the weak logic value stored in the cell, which in turn depends on the value of the defect resistance.

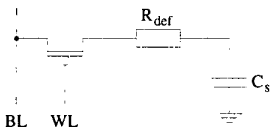

Figure 1. DRAM memory cell with an open defect.

This paper is organized as follows. First, a quantitative analysis of transient faults is made in Section 2. Then, Section 3 explores the space of transient faults. Next, Section 4 describes the consequences transient faults have on testing. Finally, Section 5 ends with the conclusions.

2 Quantifying transient faults

This section starts with enumerating the causes for leakage currents in Section 2.1. Then, Section 2.2 analyzes the timing of transient faults.

2.1 Leakage current mechanisms

Leakage currents are important to DRAMs because of the cell retention time requirements, which have increased from 16 ms in early 4 Mb DRAMs to as much as 256 ms for some types of low-power DRAM products [Adler95]. For current types of DRAMs, a number of leakage mechanisms exist that result in depleting the charge stored in a DRAM cell.

1. leakage through the pass transistor to the substrate
2. subthreshold leakage through pass transistor to bit line [Hanafi98]
3. leakage between cell capacitor plates through insulator [Romanenko98]
4. leakage between adjacent cell capacitors [Dietl90]
5. other technology specific leakage mechanisms [Adler95]

In a well constructed CMOS DRAM cell, the most important leakage mechanism of these is leakage through pass transistor to substrate (Mechanism 1). However, Hanafi[98] reports that subthreshold leakage current is the main leakage mechanism for silicon-on-insulator (SOI) DRAMs.

2.2 Timing of transient faults

In this section, the simulated memory is analyzed to approximate the value of the lifetime (L) of the observed transient FPs. Figure 2(a) shows a scale of the voltage within a DRAM cell, where a number of important cell voltages are indicated. If a memory is defect free, write operations set the stored voltage within the cell to either V_{dd} or GND, depending on the stored logic value. V_{mp} is the mid-point voltage. In a perfectly balanced sense amplifier, a stored voltage above V_{mp} is read as logic H, while a stored voltage below V_{mp} is read as logic L. However, parametric mismatches in the sense amplifier can amplify the bit line voltage differential in the wrong direction. Sarpeshkar[91] identifies four important parameters that cause sense amplifier imbalance:

1. transconductance of the sense amplifier transistors
2. gate-source parasitic capacitance of transistors
3. threshold voltage of transistors
4. bit line capacitance

As a result of sense amplifier imbalance, three voltage ranges within the cell can be identified: logic H, logic L and sense amplifier sensitivity (see Figure 2(a)). If a cell contains a voltage in the logic H range ($V_{dd} \rightarrow V_{hi}$), then a read operation always succeeds in setting the sense amplifier to 1 (cell on BT) or to 0 (cell on BC). If a cell contains a voltage in the logic L range ($V_{lo} \rightarrow$ GND), then a read operation always succeeds in setting the sense amplifier to 0 (cell on BT) or to 1 (cell on BC). If the cell contains a voltage in the sense amplifier sensitivity range ($V_{hi} \rightarrow V_{lo}$), then the effect of a read operation is unpredictable; it depends on the parametric mismatches in the sense amplifier.

After a write operation has set the cell voltage to GND, leakage currents through the PMOS pass transistor gradually charge the cell up. The cell should be refreshed before the cell voltage reaches V_{lo} in order to maintain the stored logic value. Therefore, the refresh time (t_{ref}) is less than the time needed for leakage currents to charge the cell up from GND to V_{lo}. If the memory is defective, write operations may not succeed in setting the cell voltage to GND, which means that it would take leakage currents less time to charge the cell up to V_{lo}.

In order for transient FPs to eliminate the fault effect of a cell, leakage currents should be able to charge the cell up from V_{lo} to V_{hi} in a time period $L < t_{ref}$. This L is considered to be the minimum transition time for a transient FP. Next, we will attempt to calculate the value of L for the DRAM under consideration.

Consider the memory structure shown in Figure 2(b), where the following parameters are given [Al-Ars99].

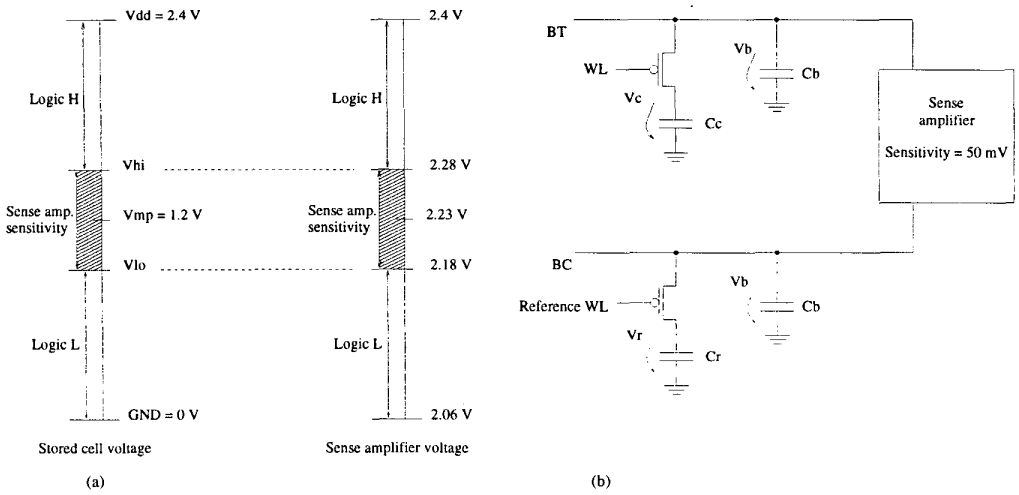

Figure 2. Regions of the voltage (a) stored within a DRAM cell, and (b) across the sense amplifier inputs.

- Storage cell capacitance: $C_c = 50$ fF
- Logic 1 on BT is $V_c = 2.4$ V, and 0 is $V_c = 0$ V
- Reference cell capacitance: $C_r = 50$ fF
- Mid-point voltage in reference cell is $V_r = 1.2$ V
- Bit line capacitance: $C_b = 300$ fF
- Bit line precharge voltage is $V_b = 2.4$ V

When a read operation is performed, the reference cell is connected to the complementary bit line. The voltage on the bit line stabilizes at

$$V_b' = \frac{Q_r + Q_b}{C_r + C_b} = \frac{1.2(50) + 2.4(300)}{50 + 300} = 2.23\text{V}$$

At the same time, the memory cell to be read is connected to the true bit line. Depending on the content of the cell, the bit line voltage stabilizes at

$$\text{Logic 1}: \quad V_b' = \frac{Q_c + Q_b}{C_c + C_b} = \frac{2.4(50) + 2.4(300)}{50 + 300} = 2.4\text{V}$$

$$\text{Logic 0}: \quad V_b' = \frac{0(50) + 2.4(300)}{50 + 300} = 2.06\text{V}$$

As shown in Figure 2, there is a linear relation between the stored cell voltage and the sense amplifier voltage. The slope of this linear relation is given by $\frac{2.4-0}{2.4-2.06} = 7.06$. Assuming that the sensitivity of the sense amplifier is given to be ± 50 mV centered around 2.23 V, this gives a sensitivity range of 2.28V $\rightarrow$ 2.18V for the sense amplifier. This means that the voltage sensitivity limits within the cell are $V_{hi} = 7.06(2.28 - 2.06) = 1.55$ V and $V_{lo} = 7.06(2.18 - 2.06) = 0.85$ V. Therefore, leakage currents have to charge up the cell from 0 V to 0.85 V in order to destroy a stored logic 0. Now, assume that it takes $t_{ref} = 60$ ms for this charging up to take place, and that we approximate the charge up process as linear. Then, in order for leakage currents to pull the stored voltage from V_{lo} to V_{hi} (a voltage of 0.7 V), it takes

$$L_{min} = \frac{V_{hi} - V_{lo}}{V_{lo} - \text{GND}} \cdot t_{ref} = \frac{0.7}{0.85} \cdot 60\text{ms} = 50\text{ms}$$

Therefore, a transient fault has a lifetime of about 50 ms or more (i.e., $L \geq 50$ ms). In order to detect a transient fault before it is corrected, it is important to perform a detecting read operation within 50 ms of sensitizing the fault. This condition, however, does not *ensure* detecting transient faults since within the sensitivity region, the sense amplifier may give a correct or an incorrect readout of the stored cell voltage. The following condition ensures that all transient faults are detected.

> To ensure that a transient fault is detected, a detecting read operation should directly be performed after sensitizing each fault.

3 Space of transient faults

This section starts with Section 3.1 where two types of SOS's are identified, detecting and non-detecting. Section 3.2 analyzes the space of all possible single-cell transient FPs. Then, the proposed transient FPs are validated in Section 3.3.

3.1 Types of SOS's

From a testing point of view, transient faults may affect the way detection conditions are constructed, which in turn modifies the resulting memory test. In order to analyze the impact of transient faults on the FP space, we divide SOS's into two types: *detecting* and *non-detecting*. A detecting SOS is a sequence that sensitizes a fault and makes it detectable on the output. A non-detecting SOS is a sequence that only sensitizes the fault but does not forward the fault to the output. This definition can be given in a more formal way, as follows. Let S be the SOS in $<S/F/R>$, where S ends with an operation or state having d as the *expected data* in the victim.

Definition: *If $R = -$ or $R = d$ then S is referred to as a **non-detecting SOS**. Otherwise, if $R \neq -$ and $R \neq d$ then S is referred to as a **detecting SOS**.*

As an example, the deceptive read destructive fault DRDF_1 ($<1r1/0/1>$) describes a fault that is only sensitized within the cell, but not forwarded to the output ($R = d = 1$) [Adams96]. Therefore, the SOS of DRDF_1 is a non-detecting SOS, because $d = 1$, which is the expected data of the $r1$ operation of S. Based on this definition, the impact of transient faults on testing can be described as follows:

- **Non-detecting SOS:** The detection of fault effects sensitized by a non-detecting SOS is done by a read operation, which may be part of the next march element, assuming that the fault effect is *permanent*. In case the fault effect is *transient*, the read operation has to be appended to the SOS, which sensitizes the fault effect. For example, to detect a permanent $\text{DRDF}_1 = \{<1r1/0/1>\}$, it is possible to perform either $\Updownarrow(..., r1, r1, ...)$ or $\Updownarrow(..., r1)\ \Updownarrow(r1, ...)$. To detect a transient $\text{DRDF}_1 = \{<1r1/0_L/1>\}$ then it is necessary to perform $\Updownarrow(..., r1, r1, ...)$.

- **Detecting SOS:** The detection of the fault effect sensitized by a detecting SOS does not require any extra read operation. Because of the fact that the fault is detected by the SOS sensitizing the fault effect, one does not have to distinguish between permanent and transient faults.

3.2 Space of transient FPs

The idea of transient FPs implies that after a fault is sensitized a mechanism results in correcting this faulty behavior before it is detected on the output. An FP has two components to describe a fault: F (the value of the faulty cell) and R (the output on a read operation). The value of R may not be transient, since is sensitized *and* detected on the output at the same time. However, as it has already been shown, it is posible for F to change in such a way that a faulty state would be transformed into a proper state within the cell.

For example, the FP $<1w1/0/->$ represents a non-transition write 1 operation that sets a faulty 0 into the memory cell. Under the assumption that faults are constant in time this FP would remain sensitized until a read operation is performed to detect this fault on the output. Under the assumption of transient FPs, this FP would only remain sensitized for a limited period of time and then the state of the cell gets automatically corrected to its expected value (i.e., logic 1). As a second example, consider the FP $<1r1/1/0>$ that represents a faulty read operation, resulting on an incorrect value on the output. It cannot be transient since the cell is in a correct state and the output is sensitized and detected simultaneously.

Table 1 shows all single-cell static and some single-cell two-operation dynamic FPs [Al-Ars00]. *Static* FPs have an SOS with no performed operations ($S \in \{0, 1\}$, meaning that the state of the victim is specified), or contains one operation ($S \in \{0w0,\ 0w1,\ 1w0,\ 1w1,\ 0r0,\ 1r1\}$). *Dynamic* FPs have an SOS with more than one performed operation. In our case, FPs with the following two-operation SOS's have been analyzed: $S \in \{0w0r0, 1w0r0, 0w1r1, 1w1r1\}$. The FFM column in the table lists the name of the fault model, where an L subscript indicates that the FFM may be transient. The FP column lists the FP of the fault, while the way these faults behave under the assumption of transient faults is listed in 'After time L'. L represents the time needed for the described behavioral change to take place. The 'Comment' column lists whether the fault is transient or not; in case the fault *is* transient, it indicates whether this transient behavior has been observed in the analysis performed in Section 3.3. Note that the transient FPs in the table that describe a read destructive behavior (e.g., $<1r1/0/0>$) do not result in hiding the whole faulty behavior, but only the internal component of it. This does not result in a proper behavior, but results in modifying the fault into a different fault.

3.3 Practical validation

In order for transient faults to take place in practice, there should be a memory mechanism that works against the fail-

Table 1. Transient faults from single-cell static and 2-operation dynamic FPs.

FFM	FP	After time L	Comment	FFM	FP	After time L	Comment
SF_{0L}	$<0/1_L/->$	Proper behavior	Not observed	SF_{1L}	$<1/0_L/->$	Proper behavior	Not observed
WDF_{0L}	$<0w0/1_L/->$	Proper behavior	Observed	WDF_{1L}	$<1w1/0_L/->$	Proper behavior	Observed
$TF\downarrow_L$	$<1w0/1_L/->$	Proper behavior	Observed	$TF\uparrow_L$	$<0w1/0_L/->$	Proper behavior	Observed
IRF_0	$<0r0/0/1>$	No change	Not transient	IRF_1	$<1r1/1/0>$	No change	Not transient
$DRDF_{0L}$	$<0r0/1_L/0>$	Proper behavior	Observed	$DRDF_{1L}$	$<1r1/0_L/1>$	Proper behavior	Observed
RDF_0	$<0r0/1/1>$	$<0r0/0/1>$	Not transient	RDF_1	$<1r1/0/0>$	$<1r1/1/0>$	Not transient
IRF_{00}	$<0w0r0/0/1>$	No change	Not transient	IRF_{11}	$<1w1r1/1/0>$	No change	Not transient
IRF_{10}	$<1w0r0/0/1>$	No change	Not transient	IRF_{01}	$<0w1r1/1_L/0>$	No change	Not transient
RDF_{00}	$<0w0r0/1/1>$	$<0w0r0/0/1>$	Not transient	RDF_{11}	$<1w1r1/0/0>$	$<1w1r1/1/0>$	Not transient
RDF_{10}	$<1w0r0/1/1>$	$<1w0r0/0/1>$	Not transient	RDF_{01}	$<0w1r1/0/0>$	$<0w1r1/1/0>$	Not transient
$DRDF_{00L}$	$<0w0r0/1_L/0>$	Proper behavior	Observed	$DRDF_{11L}$	$<1w1r1/0_L/1>$	Proper behavior	Observed
$DRDF_{01L}$	$<0w1r1/0_L/1>$	Proper behavior	Observed	$DRDF_{10L}$	$<1w0r0/1_L/0>$	Proper behavior	Observed

ure mechanism causing the failure in the first place. One such mechanism is leakage currents, which is known to have a significant impact in DRAMs. The most important DRAM leakage mechanism is leakage through the pass transistor to substrate. Note that the leakage currents of this mechanism always work in one direction, either charging or discharging a memory cell, depending on the type of access transistor being PMOS or NMOS, respectively. Nevertheless, because of using complementary bit lines, leakage currents result in restoring both logic 0 and logic 1 into different cells.

An analysis has been made by simulating the faulty behavior of injected open defects into a memory model to validate which of the proposed transient fault models actually take place. Table 2 gives the count (#) or the number of different defects that result in sensitizing the transient FP in this analysis on the true (BT) and the complementary (BC) bit lines. For example, SF_{0L} has a 0 count (# = 0) on BT and a 0 count on BC, which means that the transient fault SF_{0L} has not been observed in cells connected to BT nor to BC. WDF_{0L} has not been observed in cells on BT (count is 0), while it has been observed in cells on BC as a result of 5 different injected defects (count is 5). Explicitly indicating BT and BC is important because of the bias leakage currents have towards restoring a given voltage level back into the cell. The table shows clearly that specific types of transient FPs take place in cells on BT (those with faulty 1) or on BC (those with faulty 0). In addition the count of both transient faults on BT and on BC is equal, since transient FP instances on BC are the complementary of those on BT (they are caused by complementary defects). Note that although it is theoretically possible for state faults (SF_0 and SF_1) to be transient, this behavior has not been observed.

Table 2. Transient FFMs observed by simulation.

FFM	# on BT	# on BC	FFM	# on BT	# on BC
SF_{0L}	0	0	SF_{1L}	0	0
WDF_{0L}	0	5	WDF_{1L}	5	0
$TF\downarrow_L$	0	9	$TF\uparrow_L$	9	0
$DRDF_{0L}$	0	5	$DRDF_{1L}$	5	0
$DRDF_{00L}$	0	3	$DRDF_{11L}$	3	0
$DRDF_{01L}$	0	6	$DRDF_{10L}$	6	0

In addition, static and dynamic incorrect read faults (IRF_x and IRF_{xy}) and read destructive faults (RDF_x and RDF_{xy}) are not given in the table since they cannot be transient.

4 Impact on tests

Memory testing assumes that a sensitized FFM remains sensitized unless an action has been taken that eliminates the fault. In the specific case of DRAMs, where leakage currents play a significant role, testing assumes that FFMs are always sensitized as strong faults such that the fault remains sensitized by memory refresh until a read operation detects the sensitized FFM. This assumption does not hold for transient faults, which need specific detection conditions to ensure their detection.

Only those transient faults that have a non-detecting SOS need special action to detect them. Table 3 lists all analyzed single-cell transient and non-transient faults and gives the needed detection conditions that ensure their detection. Note that, in case of a transient fault, the detection

Table 3. Detection conditions for analyzed FPs.

FFM	FP	Condition
SF_{0L}	$< 0/1_L/- >$	$\Updownarrow(..., w0, r0, ...)$
SF_{1L}	$< 1/0_L/- >$	$\Updownarrow(..., w1, r1, ...)$
WDF_{0L}	$< 0w0/1_L/- >$	$\Updownarrow(...0, w0, r0, ...)$
WDF_{1L}	$< 1w1/0_L/- >$	$\Updownarrow(...1, w1, r1, ...)$
$TF\downarrow_L$	$< 1w0/1_L/- >$	$\Updownarrow(...1, w0, r0, ...)$
$TF\uparrow_L$	$< 0w1/0_L/- >$	$\Updownarrow(...0, w1, r1, ...)$
IRF_0	$< 0r0/0/1 >$	$\Updownarrow(...0, r0, ...)$, or $\Updownarrow(...0)\ \Updownarrow(r0, ...)$
IRF_1	$< 1r1/1/0 >$	$\Updownarrow(...1, r1, ...)$, or $\Updownarrow(...1)\ \Updownarrow(r1, ...)$
$DRDF_{0L}$	$< 0r0/1_L/0 >$	$\Updownarrow(...0, r0, r0, ...)$
$DRDF_{1L}$	$< 1r1/0_L/1 >$	$\Updownarrow(...1, r1, r1, ...)$
RDF_0	$< 0r0/1/1 >$	$\Updownarrow(...0, r0, ...)$, or $\Updownarrow(...0)\ \Updownarrow(r0, ...)$
RDF_1	$< 1r1/0/0 >$	$\Updownarrow(...1, r1, ...)$, or $\Updownarrow(...1)\ \Updownarrow(r1, ...)$
IRF_{xy}	$< xwyry/y/x >$	$\Updownarrow(...x, wy, ry, ...)$, or $\Updownarrow(...x, wy)\ \Updownarrow(ry, ...)$
RDF_{xy}	$< xwyry/x/x >$	$\Updownarrow(...x, wy, ry, ...)$, or $\Updownarrow(...x, wy)\ \Updownarrow(ry, ...)$
$DRDF_{00L}$	$< 0w0r0/1_L/0 >$	$\Updownarrow(...0, w0, r0, r0, ...)$
$DRDF_{11L}$	$< 1w1r1/0_L/1 >$	$\Updownarrow(...1, w1, r1, r1, ...)$
$DRDF_{01L}$	$< 0w1r1/0_L/1 >$	$\Updownarrow(...0, w1, r1, r1, ...)$
$DRDF_{10L}$	$< 1w0r0/1_L/0 >$	$\Updownarrow(...1, w0, r0, r0, ...)$

conditions always contain a read operation directly after sensitizing the fault. In case of a non-transient fault, two detection conditions are possible: one with a read operation directly after sensitizing the fault, and one with a read operation in the following march element. For example, the detection condition of the transient up-transition fault $TF\uparrow_L$ is $\Updownarrow(...0, w1, r1, ...)$. The symbol $\Updownarrow$ indicates that the memory can be accessed in an increasing or decreasing address order. The symbol ...0 means that the cell to be accessed should contain a 0 (usually from a preceding write operation). Then, a transition write ($w1$) operation should be performed to sensitize the fault, which is followed directly by a read operation to detect the fault.

A test that satisfies all conditions of Table 3 is:

March T = $\{\Updownarrow(w0, w0, r0, r0); \Updownarrow(w1, r1, r1); \Updownarrow(w0, r0, r0); \Updownarrow(w1, w1, r1, r1)\}$

March T has four march elements, each of which performs either a transition or a non-transition write operation as required in Table 3. Furthermore, each march element contains two read operations to sensitize and then detect deceptive read destructive faults. In addition to transient FPs, March T detects the non-transient forms of the targeted FPs, since transient FPs need more restrictive detection conditions for their detection than non-transient FPs.

5 Conclusions

In this paper, the new class of transient faults has been presented, where the time between sensitizing and detecting the fault plays an important role in testing. A quantitative analysis of transient faults has been made whereby the lifetime of the fault has been calculated. The paper also analyzed the space of transient faults and validated their existence in commercial DRAMs using simulation. The impact of transient faults on testing has been discussed and a test to detect them has been given.

References

[Adams96] R.D. Adams and E.S. Cooley. "Analysis of a Deceptive Destructive Read Memory Fault Model and Recommended Testing." *in Proc. IEEE North Atlantic Test Workshop*. 1996.

[Adler95] E. Adler *et al.*, "The Evolution of IBM CMOS DRAM Technology," *in IBM J. of Research and Development*, vol. 39, no. 1–2, 1995, pp. 167–188.

[Al-Ars99] Z. Al-Ars. *Analysis of the Space of Functional Fault Models and Its Application to Embedded DRAMs*. Technical Report no. 1-68340-28(1999)-07, CARDIT, Delft Univ. of Technology, Delft, The Netherlands, 1999.

[Al-Ars00] Z. Al-Ars and A.J. van de Goor, "Impact of Memory Cell Array Bridges on the Faulty Behavior in Embedded DRAMs," *in Proc. Asian Test Symp.*, 2000, pp. 282–289.

[Dekker90] R. Dekker *et al.*, "A Realistic Fault Model and Test Algorithms for Static Random Access Memories," *in IEEE Trans. on Computers*, vol. C-9, no. 6, 1990, pp. 567–572.

[Dietl90] J. Dietl *et al.*, "Buried Stacked Capacitor Cells for 16M and 64M DRAMs," *in Proc. European Solid State Device Research Conf.*, 1990, pp. 465–468.

[Hanafi98] H.I. Hanafi *et al.*, "Data Retention in SOI-DRAM with Trench Capacitor Cell," *in Proc. European Solid State Device Research Conf.*, 1998, pp. 276–279.

[Romanenko98] A.Y. Romanenko and W.M. Gosney, "A Numerical Analysis of the Storage Times of Dynamic Random-Access Memory Cells Incorporating Ultrathin Dielectrics," *in IEEE Trans. on Electron Devices*, vol. 45, no. 1, 1998, pp. 218–223.

[Sarpeshkar91] R. Sarpeshkar *et al.*, "Mismatch Sensitivity of a Simultaneously Latched CMOS Sense Amplifier," *in IEEE J. of Solid-State Circuits*, vol. 26, no. 10, 1991, pp. 1413–1422.

[vdGoor98] A.J. van de Goor, *Testing Semiconductor Memories, Theory and Practice*. ComTex Publishing, Gouda, The Netherlands, 1998, http://ce.et.tudelft.nl/~vdgoor/

[vdGoor00] A.J. van de Goor and Z. Al-Ars, "Functional Memory Faults: A Formal Notation and a Taxonomy," *in Proc. IEEE VLSI Test Symp.*, 2000, pp. 281–289.