

Detecting Unique Faults in Multi-Port SRAMs

Said Hamdioui^{1,2} Ad J. van de Goor² David Eastwick¹ Mike Rodgers¹

¹Intel Corporation, 2200 Mission College Boulevard, Santa Clara, CA 95052

²Delft University of Technology, Faculty of Information Technology and Systems
Section of Computer Engineering, Mekelweg 4, 2628 CD Delft, The Netherlands

E-mail: said@ce.et.tudelft.nl

Abstract: *This paper begins with a brief overview of realistic fault models for multi-port SRAMs with p ports, divided into p classes: single-port faults, two-port faults, ..., p -port faults. Except for single-port faults, all other fault classes cannot be detected with the conventional (single-port) memory tests; they require special tests. Next, the paper presents a set of three linear single-addressing tests for unique multi-port memory faults ($p > 2$) that will be merged into a single test.*

1 Introduction

Most of the published work on memory testing concentrated on *single-port (SP)* memories [1, 2, 3, 7, 14]. Testing of *multi-port (MP)* memories requires special tests since the multiple and simultaneous access can sensitize faults that are different from the conventional SP memory faults. In spite of their growing use, little work has been published on testing MP memories. In addition, most of the published work concentrated only on MP memories with two ports (i.e., two-port (2P) memories). In [13], an *ad hoc* test with no specific fault model was described. In [11], a BIST circuit, based on a serial interfacing technique for embedded 2P memories, was reported. For the same fault models, modified march tests and BIST circuits were reported in [10, 16, 17]. In [4, 12, 15] *theoretical* fault models, together with their tests were developed. However, the introduced fault models are *not* based on any experimental/industrial analysis. In addition, the proposed tests have a time complexity which is exponential in the number of ports of the MP memory; that makes them impractical. In [5], port interferences in 2P memories were *experimentally* analyzed, based on an industrial design and SPICE simulation; however, the analysis was restricted to only the interference between the two ports. A similar, but theoretical work, has been reported in [18].

In our previous work [6, 9], an experimental analysis of all possible spot defects in 2P memories has been done; realistic fault models (based on defect injection

and circuit simulation), together with linear efficient tests have been introduced; the industrial evaluation of these tests shows that they are indispensable for obtaining an industrial quality level of fault coverage [9]. However, this analysis has only been restricted to 2P memories. This paper will extend the previous work to any p -port memory. It is organized as follows: Section 2 gives a brief overview of realistic fault models for p -port memory, as established by [8]. Section 3 derives optimal march tests for such faults; while Section 4 ends with conclusions.

2 Fault Models for p P-SRAMs

Functional Fault Models (FFMs) for p P-SRAMs are given in detail in [8]; they are derived based on defect injection and circuit simulation. In this section a brief overview will be given; for more detail see [8].

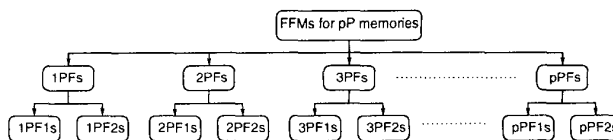


Figure 1: Classification of FFMs for p P memories

The FFMs for any MP memory can be divided into p -classes: single-port faults (1PFs), two-port faults (2PFs), three-port faults (3PFs), ..., p -port faults (p PFs); see Figure 1. The 1PFs are faults that can be sensitized using SP operations; they are divided into 1PFs involving a *single cell* (1PF1s) and 1PFs involving *two cells* (1PF2s). The 2PFs are faults that can not be sensitized using SP operations; they require the use of the two ports of the memory *simultaneously*. They are also divided into 2PFs involving a *single cell* (2PF1s) and 2PFs involving *two cells* (2PF2s). The 3PFs are faults that can not be sensitized using SP operations, neither using 2P operations; they require the use of the three ports of the memory *simultaneously*. The 3PFs can be also divided into 3PFs involving a *sin-*

gle cell (*3PF1s*) and 3PFs involving *two cells (3PF2s)*. A similar explanation applies to *pPFs*.

A detail description of each class is given in [8]. In the following, only a brief description of 3PFs will be given. However, first a notation of MP faults will be presented.

2.1 Notation of MP faults

In order to represent MP faults (e.g., three-port faults), the following terminology will be (re)introduced [12, 4]:

- *Strong fault*: This is a memory fault that can be **fully sensitized** by an operation; e.g., an SP write or read operation fails, two simultaneous read operations fail, etc. That means that the state of the v-cell is incorrectly changed, can not be changed, or that the sense amplifier(s) return(s) an incorrect result(s).
- *Weak fault*: This is a fault which is **partially sensitized** by an operation; e.g., due to a defect that creates a small disturbance of the voltage of the true node of the cell. However, a fault can be *fully sensitized* (i.e., becomes strong) when two (or more) weak faults are sensitized simultaneously, since their fault effects can be additive. This may occur when a MP operation is applied.

The terminology of weak and strong faults is used in representing the MP FFMs as follows:

- F denotes a *strong fault* F , while wF denotes the *weak fault* F . For example, RDF denotes a strong Read Destructive Fault, while $wRDF$ denotes a weak Read Destructive Fault.
- $\langle fault_1 \rangle \& \langle fault_2 \rangle \dots \& \langle fault_p \rangle$: denotes a *pPF* consisting of p weak faults; '&' denotes the fact that the p faults *in parallel* (i.e., simultaneously) form the p -port fault (*pPF*). E.g., the $wRDF\&wRDF\&wRDF$ denote a 3PF based on three weak RDFs.

2.2 Three-port faults

Three-port faults (3PFs) are divided into two subclasses; see Figure 2.

1. *The 3PFs involving a single cell (3PF1s)*: They are based on a combination of three SP operations applied simultaneously via three ports to a single cell, which is the same as the v-cell.

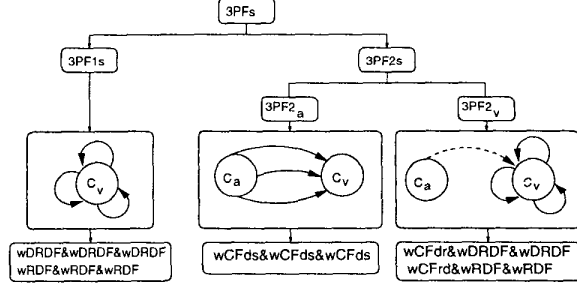


Figure 2: Classification and taxonomy of 3PFs

2. *The 3PFs involving two cells (3PF2s)*: Depending to which cells the three simultaneous operations are applied (to the a-cell or to the v-cell), the 3PF2s are further divided into two types:

- (a) The $3PF2_a$: this fault is sensitized in the v-cell c_v by applying three simultaneous operations to the same a-cell c_a .
- (b) The $3PF2_v$: this fault is sensitized in v-cell by first putting the a-cell in a certain state (dashed arrow in Figure 2), and thereafter applying three simultaneous operations to the v-cell (solid arrows in the figure).

A taxonomy of all 3PFs is also given in Figure 2. In the table:

- RDF: denotes *Read Destructive Fault* [2].
- DRDF: *Deceptive Read Destructive Fault* [2].
- CF_{ds} : *Disturb Coupling Fault*.
- CF_{dr} : *Deceptive Read Destructive Coupling Fault*.
- CF_{dr} : *Read Destructive Coupling Fault* (CF_{rd}).

Table 1 lists the FFMs together with the *Fault Primitives (FPs)* they consist of, whereby a FP is a compact notation describing the fault. They are explained below.

2.2.1 The 3PF1 fault subclass

To describe the 3PF1s, the following fault primitive (FP) notation will be used: $\langle S1 : S2 : S3/F/R \rangle_v$. It denotes a three-port FP involving a single cell (v-cell). This FP requires the use of the three ports *simultaneously*. $S1$, $S2$, and $S3$ describe the sensitizing operations of the cell; “:” denotes the fact that $S1$, $S2$ and $S3$ are applied *simultaneously* through the three ports. $S_i \in \{w0, w1, w \uparrow, w \downarrow, r0, r1\}$, whereby 0 denotes a zero value, 1 denotes a one value, $w0$ ($w1$) denotes a write 0 (1) operation, $w \uparrow$ ($w \downarrow$) denotes an up (down)

transition write operation, $r0$ ($r1$) denotes a read 0 (1) operation.

F describes the value of the *faulty* cell (v-cell); $F \in \{0, 1, \uparrow, \downarrow, ?\}$, whereby \uparrow (\downarrow) denotes an up (down) transition, and $?$ denotes an undefined logical value.

R is the read result of $S1$, $S2$ and $S3$ in the case they are the *same* read operation (i.e., ' $r0 : r0 : r0$ ' or ' $r1 : r1 : r1$ '). In the case one of the read operations returns the expected value, while the others return wrong values, then the wrong value is considered in R . $R \in \{0, 1, ?, -\}$, whereby $?$ denotes a random logical value. A random logical value can occur if the voltage difference between the bit lines (used by the sense amplifier) is very small. A '-' in R means that the output data is not applicable in that case; e.g., if $S = w0$, then no data will appear at the memory output, and therefore R is replaced by '-'.

The 3PF1 consists of two FFMs [6, 8], each with four FPs; see Table 1 and Figure 2:

1. $wDRDF&wDRDF&wDRDF$: Applying three simultaneous read operations to the v-cell causes the v-cell to flip; and the sense amplifiers return *correct values*.
2. $wRDF&wRDF&wRDF$: Applying three simultaneous read operations to the v-cell causes the v-cell to flip; and the sense amplifiers return *incorrect values*.

2.2.2 The 3PF2 fault subclass

The 3PF2s are divided into two types (see Figure 2): the 3PF2_a and the 3PF2_v.

The 3PF2_a: To denote this fault, the following FP notation is used: $\langle S1_a : S2_a : S3_a; S_v/F/R \rangle_{a,v}$. It denotes an FP whereby the three sensitizing operations, $S1_a$, $S2_a$ and $S3_a$ are applied simultaneously to the a-cell. S_v denotes the state of the v-cell; i.e., $S_v \in \{0, 1\}$. F denotes the value of the faulty cell c_v . Note that in that case R will be replaced with '-' since S_v can not be a read operation.

The 3PF2_a consists of one FFM: $wCF_{d_s}&wCF_{d_s}&wCF_{d_s}$, with eight FPs (see Table 1): applying three simultaneous operations to the a-cell will cause the v-cell to flip. Note that, e.g. the $\langle w0 : rd:rd; 1/ \downarrow /- \rangle$ denotes only one FP since the read values are irrelevant (d =don't care); the read operations are used to sensitize the fault. Note also that $\langle rx : rx : rx; 0/ \uparrow /- \rangle$ denotes two FPs since $x \in \{0, 1\}$.

The 2PF2_v: To denote this fault, the following FP notation is used: $\langle S_a; S1_v : S2_v : S3_v/F/R \rangle_{a,v}$. It denotes an FP whereby the three sensitizing operations, $S1_v$, $S2_v$, and $S3_v$, are applied simultaneously to the v-cell. S_a describes the state of the a-cell; i.e., $S_a \in \{0, 1\}$.

The 3PF2_v consists of two FFMs, each with two FPs; see Figure 2 and Table 1.

1. $wCF_{d_r}&wDRDF&wDRDF$: Applying three simultaneous read operations to the v-cell will cause the v-cell to flip if the a-cell is in a certain state. The read operations return *correct values*.
2. $wCF_{r_d}&wRDF&wRDF$: Applying three simultaneous read operations to the v-cell will cause the v-cell to flip if the a-cell is in a certain state. The read operations return *incorrect values*.

Table 1: List of 3PFs; $x \in \{0, 1\}$ and $d =$ don't care

FFM	Fault primitives
$wDRDF&wDRDF&wDRDF$	$\langle r0 : r0 : r0/ \uparrow /0 \rangle$, $\langle r1 : r1 : r1/ \downarrow /1 \rangle$
$wRDF&wRDF&wRDF$	$\langle r0 : r0 : r0/ \uparrow /1 \rangle$, $\langle r1 : r1 : r1/ \downarrow /0 \rangle$
$wCF_{d_s}&wCF_{d_s}&wCF_{d_s}$	$\langle w0 : rd : rd; 0/ \uparrow /- \rangle$, $\langle w0 : rd : rd; 1/ \downarrow /- \rangle$, $\langle w1 : rd : rd; 0/ \uparrow /- \rangle$, $\langle w1 : rd : rd; 1/ \downarrow /- \rangle$, $\langle rx : rx : rx; 0/ \uparrow /- \rangle$, $\langle rx : rx : rx; 1/ \downarrow /- \rangle$
$wCF_{d_r}&wDRDF&wDRDF$	$\langle 0; r0 : r0 : r0/ \uparrow /0 \rangle$, $\langle 0; r1 : r1 : r1/ \downarrow /1 \rangle$, $\langle 1; r0 : r0 : r0/ \uparrow /0 \rangle$, $\langle 1; r1 : r1 : r1/ \downarrow /1 \rangle$
$wCF_{r_d}&wRDF&wRDF$	$\langle 0; r0 : r0 : r0/ \uparrow /1 \rangle$, $\langle 0; r1 : r1 : r1/ \downarrow /0 \rangle$, $\langle 1; r0 : r0 : r0/ \uparrow /1 \rangle$, $\langle 1; r1 : r1 : r1/ \downarrow /0 \rangle$

3 Tests for p -port SRAMs

This section presents first tests for 3PFs. Thereafter, the tests will be extended for p PFs. However, first the march notation used for SP tests will be extended in order to specify MP tests.

3.1 Notation for March tests

The extension will be done as follows:

- A complete march test is delimited by the '{...}' bracket pair; while a march element is delimited by the '(...)' bracket pair. The march elements are separated by semicolons, and the operations within a march element are separated by commas.

- The operations applied in parallel to the ports are separated using colons, and the port number to which each of the parallel operations is applied is determined

implicitly. For example, the march element $(r0 : w1)$ denotes two simultaneous operations: a $r0$ operation applied to the first port (P_a), and a $w1$ operation applied to the second port (P_b). Port numbers can also be specified explicitly, by super-scripting the operation with the corresponding port number; e.g., $r0^a$ denotes that a $r0$ operation is applied to P_a .

- The character 'n' denotes *no operation*, while the character '-' denotes *any allowed operation*. For example, $(r0 : n)$ denotes a $r0$ operation via P_a , and no operation on P_b .

- \uparrow : denotes an up addressing (\uparrow), or a down addressing (\downarrow) sequence.

3.2 Tests for three-port faults

The FFMs for 3P memories are divided into 1PFs, 2PFs and 3PFs. Therefore, the test procedure may be divided into three parts:

1. Test(s) to detect 1PFs, for these tests see [1, 3, 7, 14].
2. Test(s) to detect 2PFs, for these tests see [6, 9].
3. Test(s) to detect 3PFs. Below, tests for detecting 3PFs will be developed.

3.2.1 Tests for the 3PF1s

The test shown in Figure 3, referred as *March 3PF1*, detects all 3PF1 faults; it has a test length of $6n$. The first three simultaneous read operations, through the three ports in each march element, sensitize and detect the $wRDF\&wRDF\&wRDF$ faults, and sensitize the $wDRDF\&wDRDF\&wDRDF$ faults; the latter will be detected by the second single read operations (see also Table 1).

$$\left\{ \begin{array}{l} \uparrow (w0 : n : n) ; \uparrow (r0 : r0 : r0, r0 : - : -) ; \\ \quad \quad \quad M_0 \quad \quad \quad M_1 \\ \uparrow (w1 : - : -) ; \uparrow (r1 : r1 : r1, r1 : - : -) \end{array} \right\}$$

$M_2 \quad \quad \quad M_3$

Figure 3: March 3PF1

3.2.2 Tests for the 3PF2s

The 3PF2s are divided into two types: $3PF2_a$ and $3PF2_v$; see Figure 2.

Tests for the $3PF2_a$ faults

An optimal test detecting all $3PF2_a$ faults is given in Figure 4, and referred as *March 3PF2_a-* ('-' is added to denote the optimal version of March 3PF2_a [8]). It

has a test length of $10n$. The $3PF2_a$ faults consists of one FFM, with eight FPs; see Figure 2 and Table 1.

$$\left\{ \begin{array}{l} \downarrow (w0 : n : n) ; \uparrow (r0 : r0 : r0, w1 : r0 : r0) ; \\ \quad \quad \quad M_0 \quad \quad \quad M_1 \\ \uparrow (r1 : r1 : r1, w0 : r1 : r1) ; \downarrow (r0 : r0 : r0, w1 : r0 : r0) ; \\ \quad \quad \quad M_2 \quad \quad \quad M_3 \\ \downarrow (r1 : r1 : r1, w0 : r1 : r1) ; \downarrow (r0 : - : -) \end{array} \right\}$$

$M_4 \quad \quad \quad M_5$

Figure 4: March 3PF2_a-

- The $\langle r0 : r0 : r0; 0 / \uparrow / - \rangle_{a,v}$ and the $\langle w1 : rd : rd; 0 / \uparrow / - \rangle_{a,v}$ will be sensitized and detected by M_1 if the v-cell has a higher address than the a-cell; i.e., $v > a$. If $v < a$, then these faults will be sensitized and detected by M_3 .

- The $\langle r1 : r1 : r1; 1 / \downarrow / - \rangle_{a,v}$ and the $\langle w0 : rd : rd; 1 / \downarrow / - \rangle_{a,v}$ will be sensitized and detected by M_2 if $v > a$. If $v < a$, then these faults will be sensitized and detected by M_4 .

- The $\langle r0 : r0 : r0; 1 / \downarrow / - \rangle_{a,v}$ and the $\langle w1 : rd : rd; 1 / \downarrow / - \rangle_{a,v}$ will be sensitized by M_1 and detected by M_2 if $v < a$; while the same faults will be sensitized by M_3 and detected by M_4 if $v > a$.

- The $\langle r1 : r1 : r1; 0 / \uparrow / - \rangle_{a,v}$ and the $\langle w0 : rd : rd; 0 / \uparrow / - \rangle_{a,v}$ will be sensitized by M_2 and detected by M_3 if $v < a$; while the same faults will be sensitized by M_4 and detected by M_5 if $v > a$.

Tests for the $3PF2_v$ faults

An optimal test detecting all $3PF2_v$ faults is shown in Figure 5, and referred as *March 3PF2_v-*; it has a test length of $13n$.

$$\left\{ \begin{array}{l} \downarrow (w0 : n : n) ; \\ \quad \quad \quad M_0 \\ \uparrow (r0 : r0 : r0, r0 : - : -, w1 : - : -) ; \\ \quad \quad \quad M_1 \\ \uparrow (r1 : r1 : r1, r1 : - : -, w0 : - : -) ; \\ \quad \quad \quad M_2 \\ \downarrow (r0 : r0 : r0, r0 : - : -, w1 : - : -) ; \\ \quad \quad \quad M_3 \\ \downarrow (r1 : r1 : r1, r1 : - : -, w0 : - : -) \end{array} \right\}$$

M_4

Figure 5: March 3PF2_v-

March 3PF2_v- detects all $3PF2_v$ faults. Table 2 shows the operations performed on two cells c_i and c_j by march elements of Figure 5. The table contains a column 'State' which identifies the state $S_{i,j}$ of the two cells (c_i, c_j) before the operation is performed, and a column 'State $S_{i,j}$ ' which identifies the state after the operation. The table shows that all states of (c_i, c_j) (i.e., 00, 01, 11, 10) are generated, and in each

state three simultaneous read operations followed by (at least) a single read operation are applied to cell c_i and c_j . The three simultaneous read operations sensitize and detect $wCF_{rd}\&wRDF\&wRDF$, and sensitize $wCF_{dr}\&wDRDF\&wDRDF$. The latter will be detected by the followed single read operations (see Table 1).

Table 2: State table for detecting $3PF2_v$ faults

Step	March element	State	Operation	State $S_{i,j}$
1	M_0	--	'w0 : n : n' to c_i	0-
2		0-	'w0 : n : n' to c_j	00
3	M_1	00	'r0 : r0 : r0' to c_i	00
4		00	'r0 : - : -' to c_i	00
5		00	'w1 : - : -' to c_i	10
6		10	'r0 : r0 : r0' to c_j	10
7		10	'r0 : - : -' to c_j	10
8		10	'w1 : - : -' to c_j	11
9	M_2	11	'r1 : r1 : r1' to c_i	11
10		11	'r1 : - : -' to c_i	11
11		11	'w0 : - : -' to c_i	01
12		01	'r1 : r1 : r1' to c_j	01
13		01	'r1 : - : -' to c_j	01
14		01	'w0 : - : -' to c_j	00
15	M_3	00	'r0 : r0 : r0' to c_j	00
16		00	'r0 : - : -' to c_j	00
17		00	'w1 : - : -' to c_j	01
18		01	'r0 : r0 : r0' to c_i	01
19		01	'r0 : - : -' to c_i	01
20		01	'w1 : - : -' to c_i	11
21	M_4	11	'r1 : r1 : r1' to c_j	11
22		11	'r1 : - : -' to c_j	11
23		11	'w0 : - : -' to c_j	10
24		10	'r1 : r1 : r1' to c_i	10
25		10	'r1 : - : -' to c_i	10
26		10	'w0 : - : -' to c_i	00

3.2.3 Test for all 3PFs

By inspecting the three introduced tests, March 3PF1, March 3PF2_a- and March 3PF2_v-, we can see that all these tests are *single-addressing tests*; i.e., they access one cell at a time. This property makes it easy to merge the three tests into a single test. The result is shown in Figure 6, and referred as *March s3PF-* ('s' stands for single-addressing). March s3PF- detects all 3PF1s, all 3PF2_{as} and all 3PF2_{vs} [8]. It has a test length of $14n$; while the test lengths of March 3PF1, March 3PF2_a- and March 3PF2_v- are $6n$, $10n$, and $13n$, respectively. Therefore, in order to detect 3PF1, 3PF2_a and 3PF2_v faults, one can use March s3PF- instead of testing these faults separately. This will reduce the total test length from $6n + 10n + 13n = 29n$ to $14n$.

It should be noted that for March s3PF-, it is assumed that two simultaneous reads and a write of the same location (with the read data discarded) is allowed. If this is not the case, then all operations 'wx:ry:ry' in Figure 6 should be replaced with 'wx : n : n'; whereby $x, y \in \{0, 1\}$.

{	\uparrow	(w0 : n : n)	;
		M_0	
	\uparrow	(r0 : r0 : r0, r0 : - : -, w1 : r0 : r0)	;
		M_1	
	\uparrow	(r1 : r1 : r1, r1 : - : -, w0 : r1 : r1)	;
		M_2	
	\downarrow	(r0 : r0 : r0, r0 : - : -, w1 : r0 : r0)	;
		M_3	
	\downarrow	(r1 : r1 : r1, r1 : - : -, w0 : r1 : r1)	;
		M_4	
	\downarrow	(r0 : - : -)	}
		M_5	

Figure 6: March s3PF-

3.3 Tests for pPFs

In a similar way as that followed for 3PFs, the tests can be introduced for any MP memory with p ports. Since the FFMs for pP memories are divided into p classes, the test procedure may be divided into p parts:

1. Test(s) to detect 1PFs.
2. Test(s) to detect 2PFs.
-
- p . Test(s) to detect p PFs.

In order to save space, only the optimal test detecting all p PFs (i.e., p PF1s and p PF2s) will be given. The test, referred as *March spPF-* [8], is given in Figure 7. It has a test length of $14n$, which is the same as that of March s3PF-. Note that March spPF- is exactly an extension of March s3PF-; this is due to the nature of p PFs, which are extensions of 3PFs. In Figure 7, e.g., 'r0^a' denotes a r0 operation via port P_a .

{	\uparrow	(w0 ^a : n ^b : ... : n ^p)	;
		M_0	
	\uparrow	(r0 ^a : r0 ^b : ... : r0 ^{p}, r0^a : -^b : ... : -^{p}, w1^a : r0^b : ... : r0^{p}}}}	;
		M_1	
	\uparrow	(r1 ^a : r1 ^b : ... : r1 ^{p}, r1^a : -^b : ... : -^{p}, w0^a : r1^b : ... : r1^{p}}}}	;
		M_2	
	\downarrow	(r0 ^a : r0 ^b : ... : r0 ^{p}, r0^a : -^b : ... : -^{p}, w1^a : r0^b : ... : r0^{p}}}}	;
		M_3	
	\downarrow	(r1 ^a : r1 ^b : ... : r1 ^{p}, r1^a : -^b : ... : -^{p}, w0^a : r1^b : ... : r1^{p}}}}	;
		M_4	
	\downarrow	(r0 ^a : - ^b : ... : - ^{p}}	}
		M_5	

Figure 7: March spPF-

4 Conclusions

In this paper realistic fault models for p -port SRAMs have been presented; they are divided into p classes: single-port fault, two-port faults, ..., p -port faults. Thereafter, linear tests for p PFs ($p \geq 3$) has been introduced. The results show that each class of the p fault classes can be detected with a linear march test having

a test length of $14n$ (n is the size of the memory). This is very attractive industrially.

Acknowledgment

We express our gratitude to David Eastwick, Mike Rodgers, Mike Spica, and Greg Tollefson from Intel corporation for giving us the opportunity to perform this research at Intel Corporation, Santa Clara, USA, using real Intel multi-port SRAM designs and tools. We also thank them for their helpful comments and suggestions.

References

- [1] M.S. Abadir and J.K. Raghbati, "Functional Testing of Semiconductor Random Access Memories", *ACM Computer Surveys*, 15(3), pp. 175-198, 1983.
- [2] R.D. Adams, "Extension of Static Random Access Memories, Modeling and Examination of Pattern for Fault Detection", Master of Science thesis, Tayer School of Engineering, Darmouth College, Darmouth, USA, May 1991.
- [3] R. Dekker, F. Beenker, and H. Tijssen, "A Realistic Fault Models and Test Algorithms for Static random Access Memories", *IEEE Trans. on CAD*, Vol. 9, No. 6, pp. 567-572, June 1990.
- [4] S. Hamdioui, and A.J. van de Goor, "Consequences of Port Restrictions on Testing Two-Port Memories", *In Proc. of Int. Test Conference ITC'98*, pp. 63-72, Oct. 1998.
- [5] S. Hamdioui, and A.J. van de Goor, "Port Interference Faults in Two-Port Memories", *In Proc. of Int. Test Conference ITC'99*, pp. 1001-1010, Sep. 1999.
- [6] S. Hamdioui, A.J. van de Goor, Mike Rodgers, and David Eastwick, "March Tests for Realistic Faults in Two-port Memories," *Rec. of Int. Workshop on Memory Technology, Design and Testing*, pp. 73-78, 2000.
- [7] S. Hamdioui, and A.J. van de Goor, "An Experimental Analysis of Spot Defects in SRAMs: Realistic Fault Models and Tests", *In Proc. of the Ninth Asian Test Symposium*, pp. 131-138, 2000.
- [8] S. Hamdioui, A.J. van de Goor, Mike Rodgers, and David Eastwick, "Realistic Fault Models and Test Procedure for Multi-Port SRAMs," *Rec. of Int. Workshop on Memory Technology, Design and Testing*, pp. 65-72, 2001.
- [9] S. Hamdioui, A.J. van de Goor, Mike Rodgers, and David Eastwick, "Efficient tests for Realistic Faults in Dual-Port SRAMs" *To Appear in IEEE Trans. on Computers*.
- [10] T. Matsumura, "An efficient Test Method for Embedded Multi-Port RAM with BIST circuitry", *Rec. of the Int. Workshop on Memory Technology, Design and Testing*, pp. 62-67, 1995.
- [11] B. Nadeau-Dostie, A. Sulburt and V.K. Agrawal, "Serial Interfacing for Embedded Memory Testing", *IEEE Design and Test of Computers*, 7(2), pp. 52-63, 1990.
- [12] M. Nicolaidis, V.C. Alves and H. Bederr, "Testing Complex Coupling Faults in Multi-Port Memories", *IEEE Transactions on VLSI Systems*, 3(1), pp. 59-71, March 1995.
- [13] M.J. Raposa, "Dual Port Static RAM Testing", *In Proc. IEEE International Test Conference*, pp. 362-368, 1988.
- [14] A.J. van de Goor, "Testing Semiconductor Memories, Theory and Practice", *ComTex Publishing, Gouda, The Netherlands*, 1998. Web: <http://ce.et.tudelft.nl/~vdgoor>
- [15] A.J. van de Goor, and S. Hamdioui, "Fault Models and Tests for Two-Port Memories", *In Proc. of 16th IEEE VLSI Test Symposium*, pp. 401-410, Monterey, CA., USA, April 1998.
- [16] S.W. Wood, *et.al.*, "A 5Gb/s 9-Port Application Specific SRAM with Built-in Self-Test", *Records of the 1995 IEEE Int. Workshop on Memory Technology, Design and Testing*, San Jose, CA., pp. 78-73, 1995.
- [17] Y. Wu and S. Gupta, "Built-In Self Testing for Multi-Port RAMs", *In Proc. of the sixth Asian Test Symposium*, pp. 398-403, 1997.
- [18] J. Zhao, S. Irrinki, M. Puri, and F. Lombardi, "Detection of Inter-Port Faults in Multi-Port Static RAMs", *In Proc. of VLSI Test Symposium*, Montreal, Canada, pp. 297-302, 2000.