Comparitive BTI Analysis in Nano-scale Circuits Lifetime

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Abstract. As semiconductor manufacturing has entered into the nanoscale era, Bias Temperature Instability (BTI) has become one of the most significant aging mechanisms leading to reliability issues. This paper presents ReverseAge, a technique that detects delay due to NBTI and utilizes design timing margins to ensure reliable circuit operation. First, it presents a scheme to detect the NBTI induced delay. Second, it presents a technique to tolerate the errors; the technique exploits the available design timing margins to compensate for the NBTI induced delay. The evaluation of ReverseAge has been performed by integrating it in an ISCAS-89 benchmark circuit. The simulation results show 3× reliability improvements with respect to state-of-the-art. The improvement comes at the cost of 3.77% area and 1.4% power overheads.

1 Introduction

With the relentless downscaling of CMOS technology, the reliability issues as well as the variability issues of transistors have become constraint of IC performance and lifetime [1]. Amongst the reliability issues bias temperature instability (BTI) -NBTI in PMOS transistors and PBTI in NMOS transistors- has drawn particular attention [2]. NBTI/PBTI degrade the performance of PMOS/NMOS transistors under a negative/positive gate stresses at elevated temperature [3, 4]. The effects of NBTI/PBTI on a PMOS/NMOS transistors include: (a) threshold voltage increment, (b) drain current degradation, and (c) delay increment [4, 5]. These effects show up themselves at the circuit level by increasing circuit delays and in turn circuit timing errors.

BTI degradation results from several electro-chemical sub-processes in the MOS transistors with pure silicon dioxide (SiO_2), plasma nitrided or thermally nitrided dielectric layer [6]. These sub-processes take place during transistor "ON" state and produce charges at the Si-SiO_2 interface [3, 4]. The charges cause transistor threshold voltage shift and consequently gate delay increment at the circuit level. A unique property of BTI is annealing of the charges at the Si-SiO_2 interface during the transistor "OFF" state. The charge annealing reduces the threshold voltage shift and results in a lower gate delay. Therefore, depending on the "ON", "OFF" states of the transistors, gates in a circuit suffer from higher/lower delays. Furthermore, BTI effects depend on process parameters (e.g. V_{th}) as well as environmental parameters (e.g. temperature).

In recent years, there is an escalation of interest in BTI modeling and analysis at: (a) device, (b) gate, and (c) circuit levels. The BTI modeling and analysis proposed in the literature so far can be classified as:

- **Device level analysis:** Alam et al. in [4] modeled NBTI in the PMOS transistors as Reaction Diffusion (RD) process, while Tibor et al. in [7] modeled

NBTI in term of first order kinetics. Similarly, Zafar et al. [3] also reported PBTI in the high-κ dielectrics.

- **Gate level analysis:** Paul et al. in [8] modeled NBTI impact on the gate delay using RD model. Similarly, Rakesh et al. in [13] modeled long term NBTI impacts on gate delays.
- **Circuit level analysis:** Wang et al. in [14] analyzed NBTI impact on combinational and sequential circuits. Krishnan et al. in [15] presented experimental results of NBTI impacts in digital circuits.

All the above studies focus on BTI modeling and analysis. At the device level BTI is deeply analyzed and modeled analytically (although the exact mechanism is still under the debate [3, 4, 7]). The research at the gate and circuit levels suffers from very fundamental limitations as they do not consider: (a) BTI distribution in the gate's transistors (b) electrical interference between BTI's in the adjacent transistors of the gate, (c) biasing at each transistor input in the gate, and (d) process and temperature variation in the circuit. Moreover, the interdependence of these parameters further complicates BTI at gate and circuit levels. Hence, there is a growing need for comparative analysis of BTI impact at gate and circuit levels.

This paper presents BTI analysis at gate and circuit levels. The gate level analysis is based on organization of transistors inside a gate. The analysis reveal that PBTI in serially connected NMOS transistors of NAND gate has a positive interference and causes additional delay up to 1.44× the NBTI induced additional delay in the parallel connected PMOS transistors. Similarly, NBTI in serially connected PMOS transistors of PMOS transistors causes additional delay up to 55 × PBTI induced delay in the parallel connected NMOS transistors. The circuit level analysis are based on the gates organization in the circuit. Specifically Therefore, to have a realistic insight of BTI analysis at the gate and circuit levels. In addition, impacts of the BTI on the leakage current and power - both static and dynamic - powers are presented.

The rest of the paper is organized as follows: Section 2 presents BTI mechanisms and its analysis at the device level. Section 3 presents gate levels analysis of BTI. The circuit level analysis are presented in Section 4. Finally, Section 5 concludes the paper.

2 Device Level BTI Analysis

BTI is characterized by the threshold voltage (V_{th}) increments of the MOS transistors. V_{th} increment in PMOS transistors that occurs under the negative gate stress is referred as NBTI and one that occur in NMOS transistors during positive gate stress is knows as PBTI. Zafar et al. in [3] have made a comparative study of NBTI and PBTI in MOS transistors with different gate dielectrics and concluded that either NBTI or PBTI can can become more significant depending on the type of dielectrics.

NBTI affects PMOS transistors and originates from Silicon Hydrogen bonds (≡Si-H) breaking that occur at Silicon-Silicon dioxide ($Si\text{-}SiO_2$) interface as shown in Fig. 1(a). The broken Silicon bonds (≡Si-) act as interface traps at the $Si\text{-}SiO_2$ interface and the H atoms/molecules diffuse toward the poly gate. The *number of interface traps (N_{IT})* depends on ≡Si-H bond breaking rate (k_f) and ≡Si- bond recovery rate (k_r). A similar mechanism in NMOS transistors under the positive gate stress results in PBTI.

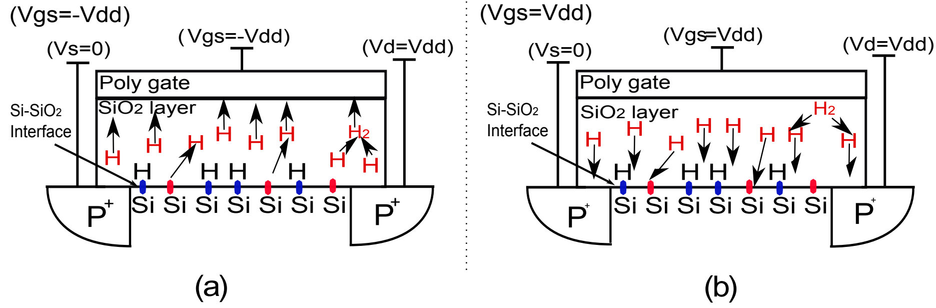

Fig. 1. Schematic view of (a) Si-H bond breaking, H and H_2 diffusions toward poly gate and their interconversion at Si/Si0_2 interface and inside oxide dielectric under negative gate stress (b) H and H_2 diffusions toward the Si-SiO$_2$ interface and ≡Si- bond recovery under positive gate stress

In recent times, exhaustive efforts have been put to understand NBTI at the device level [3, 9, 4]. Kackzer et al. in [9] have analyzed NBTI at the device level reasonably well but have not extended their analysis to deal with NBTI at a higher level. Alam et al. in [4] have modeled the overall dynamics of BTI as a reaction diffusion process. The model is usable at a higher level such as circuit level. Since in this work, BTI analysis is done at the gate and circuit levels, model of [4] will be used that relates N_{IT} with time (t) as follows:

$$N_{IT}(t) = \left(\frac{k_f.N_o}{k_r}\right)^{2/3} \left(\frac{k_H}{k_{H_2}}\right)^{1/3} (6.D_{H_2}.t)^{1/6}, \tag{1}$$

where N_o, k_H, k_{H2}, and D_{H2} represent initial bond density, H to H_2 conversion rate, H_2 to H conversion rate, and H_2 diffusion rate inside SiO$_2$ layer, respectively. Interface traps are the charges remaining at the Si-SiO$_2$ interface that oppose the applied gate stress resulting in the threshold voltage increment (ΔV_{th}). The relation between N_{IT} and ΔV_{th} is given by:

$$\Delta V_{th} = (1+m).\chi.q.N_{IT}/C_{ox}, \tag{2}$$

where m, q, and C_{ox} are the holes mobility degradation that contribute to the V_{th} increment [5], electron charge, and oxide capacitance, respectively. Similarly, χ is BTI coefficient with a value χ=1 for NBTI and χ=0.5 for PBTI. On the other hand, NBTI/PBTI annealing takes place under the positive/negative gate stresses in PMOS/NMOS transistors; in this case, the H atoms anneal back towards the Si-SiO$_2$ interface as shown in Fig. 1(b). The H atoms/molecules anneal the ≡Si- bonds resulting in lower N_{IT} and hence lower ΔV_{th}.

The NBTI/PBTI induced ΔV_{th} of PMOS/NMOS transistors causes additional gate delay by increasing rising/falling transition times [10]. A generalized formula for NBTI/PBTI induced additional delay is given by [8]:

$$\Delta D = \gamma.\frac{n.\Delta V_{th}}{(V_{gs} - V_{th})} \tag{3}$$

where n is the velocity saturation index and γ represents the distribution of stress and recovery -negative and positive gate stresses- durations. The γ dependence of the additional delay reveals that transistors in circuit having different stress/recovery duration will suffer from different delays, resulting in the circuit delay variation. The impacts of BTI on the transistors is investigated by

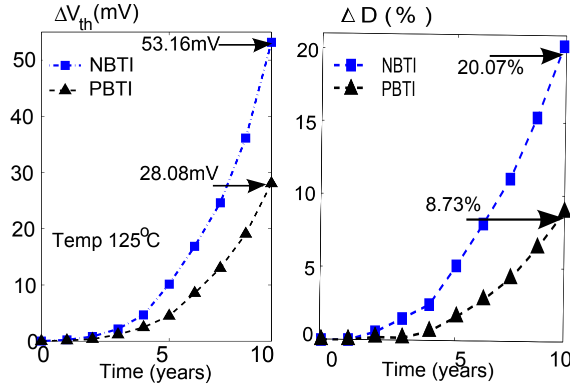

Fig. 2. (a) BTI induced (ΔV_{th}) increment of PMOS and NMOS transistors as a function of time (b) Inverter delay ΔD increment due to NBTI and PBTI

simulating 45nm Predictive Technology Model (PTM) transistor models [17] using HSPICE. To focus on BTI in the transistors, it is assumed that process variations and the other failure mechanisms, e.g. Hot Carrier Degradation, Electro-migrations and Time Dependent Dielectric Breakdown are not affecting the transistors. Throughout the simulation, γ=50% and BTI parameters used to get ΔV_{th} are, $k_f = 8\times10^{-4}s^{-1}$, $k_r=3\times10^{-18}cm^3s^{-1}$, $N_o = 5\times10^{16}cm^2$, $D_{H2}=4\times10^{-21}cm^2s^{-1}$ and T = 125°C [11]. Fig. 2(a) gives the ΔV_{th} increment of PMOS/NMOS transistors due to NBTI/PBTI; it shows that ΔV_{th} due to NBTI and PBTI approache 53.16mV and 28.08mV, respectively, after 10 years of operation. The curve follows 1/6 trend and have a good match with the experimental results presented in [3, 12]. Fig. 2(b) shows ΔD i.e. the percentage increment of the delay that approache 20.07% -at rise output transition- and 8.73% -at falling output transition- due to NBTI and PBTI, respectively. Paul et al. in [8] has suggested the same ΔD trend due to NBTI for the other gates of a circuit.

3 Gate Level BTI analysis

Traditionally, BTI impacts on logic gates are estimated as follows: the PMOS and NMOS transistors are considered mutually independent. ΔV_{th}'s of PMOS/NMOS transistors due to NBTI/PBTI are estimated using Eq. 2. Then the maximum ΔV_{th} is taken and applied to all the transistors used to calculate delay of the gates. Clearly, the traditional method is not realistic in the gate level analysis, because the impacts of transistors organization in the gate and the corresponding input is not considered. This section presents BTI analysis in the gate level that consider transistor organization and input impacts.

Sakuri et al. in [16] suggested that the gate output rise and fall transition times depend on the threshold voltages of the PMOS and NMOS transistors, respectively. Since NBTI/PBTI affects PMOS/NMOS transistor threshold voltages, gate rise and falling transition times has to be considered for NBTI and PBTI analysis, respectively [10]. To compare the impacts of NBTI and PBTI on gate delays it is necessary to consider on organization of transistors in the gate. The consideration will determine the stresses on the individual PMOS and NMOS transistors and consequently differentiate the impact of NBTI and PBTI on the gate.

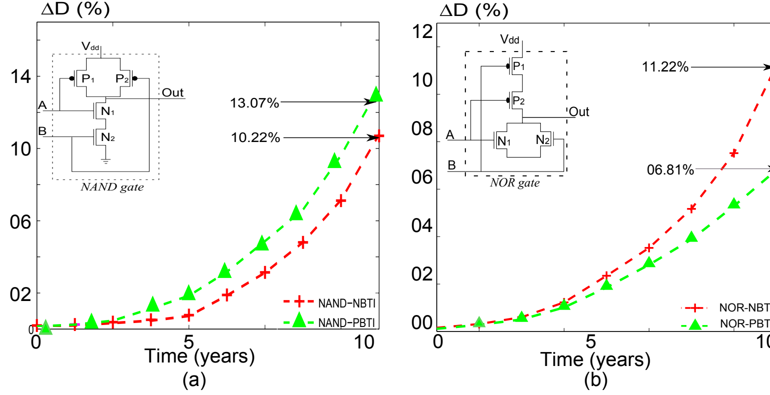

Fig. 3. (a) Percent delay (rising and falling output transition time increment) of NAND and AND gates due to NBTI and PBTI (b)Percent delay (rising and falling output transition time increment) of NOR and OR gates due to NBTI and PBTI

The inset in Fig. 3(a) shows transistor organization in a NAND gate. The figure shows that the gate has two NMOS -N_1 and N_2- transistor connected in series and two PMOS -P_1 and P_2- transistors connected in parallel. PBTI impact on the serially connected NMOS transistors will accumulate resulting in the larger output *falling* transition time. However, PMOS transistors are connected in parallel and have mutually exclusive impact on the *rising* transition of the output. NAND of the inset are synthesized using 45nm Predictive Technology Model (PTM) transistor models [17] and simulated using HSPICE for 10 years operation. Simulation result in the figure shows that due to this organization of transistors in NAND gate, far a given activity factor at the inputs A and B -50% of total period-, the delay increment due to PBTI is about 13.07% as compared to 10.22% of the NBTI induced delay to the gate. Therefore, it can be concluded that PBTI impact dominates in NAND gate and approaches upto 1.28× the NBTI impact.

The inset of Fig. 3(b) shows a NOR gate with series connected PMOS -P_1 and P_2- transistors and parallel connected NMOS -N_1 and N_2- transistors. The figure show that NBTI impact in the serially connected PMOS transistors will agglomerate to cause higher increment to the output *rising* transition time than the PBTI in the parallel connected NMOS transistors will cause to the *falling* transition time. NOR gate of the inset is synthesized using 45nm Predictive Technology Model (PTM) transistor models [17] and simulated using HSPICE for 10 years operation. The simulation results shows that impact of NBTI - 11.22% increment to the rise transition time- is 1.64× the PBTI impact -6.81% increment in the fall transition time- for NOR gate under identity input activity.

Having analyzed BTI effects in the basic gates, the next is BTI analysis in complex gates. Complex gates realize complex logic functions using suitable MOS transistors configuration. For example, the logic function is realized by the transistor configuration show in Fig. 3(a). The figure shows that the gate has XX serially connected XMOS transistors that causes up to XX% additional delay, while XBTI under the worst case can cause up to XY% delay. Moreover, to extend BTI in other complex gates. Table 1 shows the complex logic functions and impact of BTI.

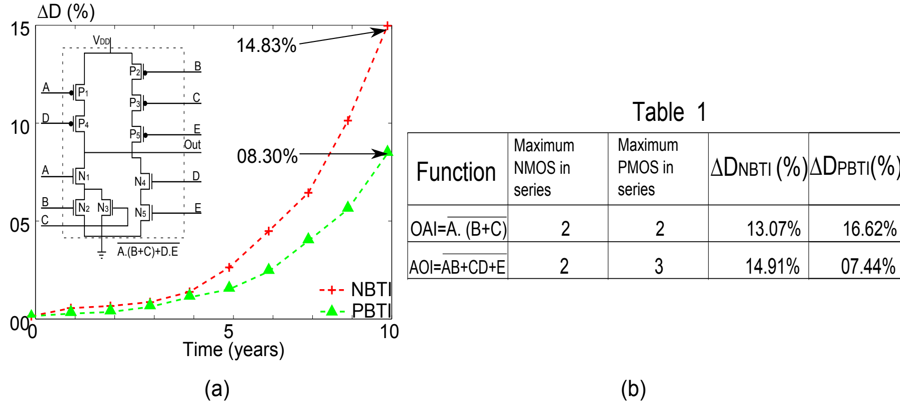

Table 1

Function	Maximum NMOS in series	Maximum PMOS in series	ΔD_{NBTI} (%)	ΔD_{PBTI}(%)
OAI=$\overline{\text{A. (B+C)}}$	2	2	13.07%	16.62%
AOI=$\overline{\text{AB+CD+E}}$	2	3	14.91%	07.44%

Fig. 4. (a) Percent delay (rising and falling output transition time increment) of NAND and AND gates due to NBTI and PBTI (b)Percent delay (rising and falling output transition time increment) of NOR and OR gates due to NBTI and PBTI

4 Circuit Level BTI Analysis

The analysis of BTI at circuit is more complicated due to organization of transistors in gates that are connected to each other.

To demonstrate BTI analysis at the circuit level, an example circuit of C17 ISCAS 85 benchmark as shown in Fig.4(a) is considered. The ΔV_{th} of Eq. 2 was integrated in the circuit to compute delay of gates in the circuit. Delay increment measurements taken from HSPICE simulation using 45nm PMOS transistor model. Fig.4(b) shows a gates based delay analysis of the circuit. The key insight of the figure reveals that:

– At the same level in circuit, at the same γ value, NBTI induced delay of a gate is larger than PBTI induced delay. For example G9 has NBTI induced delay of about 17%, however, it suffers from only 12.4% PBTI induced delay delay. This verifies our gate level analysis that NBTI induced delayis larger than the PBTI induced delay.
– NBTI induced delay in a gate affects PBTI impact on the succeeding gate. For example, G_{16} has larger -27%- NBTI induced delay increment that results in higher PBTI impact -17%- in G_{17}. This increment may be attributed to the fact that NBTI increases rise transition time of G_{16} output, that adds to PBTI impact on G_{17} and results in higher falling transition time of G_{17} output.

Bechmark	Delay(%)		
	NBTI	PBTI	BTI (NBTI+PBTI)
C432	14.65	4.71	17.67
C880	6.39	4.32	11.31
C1355	10.57	16.87	15.34
C1908	5.67	3.23	9.04

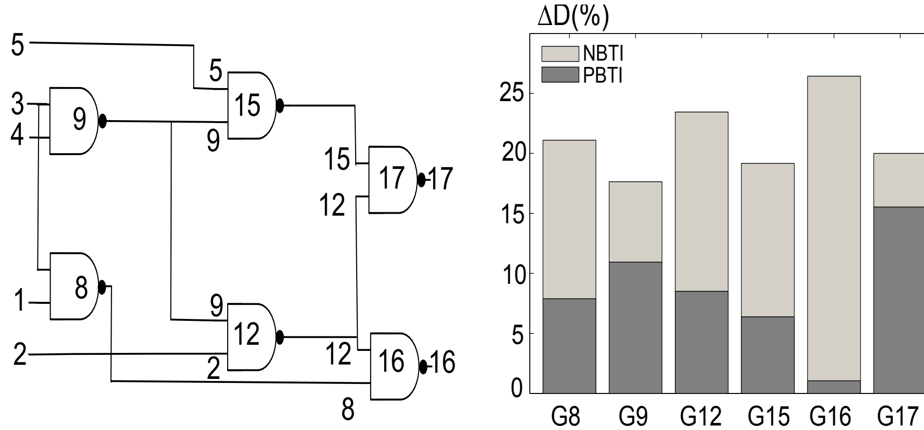

Fig. 5. (a) Schematics of C17 ISCAS-85 benchmark circuit (b)Percent delay (rising and falling output transition time increment) C17 gates due to NBTI and PBTI

5 Conclusion

This paper presented ReverseAge, an online technique to tolerate NBTI induced delays by utilizing design time margin. ReverseAge proposes an NBTI monitoring scheme along with a technique to tolerate NBTI induced delay. The monitor detects NBTI induced delay and generate a timing error signal. Thereafter, the timing error of the stage is tolerated by borrowing time from the successive stages. Simulation result from benchmark circuit shows that ReverseAge ensures 3× reliability improvement at the cost of 3.77% area and 1.4% power overheads.

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