A New Latch-Based Threshold Logic Family

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Abstract

This paper presents a new low-power Threshold Logic family with self lock-out property. The simulated results have shown that, the proposed Threshold Logic dissipates between 10% *and* 79% *less power and between* 57% *and* 71% *less energy, at* $VDD = 5V$*, when compared with previous similar Threshold Logic families. Moreover, at* $VDD = 3.3V$*, it has between* 12% *and* 48% *less energy and between* 34% *and* 60% *less dissipated power in the worst case.*

1 Introduction and Previous Work

Traditional digital IC implementations are based on Boolean theory. As the operands length is becoming larger and larger, Boolean implementation performance might be severely affected by a large circuit depth and alternative solutions are required. A potential alternative to Boolean Logic appears to be Threshold Logic (TL) [5] which makes use of a generalized basic building block named *Linear Threshold Gate* (LTG). Such an LTG is a multi-terminal device which performs two basic operations: input weighting and thresholding. The output is logic one if the weighted sum of the input values is greater than the threshold value, T, and zero otherwise.

More formally, the output of a linear threshold gate is given by:

$$F(X) = sgn\{\mathcal{F}(X)\} = \begin{cases} 0, & \text{if } \mathcal{F}(X) < 0 \\ 1, & \text{otherwise} \end{cases} \quad (1)$$

$$\mathcal{F}(X) = \sum_{i=0}^{n-1} \omega_i x_i - T \quad (2)$$

where the set of input variables and weights associated with the inputs are defined by $X = \{x_0, x_1, \ldots, x_{n-1}\}$ and $\Omega = \{\omega_0, \omega_1, \ldots, \omega_{n-1}\}$, respectively.

Given that LTGs are fundamentally more powerful[1] than the conventional Boolean gates a number of theoretical investigations have been reported regarding the possibilities of such an approach in the design of useful

[1] Speaking from the device/circuitry point of view the main advantage of LTGs when compared to standard Boolean gates is the parallel processing due to internal multiple-valued computation of the weighted sum. However when compared to classical multiple-valued logic circuits LTG gates are more robust against parameter variation because the LTG inputs and output are still digital encoded.

0-7803-6666-2/01/$10.00

Boolean functions [2],[5],[8]. Moreover, TL implementations have received considerable attention in the early 90's [4],[7],[9] and later, with the technology advances, more LTG implementations have been proposed [1],[3],[6].

Although the so called Neuron MOS transistor (νMOS) [9] is very compact, it suffers from process dependence due to the unpredictable resolution and reprogramming relies ultimately on UV erasure. The implementations proposed in [4] and [7] although favorable in integration density, suffer from high nonlinearity and power consumption. Capacitive Threshold Logic (CTL) [6] has a high fan-in capability but performs weighting using a capacitive bank which is prone to a high area in a typical CMOS technology. Moreover, thresholding is performed with a properly designed inverter chain, which suffers from a lower speed at higher fan-in. In addition, CTL gate presents DC power consumption in evaluation phase which restricts its utilization only for rather small designs.

Recently, two latch-based LTGs [1],[3] were disclosed. In contrast with previous LTGs, both feature only dynamic power consumption and are differential. The gates have in common two parallel connected sets of NMOS transistors implementing basically the weighting operation and a CMOS comparator based on cross-coupled inverters.

The latch-type comparator TL (LCTL) [1], features an internal self-locking mechanism to cut-off the power supply current immediately after the evaluation but the internal latch has a high recovery time caused by a long feedback chain. While cross-coupled inverters with asymmetrical loads TL (CIALTL) [3] has the NMOS banks external to the CMOS latch, and thus reducing dynamic power consumption, it has a great amount of power dissipated in the internal clock front end.

In the present paper we propose a low-power latch-based LTG based on differential-current switch logic (DCSL) [10]. Compared with the LTGs presented above, our scheme has the following advantages:

- higher speed when compared with LCTL since the $Clk - Y$ delay is imposed by a simpler latch;
- less dissipated dynamic power when compared with CIALTL. This is both due to the true single phase clock operation and due to a more restricted voltage swings in the internal highly capacitive nodes.

2 Gate Description and Operation

The proposed LTG circuit is depicted in Figure 1.

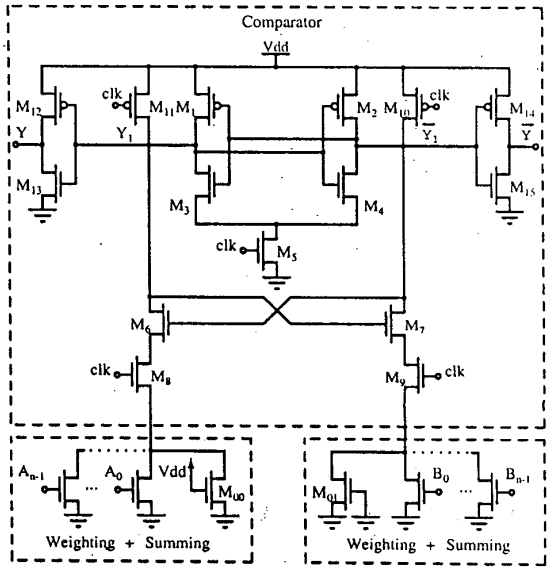

Figure 1: The Proposed Differential Current-Switch TL schematic (DCSTL)

The comparator is implemented with a strobed CMOS latch circuit while the analog computation blocks consist of two parallel connected sets of NMOS transistors, referred from

this point as *NMOS banks*. Compared with CIALTL, two new transistors, M_6 and M_7, are present for automatic lock-out of inputs and reduced effective internal capacitance at the output, [10]. The comparator decides if the voltage level in Y_1 is greater than the voltage level in $\overline{Y_1}$. Those voltages are imposed by the currents generated in both NMOS banks.

The gate is in principle a clocked differential cascode voltage switch (DCVS) circuit, operated with a single phase clock. M_{10} and M_{11} are precharge transistors while CMOS inverters $M_{12} - M_{13}$, $M_{14} - M_{15}$ are provided for buffering to succeeding LTG stages. M_6 and M_7 are two transistors introduced for reduced voltage swing (and thus power dissipation) in the NMOS trees. The dynamic operation of this LTG is divided into a precharge phase and an evaluation phase.

During precharge phase, *clk* low switches on M_{10}, M_{11} precharging the parasitic capacitors from Y_1 and $\overline{Y_1}$. The evaluation phase starts with *clk* high, switching on the NMOS transistors M_5, M_8, M_9, and cutting off M_{10} and M_{11}. The currents flowing from the NMOS banks discharge the parasitic capacitors and the voltage difference between Y_1 and $\overline{Y_1}$ is amplified to a voltage swing nearly equal to the power supply voltages. The evaluation is performed in two steps. During the first step the dynamic latch don't regenerate because both Y_1 and $\overline{Y_1}$ node voltages are greater than inverter's threshold. During the second step, the latch rapidly regenerates according to the voltage difference between the nodes. Assuming the left bank current greater than the current in the right one, M_7 tend to switch off while M_6 progressively switches on and thus, the high going internal node is decoupled from being connected to ground, reducing power.

3 Performance Evaluation

The proposed gate performance is compared with CIALTL [3] and LCTL [1]. To have a fair comparison, we used a 31-input AND function as a benchmark ($T = 31$) because it achieves the highest level of current generated by the threshold mapping block. Also, all three gates were simulated with an identical load of 100fF and the input signals were applied via minimum-sized inverters. The results were obtained in 1.6μ gate length CMOS technology using Philips MOS Level 9 models, at room temperature.

For all considered gates, the transistor's geometries were optimized to achieve the minimum gate power-delay-product using the HSPICE optimizer. The power is the sum between the power dissipated in the internal gate, necessary to switch the load capacitance and the power dissipated in the clock drivers. During the simulation-optimization cycle, 30 inputs of the gates are logic one and a single input switches. Since the CMOS latch has to evaluate correctly even in that case, with a small amount of voltage difference between the differential latch inputs, this is the worst case from the power dissipation point of view.

Table 1 summarizes the simulated characteristics of each LTG after power-delay product optimization. Note that, when compared with CIALTL, DCSTL exhibits an average delay penalty of at most 30%, given the higher strength of the NMOS trees but saves 60% power mainly due to the single phase clock operation and a lower voltage swing of the nodes A and B.

Conversely, LCTL is with 22% slower than DCSTL and has 10% more dynamic power dissipation. DCSTL and LCTL have lower power dissipation when compared with CIALTL because they present quite similar mechanisms of reducing the power supply currents by self-locking of the outputs and both are operated with a single-phase clock scheme. However, when compared with LCTL and CIALTL, in terms of power-delay-product, DCSTL has between 57% and 71% less energy, at $VDD =$

Table 1: LTGs simulated characteristics for VDD=5V and VDD=3.3V

	VDD=5V				VDD=3V				
	Power (μW)	Delay (pS)	PDP (pJ)	Total Gate Width (μm)	Power (μW)	Delay (pS)	PDP (pJ)	Total Gate Width (μm)	Device Count
DCSTL	729	358	0.261	244	293	715	0.209	270	17+2*n
CIALTL	1325	288	0.381	218	468	505	0.236	245	27+2*n
LCTL	840	524	0.440	208	393	1793	0.704	190	14+2*n

$5V$, and between 12% and 48% less energy at $VDD = 3.3V$.

4 Conclusions

In this paper a Differential Current-Switch Threshold Logic (DCSTL) for low-power was presented. The simulated results have shown that, the proposed Threshold Logic dissipates between 10% and 79% less power and between 57% and 71% less energy, at $VDD = 5V$, when compared with previous similar Threshold Logic families. Moreover, at $VDD = 3.3V$, it has between 12% and 48% less energy and between 34% and 60% less dissipated power in the worst case.

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