Impact of Memory Cell Array Bridges on the Faulty Behavior in Embedded DRAMs

Zaid Al-Ars Ad J. van de Goor
Section CARDIT, Faculty of Information Technology and Systems
Delft University of Technology, Mekelweg 4, 2628 CD Delft, The Netherlands
E-mail: z.e.al-ars@its.tudelft.nl, vdGoor@cardit.et.tudelft.nl

Abstract: *Establishing functional faults, based on defect injection and circuit simulation, has become an important method in understanding faulty memory behavior and in improving memory tests. In this paper, this approach is used to study the effects of bridges on the faulty behavior of embedded DRAM (eDRAM) devices. The paper applies the new approach of fault primitives to perform this analysis. The analysis shows the existence of previously defined memory fault models, and (re)establishes new ones. The paper also investigates the concept of dynamic faulty behavior and establishes its importance for memory devices.*

Key words: *Embedded DRAM, functional fault models, fault primitives, defect simulation, bridges, dynamic faulty behavior.*

1 Introduction

Embedded DRAMs (eDRAMs) are dynamic RAM cores used on-chip along with other electrical components. Using on-chip memory components has many advantages over external memory chips, such as an increased bandwidth, reduced power consumption, suitable memory organization and low electromagnetic interference. Although *e*DRAMs have been extensively used in application specific integrated circuits (ASICs), little has been published on their fault analysis and testing.

For quite a while now, researchers have been studying the faulty behavior of memory devices and defining *functional fault models (FFMs)* to describe the detected faulty behavior, and develop tests which target these FFMs [vdGoor98, Adams96]. On the other hand, papers have been published that study the faulty behavior of memory devices by performing a large number of tests and statistically analyzing the detected FFMs [vdGoor99, Schanstra99]. The results of the theoretical and practical analysis show that our ability to understand, and thus predict, the faulty behavior of memories is still limited to relatively simple cases of defective devices.

Much of the work on functional fault modeling has been concerned with modeling faults sensitized by a single performed operation; these fault models are referred to as *static FFMs*. In this paper, it is shown that a large number of FFMs exist that have to be sensitized by a sequence of two or more operations; these are referred to as *dynamic FFMs*.

This paper establishes all static single-cell FFMs, a number of single-cell 2-operation dynamic FFMs, and a number of two-cell static and dynamic FFMs. The analysis is performed on the memory cell array of an *e*DRAM, by injecting electrical bridge defects into the electrical model of the *e*DRAM. Naik[93] has used this approach for static FFMs in SRAMs.

This paper is organized as follows. Section 2 describes the used *e*DRAM simulation model, then Section 3 defines the static and dynamic FFMs targeted in this paper. In Section 4, the defects to be injected into the simulation model are defined and classified. Section 5 gives the methodology to be used for performing the simulations and extracting the FFMs. Section 6 discusses the simulation results, followed by Section 7 with the conclusions.

2 *e*DRAM simulation model

This section introduces the *e*DRAM simulation model used for defect injection and fault analysis. The analysis focuses on the memory cell array part of the *e*DRAM, since it has the largest chip area and is the most fault sensitive.

The simulation model is based on a design-validation model of an actual *e*DRAM. Since the time needed for simulating a complete memory device is excessively long, the simulation model used is simplified, taking two factors into consideration in order to preserve the model accuracy. First, removed components should be electrically compensated, and second, the resulting simplified circuit should

1081-7735/00 $10.00 © 2000 IEEE

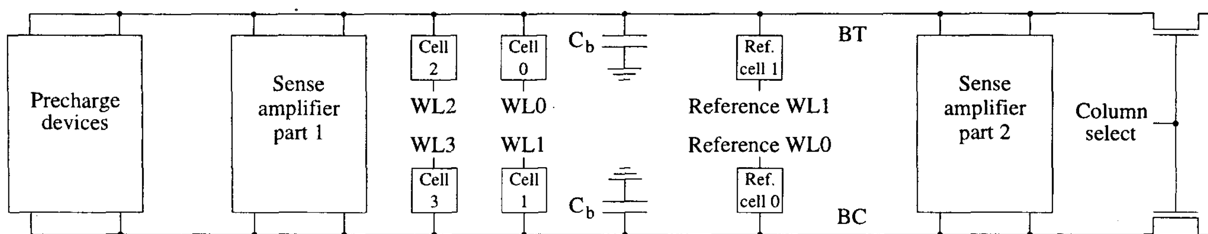

Figure 1. Cell array column of the *e*DRAM, complete with reference cells, sense amplifier, precharge and access circuits.

describe enough of the memory to enable injecting the defects of interest.

The analysis in this paper accesses only four memory cells along one memory cell array column, which means that the state of the unused cells does not affect the behavior of the cell array column. Yet, unused cells do contribute to capacitance of the bit lines. Therefore, the memory model can be simplified by removing the unused cells and compensating their effect by resistances and capacitances along the bit line. Figure 1 shows a block diagram of the cell array column of the simulated *e*DRAM. The simplified simulation model contains a 2×2 cell array, in addition to two reference cells, precharge circuits and a sense amplifier. In addition to the shown cell array column, the simulation model contains one data output buffer needed to examine data on output lines, and a write driver needed to perform write operations.

Despite the fact that the general structure of the *e*DRAM model shown in Figure 1 is similar to the structure of other types of DRAM, the device parameters used for this model are derived for an *e*DRAM fabrication process. Whether the results given in this paper are also applicable for other DRAM products is a question open for investigation.

3 Definition of FFMs

In this section, the FFMs used in this paper are defined. First, a classification of the FFMs is presented with which the total space of faults can be divided into a number of classes. Then, four of these classes are discussed and used to define the targeted FFMs.

3.1 Classification of fault models

Two basic ingredients are needed to define any fault model: a list of performed memory operations and a list of corresponding deviations in the observed behavior from the expected one. The only functional deviations considered relevant to the faulty behavior are the stored logic value in the cell and the output value of a read operation.

Any difference between the observed and expected memory behavior can be denoted by the following notation $<S/F/R>$, referred to as a *fault primitive (FP)*. S describes the *sensitizing operation sequence (SOS)* that sensitizes the fault; F describes the value of the faulty cell, $F \in \{0,1\}$; and R describes the logic output level of a read operation, $R \in \{0,1,-\}$. If the operation that sensitizes the fault is a write operation, then the memory has no expected output; the '–' is used for the R in this case.

FPs can be classified according to $\#C$, the number of different cells accessed during an SOS, and according to $\#O$, the number of different operations performed in an SOS. A taxonomy of FPs is shown in Figure 2.

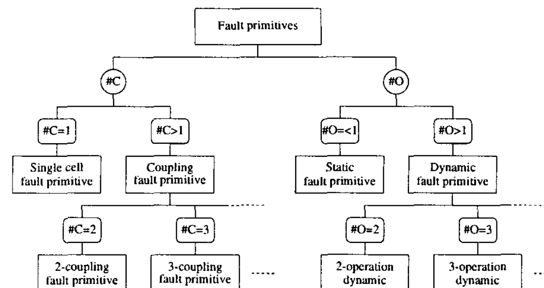

Figure 2. Taxonomy of fault primitives.

The notion of FPs makes it possible to give a precise definition of an FFM as understood for memory devices. This definition is presented next.

> A **functional fault model** (FFM) is a non-empty set of fault primitives (FPs).

3.2 Single-cell static FFMs

Single-cell static FFMs describe faults sensitized by performing at most one operation on the faulty cell. As mentioned earlier, a particular FP is denoted by $<S/F/R>$. S describes the value or operation that sensitizes the fault,

Table 1. All possible combinations of the values in the $<S/F/R>$ notation resulting in single-cell static FPs.

#	S	F	R	FP	Fault model
1	0	1	-	$< 0/1/- >$	SF_0
2	1	0	-	$< 1/0/- >$	SF_1
3	$0w0$	1	-	$< 0w0/1/- >$	WDF_0
4	$0w1$	0	-	$< 0w1/0/- >$	$TF\uparrow$
5	$1w0$	1	-	$< 1w0/1/- >$	$TF\downarrow$
6	$1w1$	0	-	$< 1w1/0/- >$	WDF_1
7	$0r0$	0	1	$< 0r0/0/1 >$	IRF_0
8	$0r0$	1	0	$< 0r0/1/0 >$	$DRDF_0$
9	$0r0$	1	1	$< 0r0/1/1 >$	RDF_0
10	$1r1$	0	0	$< 1r1/0/0 >$	RDF_1
11	$1r1$	0	1	$< 1r1/0/1 >$	$DRDF_1$
12	$1r1$	1	0	$< 1r1/1/0 >$	IRF_1

$S \in \{0, 1, 0w0, 0w1, 1w0, 1w1, 0r0, 1r1\}$ for static FPs. F and R have already been defined in Section 3.1.

Now that the possible values for S, F and R are known for single-cell static FPs, it is possible to list all detectable FPs using this notation. Table 1 lists all 12 possible combinations of the values, in the $<S/F/R>$ notation, that result in FPs [vdGoor00]. The column 'Fault model' states the FFM defined by the corresponding FP.

All FPs listed in Table 1 are targeted in this paper. Below, they are used to define 6 different FFMs described in terms of non-empty sets of FPs.

1. **State faults (SF_x)**—A cell is said to have an SF if the logic value of the cell flips before it is accessed, even if no operation is performed on it[1]. Two types of SF exist: $SF_0 = \{<0/1/->\}$, with FP #1, and $SF_1 = \{<1/0/->\}$, with FP #2.
2. **Transition faults (TFx)**—A cell is said to have a TF if it fails to undergo a transition ($0 \rightarrow 1$ or $1 \rightarrow 0$) when it is written. Two types of TF exist: $TF\uparrow = \{<0w1/0/->\}$, with FP #4, and $TF\downarrow = \{<1w0/1/->\}$, with FP #5.
3. **Read disturb faults (RDF_x)** [Adams96]—A cell is said to have an RDF if a read operation performed on the cell changes the data in the cell and returns an incorrect value on the output. Two types of RDF exist: $RDF_0 = \{<0r0/1/1>\}$, with FP #9, and $RDF_1 = \{<1r1/0/0>\}$, with FP #10.
4. **Write disturb faults (WDF_x)**—A cell is said to have a WDF if a non-transition write operation ($0w0$ or $1w1$) causes a transition in the cell. Two types of WDF exist: $WDF_0 = \{<0w0/1/->\}$, with FP #3, and $WDF_1 = \{<1w1/0/->\}$, with FP #6.
5. **Incorrect read faults (IRF_x)**—A cell is said to have an IRF if a read operation performed on the cell returns the incorrect logic value, while keeping the correct stored value in the cell. Two types of IRF exist: $IRF_0 = \{<0r0/0/1>\}$, with FP #7, and $IRF_1 = \{<1r1/1/0>\}$, with FP #12.
6. **Deceptive read disturb faults ($DRDF_x$)** [Adams96]—A cell is said to have a DRDF if a read operation performed on the cell returns the correct logic value, while it results in changing the contents of the cell. Two types of DRDF exist: $DRDF_0 = \{<0r0/1/0>\}$, with FP #8, and $DRDF_1 = \{<1r1/0/1>\}$, with FP #11.

The 6 FFMs defined above cover the space of all 12 single-cell static FPs of Table 1. Any single-cell static FFM can be represented as the union set of two or more of these 12 FPs. For example, if a defect results in a faulty behavior represented by an incorrect read-1 fault (IRF_1) and a read-0 disturb fault (RDF_0), then the corresponding behavior is described as $\{<1r1/1/0>\} \cup \{<0r0/1/1>\} = IRF_1 \cup RDF_0$.

3.3 Single-cell dynamic FFMs

FFMs sensitized by performing more than one operation on the faulty memory cell are called *dynamic fault models*. There are 2-operation, 3-operation, ..., dynamic fault models, depending on $\#O$. Here, we restrict ourselves to the analysis of 2-operation dynamic FFMs.

There are 30 different single-cell 2-operation dynamic FPs possible [vdGoor00], but in order to reduce simulation time, not all 30 FPs are considered. We choose only to target the 4 dynamic SOS's $0w0r0$, $0w1r1$, $1w0r0$ and $1w1r1$ (in short $xwyry$), because in memory devices, an isolated write operation may not be sufficient to detect a fault since, externally, a cell needs to be read to detect the stored value set during the write.

The 4 targeted SOS's are capable of sensitizing 12 single-cell 2-operation FPs, which are used to define the following 3 FFMs. The names of these FFMs are chosen in such a way that they represent an extension of the single-cell static FFMs defined in Section 3.2.

1. **Dynamic read disturb fault (RDF_{xy})** is a fault whereby an $xwyry$ SOS changes the stored

[1] It should be noted that the state fault should be understood in the static sense. That is, the cell should flip in the short time period after initialization and before accessing the cell.

logic value to $\overline{y}$ and gives an incorrect output. Four types of dynamic RDF exist: RDF_{00} = $\{<0w0r0/1/1>\}$, RDF_{11} = $\{<1w1r1/0/0>\}$, RDF_{01} = $\{<0w1r1/0/0>\}$, and RDF_{10} = $\{<1w0r0/1/1>\}$.

2. **Dynamic incorrect read fault (IRF_{xy})** is a fault whereby an $xwyry$ SOS returns the logic value $\overline{y}$ while keeping the correct state of the cell. Four types of dynamic IRF exist: IRF_{00} = $\{<0w0r0/0/1>\}$, IRF_{11} = $\{<1w1r1/1/0>\}$, IRF_{01} = $\{<0w1r1/1/0>\}$, and IRF_{10} = $\{<1w0r0/0/1>\}$.

3. **Dynamic deceptive read disturb fault ($DRDF_{xy}$)** is a fault whereby an $xwyry$ SOS returns the correct logic value y while destroying the state of the cell. Four types of dynamic DRDF exist: $DRDF_{00}$ = $\{<0w0r0/1/0>\}$, $DRDF_{11}$ = $\{<1w1r1/0/1>\}$, $DRDF_{01}$ = $\{<0w1r1/0/1>\}$, and $DRDF_{10}$ = $\{<1w0r0/1/0>\}$.

3.4 Two-cell static FFMs

Two-cell static FFMs describe faults sensitized by performing at most one operation while considering the effect two different cells have on each other. A two-cell static FP can be represented as follows $<S/F/R>$ = $<S_a;S_v/F/R>_{a,v}$, where S_a and S_v are the sequences performed on the aggressor and victim, respectively. S_a and $S_v \in \{0, 1, 0w0, 0w1, 1w0, 1w1, 0r0, 1r1\}$. There are 36 possible two-cell static FPs this notation can distinguish [vdGoor00].

Below, a list of FFMs is constructed from the 36 FPs in such a way that all FPs are covered by at least one FFM.

1. **State coupling fault (CFst)** is a fault whereby the victim is forced into a given logic state only if the aggressor is in a given state, without performing any operation on the victim. This fault is special in the sense that no operation is needed to sensitize it and, therefore, it only depends on the initial stored values in the cells. Four types of CFst exist which can be summed up as: $CFst_{x;y}$ = $\{<x;y/\overline{y}/->\}$, where x, $y \in \{0,1\}$.
2. **Disturb coupling fault (CFds)** is a fault whereby an operation (write or read) performed on the aggressor forces the victim into a given logic state. Here, any operation performed on the aggressor is accepted as a sensitizing operation for the fault, be it a read, a transition write or a non-transition write operation. Twelve types of CFds exist which can be summed up as: $CFds_{xwy;z}$ = $\{<xwy;z/\overline{z}/->\}$ and $CFds_{xrx;y}$ = $\{<xrx;y/\overline{y}/->\}$, where x, y, $z \in \{0,1\}$.
3. **Transition coupling fault (CFtr)** is a fault whereby a given logic value in the aggressor results in the failure of a transition write operation performed on the victim. This fault is sensitized by a write operation on the victim and setting the aggressor into a given state. Four types of CFtr exist which can be summed up as: $CFtr_{x;\uparrow}$ = $\{<x;0w1/0/->\}$ and $CFtr_{x;\downarrow}$ = $\{<x;1w0/1/->\}$, where $x \in \{0,1\}$.
4. **Write disturb coupling fault (CFwd)** is a fault whereby a non-transition write operation performed on the victim results in a transition when the aggressor is set into a given logic state. Four types of CFwd exist: $CFwd_{x;y}$ = $\{<x;ywy/\overline{y}/->\}$, where x, $y \in \{0,1\}$.
5. **Read disturb coupling fault (CFrd)** is a fault whereby a read operation performed on the victim destroys the data stored in the victim if a given state is present in the aggressor. Four types of CFrd exist: $CFrd_{x;y}$ = $\{<x;yry/\overline{y}/\overline{y}>\}$, where x, $y \in \{0,1\}$.
6. **Incorrect read coupling fault (CFir)** is a fault whereby a read operation performed on the victim returns the incorrect logic value when the aggressor is set into a given state. Four types of CFir exist: $CFir_{x;y}$ = $\{<x;yry/y/\overline{y}>\}$, where x, $y \in \{0,1\}$.
7. **Deceptive read disturb coupling fault (CFdr)** is a fault whereby a read operation performed on the victim returns the correct logic value and changes the contents of the victim, when the aggressor is set into a given logic state. Four types of CFdr exist: $CFdr_{x;y}$ = $\{<x;yry/\overline{y}/y>\}$, where x, $y \in \{0,1\}$.

3.5 Dynamic two-cell FFMs

Just like the case of single-cell dynamic FFMs, we restrict ourselves here to the analysis of 2-operation dynamic fault models. Any particular FP is denoted by $<S/F/R>$ where S has the form given in Section 3.1. For example, the two-cell 2-operation FP $<v(0r0)\ a(1r1)/1/->$ stands for an FP sensitized by performing a $0r0$ first on the victim then performing a $1r1$ on the aggressor. After performing the sensitizing sequence, a 1 is detected in the victim cell instead of the expected 0. Based on the values of S, F and R, 192 detectable two-cell 2-operation dynamic FPs can be compiled.

Since we will only attempt to verify a limited number of dynamic FFMs for the reasons mentioned in Section 3.3), only those FPs with an SOS of the form $S = a(x)\ v(ywzrz)$ are targeted, where x, y and $z \in \{0,1\}$. This choice of S results in 24 different FPs targeted by the performed simulation. Since these FPs have not been observed in the analysis, they are not used to define corre-

sponding FFMs here. Such FFM definitions can be found in a previously published paper for vdGoor[00] .

4 Simulated defects

The defects to be considered for injection and analysis are modeled at the electrical level by parasitic components with a given impedance. The impedance (Z) consists of a resistance (R) and a capacitance (C) connected in parallel between two defective nodes. Depending on the defective nodes the injected defects are connected to, the defects may be classified into opens, shorts and bridges. This paper is only concerned with the effects of bridges, and does not address the effects of opens nor shorts.

Bridges represent unwanted impedances between two signal lines. For a bridge, the impedance value is denoted by Z_{br} and may have resistive and capacitive components. The value of R_{br} for a bridge resistance may have any value ($0 \leq R_{br} \leq \infty\ \Omega$), while C_{br} is bounded by some given realistic limits ($C_{min} \leq C_{br} \leq C_{max}$). The lower bound of the bridge capacitance is taken to be 0 F ($C_{min} = 0$ F), while the maximum bound is considered to be equal to the bit line capacitance in the memory ($C_{max} = C_b$). The reason behind this choice is that the bit line has the highest capacitance along a single cell array column. Therefore, it is highly unexpected for a parasitic capacitance to have yet a higher value.

4.1 Classification of bridges

By analyzing the electrical circuits of the cell array column, we notice some symmetry in the topology of these circuits. This results in a symmetry in the faulty behavior, which can be used to reduce the number of defects to be simulated and analyzed. The faulty behavior of one defect can help deduce the faulty behavior of another symmetrically related defect. For this purpose, we provide the following definitions:

- A defect D1 at a given position shows the **complementary faulty behavior** of a defect D2 at another position, if the faulty behavior of D1 is the same as that of D2, with the only difference that all 1s are replaced by 0s, and vice versa. For example, if D1 sensitizes $<0r0/1/1>$ then D2 sensitizes $<1r1/0/0>$.

- A defect D1 shows the **reverse faulty behavior** of a defect D2, if the faulty behavior of D1 and D2 contain two-cell faults, and if these two-cell faults are the same with the exception that the aggressor and victim are exchanged. In general, if a two-cell fault has the following notation $<S/F/R>_{x,y}$, then the reverse fault is given by the notation $<S/F/R>_{y,x}$.

- A defect D1 shows a **single-sided complementary behavior** of a defect D2, if the faulty behavior of D1 and D2 contain two-cell faults, and if these two-cell faults are the same with the exception that all 1s are replaced by 0s, and vice versa, in either the aggressor or the victim cells (not both). If the victim sides of two faults are the complement of each other, then these two faults are called *victim-sided complementary*. If the aggressor sides of two faults are the complement of each other, then these two faults are called *aggressor-sided complementary*. For example, suppose that D1, D2 and D3 affect cells x and y, and that D1 forces a $0w0$ operation to cause an up transition in y if cell x is in state 1, then this faulty behavior of D1 is denoted by $<1; 0w0/1/->_{x,y}$. The aggressor-sided complementary defect D2 should force a $0w0$ operation to cause an up transition in y if cell x is in state 0, which is the fault denoted by $<0; 0w0/1/->_{x,y}$. On the other hand, The victim-sided complementary defect D3 should force a $1w1$ operation to cause a down transition in y if cell x is in state 1, which is the fault denoted by $<1; 1w1/0/->_{x,y}$.

4.2 Location of bridges

A bridge in the memory cell array can connect any arbitrary pair of nodes. However, not all possible bridges in the cell array have been simulated, but only those that take place within a single cell or between different cells. This choice is motivated by the fact that memory cells take the largest part of the surface area in a dynamic RAM. Bridges connecting circuit nodes to V_{DD} or GND are excluded since these are considered as shorts.

Bridge within a memory cell (BWC)

To describe the bridges present within a memory cell, we refer to Figure 3 where the different nodes in the cell are given names. There are 4 nodes in the cell with the names BL[2], WL, rtop and ctop. In order to take all bridges into consideration, every node is bridged to every other node. Here, bridges between word and bit lines are excluded. The choice is made to simulate the bridges of a cell on BT. As a result, the behavior of a BWC defect in a cell on the complement bit line may be derived from the corresponding simulated one, since these two defects show a complementary behavior. A list of the simulated and complementary BWC defects is given in Table 2.

[2]BL means BT if the cell is connected to the true bit line, while it means BC if the cell is connected to the complementary bit line.

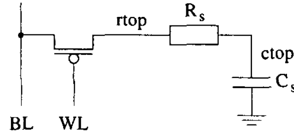

Figure 3. One *e*DRAM memory cell in which different nodes are given names.

Table 2. Description of the simulated and complementary bridges within a memory cell (BWC).

BWC on BT	BWC on BC	Description
BWC1s	BWC1c	Bridge between bit line and rtop
BWC2s	BWC2c	Bridge between bit line and ctop
BWC3s	BWC3c	Bridge between word line and rtop
BWC4s	BWC4c	Bridge between word line and ctop
BWC5s	BWC5c	Bridge between ctop and rtop

Bridge between two memory cells (BBC)

To describe all bridges possible between two memory cells, we refer again to Figure 3 where the different nodes in the cell are given names. There are 4 nodes in the cell with the names BL, WL, rtop and ctop. A number between 1 and 4 is added to every node name to indicate the cell each node belongs to. If all bridges are to be considered, every node in one cell on BT and BC should be bridged with every other node in one cell on the same bit line and one cell on the complementary bit line. Here, bridges among word lines, among bit lines, and between word lines and bit lines are excluded. Bridges between bit lines and cells are considered as bridges within cells. A list of the BBC defects is given in Table 3.

5 Simulation results

This section discusses the electrical level simulation employed to establish FFMs caused by bridges. The behavior of the *e*DRAM is studied after injecting and simulating each of the bridges defined in Section 4.2. The bridge impedance has a resistive and a capacitive component that are connected in parallel between the two defective nodes. The bridge resistance (R_{br}) is taken to change from 0 Ω to ∞ Ω, while the bridge capacitance (C_{br}) is varied between 0 F and C_b. The bridge capacitor is initialized to a voltage consistent with the initial voltages of the defective nodes.

For each value of R_{br} and C_{br}, all the SOS's associated with the *targeted* FPs defined in Section 3 are performed and inspected for proper functionality. As a result, the faulty behavior resulting from the analysis of bridges is represented as regions on the (C_{br}, R_{br}) plain. In the following, an example of the simulation results of a bridge between cells is shown first, followed by the results of a bridge within a cell. The simulation results given next are a bit simplified so that insight into the shown figures is not lost.

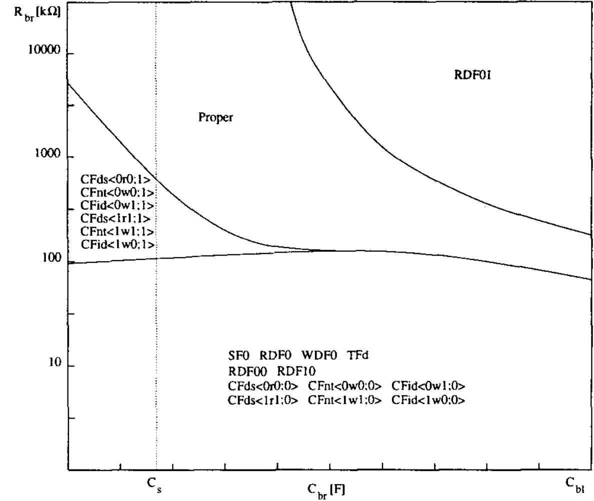

Figure 4. Summary of the fault analysis results for the BBC1s bridge on the (C_{br}, R_{br}) plane under $T = 27°$ C.

5.1 Bridge between cells

The results of the fault analysis performed on BBC1s (bridge between word line and rtop nodes of two memory cells) are shown in Figure 4. According to the figure, the faulty behavior of BBC1s depends on both R_{br} and C_{br}. There are three fault regions shown in the figure, listed next with increasing R_{br} value.

1. Fault region $SF_0 \cup RDF_0 \cup WDF_0 \cup TF\downarrow \cup RDF_{00} \cup RDF_{10} \cup CFds_{0r0;0} \cup CFnt_{0w0;0} \cup CFid_{0w1;0} \cup CFds_{1r1;0} \cup CFnt_{1w1;0} \cup CFid_{1w0;0}$
2. Fault region $CFds_{0r0;1} \cup CFnt_{0w0;1} \cup CFid_{0w1;1} \cup CFds_{1r1;1} \cup CFnt_{1w1;1} \cup CFid_{1w0;1}$
3. Fault region RDF_{01}

The figure shows a relatively simple faulty behavior of the bridge defect BBC1s as compared with other analyzed bridge defects. For $C_{br} = 0$ F and an increasing R_{br}, the number of failing SOS's decreases until the memory starts to function properly with $R_{br} > 5$ MΩ. On the other hand, the faulty behavior is also dependent on the value of C_{br}, such that for increasing C_{br} the region of proper operation decreases gradually in size. Note that the faulty behavior changes gradually with no new fault regions appearing as long as $C_{br} < 2C_s$.

Table 3. List of possible bridge defects between memory cells (BBC) classified into five defect classes.

Simulated BBC		Complementary BBC		Reverse BBC		Reverse complementary BBC		Aggressor-sided complementary BBC		Reverse aggressor-sided BBC	
BBC1s	WL2-rtop0	BBC1c	WL3-rtop1	BBC1r	WL0-rtop2	BBC1rc	WL1-rtop3	BBC1a	WL1-rtop0	BBC1ra	WL0-rtop1
BBC2s	WL2-ctop0	BBC2c	WL3-ctop1	BBC2r	WL0-ctop2	BBC2rc	WL1-ctop3	BBC2a	WL1-ctop0	BBC2ra	WL0-ctop1
BBC3s	rtop0-rtop2	BBC3c	rtop1-rtop3					BBC3a	rtop0-rtop1		
BBC4s	rtop0-ctop2	BBC4c	rtop1-ctop3	BBC4r	rtop2-ctop0	BBC4rc	rtop3-ctop1	BBC4a	rtop0-ctop1	BBC4ra	rtop1-ctop0
BBC5s	ctop0-rtop2	BBC5c	ctop1-rtop3	BBC5r	ctop2-rtop0	BBC5rc	ctop3-rtop1	BBC5a	ctop0-rtop1	BBC5ra	ctop1-rtop0
BBC6s	ctop0-ctop2	BBC6c	ctop1-ctop3					BBC6a	ctop0-ctop1		
BBC7s	WL0-rtop2	BBC7c	WL1-rtop3	BBC7r	WL2-rtop0	BBC7rc	WL3-rtop1	BBC7a	WL0-rtop1	BBC7ra	WL1-rtop0
BBC8s	WL0-ctop2	BBC8c	WL1-ctop3	BBC8r	WL2-ctop0	BBC8rc	WL3-ctop1	BBC8a	WL0-ctop1	BBC8ra	WL1-ctop0

It is interesting to note that for any C_{br} value, there is a R_{br} for which the memory behaves properly. In other words, despite the presence of a defect, given combinations of R_{br} and C_{br} values can neutralize the faulty effect of the bridge and result in a properly operational memory (at least for the used SOS's).

The fault region RDF_{01} is an interesting region because it only shows dynamic faulty behavior, but no static faults. In this region, the sequence $0w1r1$ succeeds at first in writing a 1 but the subsequent read results in a faulty 0 on the output and leaves a stored 0 within the cell. This fault is mainly caused by the high value of C_{br} which shares the voltage of a write 1 operation with the storage capacitor, resulting in storing a weak 1 into the cell. When a read is performed afterwards, the sense amplifier fails to detect this weak 1 value and senses a 0 instead. The fact that only a dynamic fault is sensitized means that in order to detect the faulty behavior of this region, tests should be used that specificly target dynamic faults.

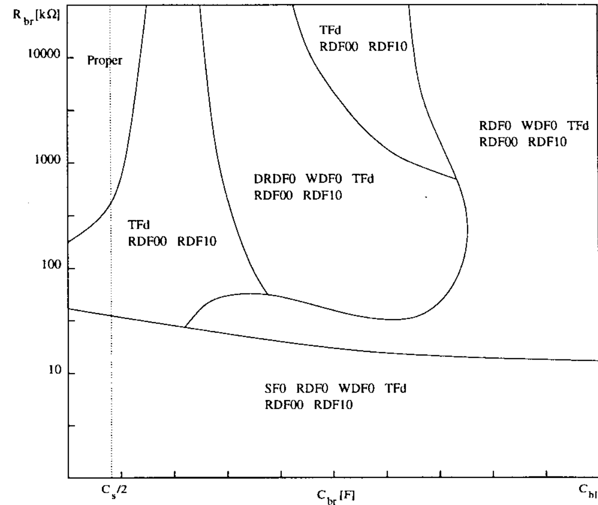

Figure 5. Summary of the fault analysis results for BWC1s in the (C_{br}, R_{br}) plane under $T = 27°$ C.

5.2 Bridge within a cell

The results of the fault analysis performed on BWC1s (bridge between bit line and rtop node) are shown in Figure 5 (TFd in the figure stands for TF↓). According to the figure, the faulty behavior of BWC1s is a rather complex function of both C_{br} as well as R_{br}. There are 4 fault regions shown in the figure that are listed next with increasing R_{br} value.

1. Fault region $SF_0 \cup RDF_0 \cup WDF_0 \cup TF\downarrow \cup RDF_{00} \cup RDF_{10}$
2. Fault region $TF\downarrow \cup RDF_{00} \cup RDF_{10}$
3. Fault region $DRDF_0 \cup WDF_0 \cup TF\downarrow \cup RDF_{00} \cup RDF_{10}$
4. Fault region $RDF_0 \cup WDF_0 \cup TF\downarrow \cup RDF_{00} \cup RDF_{10}$

The figure shows that if $C_{br} = 0$ F and for increasing R_{br}, the number of faulty SOS's decreases until the memory starts to function properly with $R_{br} > 200$ kΩ. As C_{br} increases, the region of proper operation decreases rapidly until it disappears for $C_{br} > C_s$. According to the figure, the faulty behavior of this bridge changes gradually as long as $C_{br} < \frac{C_s}{2}$; this result can be stated for all simulated bridges.

It is interesting to note that the fault region 2 appears twice in the figure, interrupted by the fault region 3. By holding R_{br} at 1 MΩ, for example, and increasing C_{br} gradually from 0 F, we leave the region of proper operation into the fault region 2, then 3, then back to 2, and finally end with the fault region 4. The fault region 3 has the same FFMs as the fault region 2 in addition to $DRDF_0$ and WDF_0. This means that *increasing* the defect capacitance can sometimes *reduce* the number of failing SOS's. A similar observation has been made for the bridge BBC1s (see Figure 4).

Table 4. Summary of the sensitized single-cell FFMs for each one of the analyzed bridge defects.

Bridge	Simulated	Complementary
BWC1-2	SF_0, TF↓, WDF_0, RDF_0, $DRDF_0$, RDF_{00}, RDF_{10}	SF_1, TF↑, WDF_1, RDF_1, $DRDF_1$, RDF_{11}, RDF_{01}
BWC3-4	SF_0, TF↓, WDF_0, RDF_1, IRF_1, $DRDF_0$, IRF_{01}, IRF_{11}, $DRDF_{00}$, $DRDF_{10}$	SF_1, TF↑, WDF_1, RDF_0, IRF_0, $DRDF_1$, IRF_{10}, IRF_{00}, $DRDF_{11}$, $DRDF_{01}$
BBC1-2	SF_0, TF↓, WDF_0, RDF_0, RDF_{00}, RDF_{01}, RDF_{10}	SF_1, TF↑, WDF_1, RDF_1, RDF_{11}, RDF_{10}, RDF_{01}

Table 5. Summary of the sensitized two-cell FFMs for each one of the analyzed bridge defects.

Bridge	Simulated	Complementary	Aggressor-sided complementary
BBC1-2	$CFds_{0r0;0}$, $CFds_{1r1;0}$, $CFds_{0w0;0}$, $CFds_{1w1;0}$, $CFds_{0w1;0}$, $CFds_{1w0;0}$, $CFds_{0r0;1}$, $CFds_{1r1;1}$, $CFds_{0w0;1}$, $CFds_{1w1;1}$, $CFds_{0w1;1}$, $CFds_{1w0;1}$	$CFds_{1r1;1}$, $CFds_{0r0;1}$, $CFds_{1w1;1}$, $CFds_{0w0;1}$, $CFds_{1w0;1}$, $CFds_{0w1;1}$, $CFds_{1r1;0}$, $CFds_{0r0;0}$, $CFds_{1w1;0}$, $CFds_{0w0;0}$, $CFds_{1w0;0}$, $CFds_{0w1;0}$	$CFds_{1r1;0}$, $CFds_{0r0;0}$, $CFds_{1w1;0}$, $CFds_{0w0;0}$, $CFds_{1w0;0}$, $CFds_{0w1;0}$, $CFds_{1r1;1}$, $CFds_{0r0;1}$, $CFds_{1w1;1}$, $CFds_{0w0;1}$, $CFds_{1w0;1}$, $CFds_{0w1;1}$
BBC3-6	$CFst_{0;1}$, $CFrd_{0;1}$, $CFds_{0r0;1}$, $CFds_{1w1;0}$, $CFds_{0w1;0}$, $CFds_{1w0;1}$	$CFst_{1;0}$, $CFrd_{1;0}$, $CFds_{1r1;0}$, $CFds_{0w0;1}$, $CFds_{1w0;1}$, $CFds_{0w1;0}$	$CFst_{1;1}$, $CFrd_{1;1}$, $CFds_{1r1;1}$, $CFds_{0w0;0}$, $CFds_{1w0;0}$, $CFds_{0w1;1}$

6 Discussing simulation results

All bridges defined in Section 4.2 have been injected, simulated and analyzed. The analysis results of bridges are organized in figures depicting a part of the (C_{br}, R_{br}) plane [Al-Ars99]. In the following, the faulty behavior revealed by these results is discussed.

Table 4 gives a summary of the observed single-cell FFMs for all analysed bridge defects. The first column in the table specifies the names of the bridges (in case more than one defect sensitize the same FFMs, they are listed together), while the second and third columns list the FFMs observed for the simulated and complementary instances of these defects, respectively. Inspecting the table reveals that all single-cell FFMs defined in Section 3 are present.

The table shows that bridges between any node and both sides of the track resistance within cells cause the same faulty behavior. The table also shows that defects not only cause static FFMs, but also result in 2-operation dynamic FFMs, which indicates the significance of dynamic fault analysis. It is important from a testing point of view to state the observed fault regions that only show dynamic faulty behavior, since for these regions testing for static faulty behavior cannot detect the defect. The only regions with strict dynamic single-cell FFMs belong to BBC1 and BBC2, where for approximately $R_{br} > 400$ kΩ and $C_{br} > 3C_s$ only RDF_{01} and RDF_{10} can be detected (see Figure 4).

Table 5 lists the observed two-cell FFMs as a result of simulated bridges. The first column in the table lists the defect name, the second lists the simulated faulty behavior, the third lists the complementary behavior, while the fourth lists the aggressor-sided complementary faulty behavior. The table shows that the following static two-cell FFMs have not been observed. $CFst_{0;0}$, $CFrd_{0;0}$, all CFtrs, all CFwds, all CFirs and all CFdrs. Moreover, none of the targeted dynamic two-cell FFMs have been observed. This can be explained by the fact that not all possible two-cell dynamic SOS's have been used, but only those that begin with a write operation followed by a read operation on the victim (see Section 3.5). Since no write operation on the victim results in a coupling fault, it is not expected that a subsequent read operation would cause a coupling fault either.

7 Conclusions

In this paper, the faulty behavior of an *e*DRAM has been analyzed using bridge injection and circuit simulation. The fault analysis has not been restricted to the static memory behavior, but the 2-operation dynamic behavior has also been included. Known static FFMs have been observed and related to given bridges in the memory. New static FFMs (SF_x and WDF_x) and a number of new dynamic FFMs (RDF_{xy}, IRF_{xy} and $DRDF_{xy}$) have been introduced and established for bridges. The analysis showed that dynamic faulty behavior can take place in the absence of static faulty behavior which indicates the importance of dynamic fault analysis.

References

[Adams96] R.D. Adams and E.S. Cooley, "Analysis of a Deceptive Destructive Read Memory Fault Model and Recommended Testing," *in Proc. IEEE North Atlantic Test Workshop*, 1996.

[Al-Ars99] Z. Al-Ars, *Analysis of The Space of Functional Fault Models and Its Application to Embedded DRAMs*, Technical Report No. 1-68340-28(1999)-07, CARDIT, Delft University of Technology, Delft, the Netherlands, 1999.

[Dekker90] R. Dekker *et al.*, "A Realistic Fault Model and Test Algorithms for Static Random Access Memories," *in IEEE Trans. on Computers*, vol. C-9, no. 6, 1990, pp. 567–572.

[Naik93] S. Naik, F. Agricola and W. Maly, "Failure Analysis of High Density CMOS SRAMs," *in IEEE Design and Test of Computers*, vol. 10, no. 2, 1993, pp. 13–23.

[Schanstra99] I. Schanstra and A.J. van de Goor, "Industrial Evaluation of Stress Combinations for March Tests applied to SRAMs," *in Proc. IEEE Inter. Test Conf.*, 1999, pp. 983–992.

[vdGoor98] A.J. van de Goor, *Testing Semiconductor Memories, Theory and Practice*, ComTex Publishing, Gouda, the Netherlands, 1998, e-mail: vdGoor@cardit.et.tudelft.nl

[vdGoor99] A.J. van de Goor and J. de Neef, "Industrial Evaluation of DRAM Tests," *in Proc. Design, Automation and Test in Europe*, 1999, pp. 623–630.

[vdGoor00] A.J. van de Goor and Z. Al-Ars, "Functional Memory Faults: A Formal Notation and a Taxonomy," *in Proc. IEEE VLSI Test Symp.*, 2000, pp. 281–289.