Industrial Evaluation of DRAM SIMM Tests

Ad J. van de Goor Alexander Paalvast
Delft University of Technology, Faculty of Information Technology and Systems
Department of Electrical Engineering, Section Computer Architecture and Digital Technique
Mekelweg 4, 2628 CD Delft, The Netherlands
E-mail: A.J.vdGoor@its.tudelft.nl

Abstract

This paper describes the results of testing 50 single in-line memory modules (SIMMs), each containing 16 16Mbit DRAM chips (DUTs); 39 SIMMs failed, and of the 800 DUTs, 116 failed. In total 54 different test algorithms have been applied, using up to 168 different stress combinations for each test. The results show that GAL9R is the best test. Furthermore, it is shown that burst mode tests detect a completely different class of faults as compared with traditional word mode tests, and that tests with address scrambling enabled detect more faults.

Keywords: Memory tests, stress combination, fault coverage, data background, scrambling.

1. Introduction

DRAM production tests currently are required to have a PPM level which approaches the single digit numbers. This implies that a single memory test is not sufficient; a set of tests has to be used. In addition, in order to obtain economically acceptable test times, the set of tests has to be optimized for the particular technology used, requiring manual optimization of the test set.

Much work has been done on designing memory tests [4] [7] [1] [3] optimized to detect a particular class of faults, which may have an academic origin or is based on inductive fault analysis and SPICE simulation. The question remains as how effective these tests are. [11] has applied a small set of tests to 2K*8 SRAMs and found that the fault coverage was heavily dependent on the used data backgrounds and address orders. [5] reports results of testing 1024 128K*8 SRAM chips using a small number of tests; the results indicated that the fault coverage was heavily dependent on the used stresses such as the load used on the output pins, and/or on the power supply voltage.

[10] reports industrial results of applying a number of tests, under different stresses, to SRAMs. [2] describes results of applying a large number of tests, using a large number of stresses, to DRAMs.

This paper is an extension of the work performed in [2]; a large number of new tests have been performed, the number of used data backgrounds has been increased, etc.; while the tests have been applied to SIMMs, populated with DRAMs, using word mode as well as burst mode addressing. In addition, it should be noted that the tested SIMMs all passed the Advantest based production test; however, they failed in the PC. This means that the DUTs contain faults which are very hard to detect [8].

This paper presents the results of a set of 54 tests, applied to 50 *Single In-line Memory Modules (SIMMs)*, each containing 16 4Mx4 DRAM chips. A total of $50 \times 16 = 800$ chips (DUTs) have been tested. A *test* consists of a *base test (BT)* applied using a particular *stress combination (SC)*. An SC consists of a combination of values for the different *stresses*; e.g.; $V_{CC} = 4.6V$, Load =50%, etc. BTs have been performed with up to 168 different SCs.

The organization of the paper is as follows: Section 2 gives an overview of the used BTs and stresses, Section 3 describes the results of the tests, while Section 4 presents an optimized set of tests, and Section 5 ends with conclusions.

2. Used base tests and stresses

Section 2.1 gives an overview of the used BTs, while the stresses (which are the components of an SC) are described in Section 2.2.

2.1. Overview of the used base tests

Table 1 gives a list of the base tests used, their algorithm and their complexity. The table has the following columns:

1. #: This is the *test number* of the base test (BT) as used in the remainder of this paper.

Table 1. Base test algorithms

#	Grp	Base test	Algorithm	Length
1,3	1	BuWRx	$\{\Uparrow (wx, rx)\}$ (1: x=0; 3: x=1)	$2n$
2,4	1	BdWRx	$\{\Downarrow (wx, rx)\}$ (2: x=0; 4: x=1)	$2n$
5,7	2	BuW-Rx	$\{\Uparrow (wx); \Uparrow (rx)\}$ (5: x=0; 7: x=1)	$2n$
6,8	2	BdW-Rx	$\{\Downarrow (wx); \Downarrow (rx)\}$ (6: x=0; 8: x=1)	$2n$
9,11	3	BuWRWx	$\{\Uparrow (wx); \Uparrow (rx, w\overline{x})\}$ (9: x=0; 11: x=1)	$3n$
10,12	3	BdWRWx	$\{\Downarrow (wx); \Downarrow (rx, w\overline{x})\}$ (10: x=0; 12: x=1)	$3n$
13,15	4	BuWRWx	$\{\Uparrow (wx); \Uparrow (rx, wx)\}$ (13: x=0; 15: x=1)	$3n$
14,16	4	BdWRWx	$\{\Downarrow (wx); \Downarrow (rx, wx)\}$ (14: x=0; 16: x=1)	$3n$
17,19	5	BuWDx	$\{\Uparrow (wx); \Uparrow (rx, w\overline{x}, r\overline{x})\}$ (17: x=0; 19: x=1)	$4n$
18,20	5	BdWDx	$\{\Downarrow (wx); \Downarrow (rx, w\overline{x}, r\overline{x})\}$ (18: x=0; 20: x=1)	$4n$
21	6	SCAN	$\{\Uparrow (w0); \Uparrow (r0); \Uparrow (w1); \Uparrow (r1)\}$	$4n$
22	6	MATS+ 1	$\{\Updownarrow (w0); \Uparrow (r0, w1); \Downarrow (r1, w0)\}$	$5n$
23	6	MATS+ 2	$\{\Updownarrow (w0); \Uparrow (r0, w1); \Downarrow (r1, w0)\}$	$5n$
24	6	March C-	$\{\Updownarrow (w0); \Uparrow (r0, w1); \Uparrow (r1, w0); \Downarrow (r0, w1); \Downarrow (r1, w0); \Downarrow (r0)\}$	$10n$
25	6	PMOVI	$\{\Downarrow (w0); \Uparrow (r0, w1, r1); \Uparrow (r1, w0, r0); \Downarrow (r0, w1, r1); \Downarrow (r1, w0, r0)\}$	$13n$
26	6	March Y	$\{\Updownarrow (w0); \Uparrow (r0, w1, r1); \Downarrow (r1, w0, r0); \Updownarrow (r0)\}$	$8n$
27	6	March LA	$\{\Updownarrow (w0); \Uparrow (r0, w1, w0, w1, r1); \Uparrow (r1, w0, w1, w0, r0);$ $\Downarrow (r0, w1, w0, w1, r1); \Downarrow (r1, w0, w1, w0, r0); \Downarrow (r0)\}$	$22n$
28	7	Marching 1/0	$\{\Uparrow (w0); \Uparrow (r0, w1, r1); \Downarrow (r1, w0, r0); \Uparrow (w1); \Uparrow (r1, w0, r0); \Downarrow (r0, w1, r1)\}$	$14n$
29	7	March Y-R	$\{\Uparrow (w0); \Uparrow (r0, w1, r1, r1); \Downarrow (r1, w0, r0, r0)\}$	$9n$
30	7	March Y-RR	$\{\Uparrow (w0); \Uparrow (r0, w1, r1, r1, r1); \Downarrow (r1, w0, r0, r0, r0)\}$	$11n$
31	7	March C-R	$\{\Uparrow (w0); \Uparrow (r0, r0, w1); \Uparrow (r1, r1, w0); \Downarrow (r0, r0, w1); \Downarrow (r1, r1, w0); \Downarrow (r0, r0)\}$	$15n$
32	7	PMOVI-R	$\{\Downarrow (w0); \Uparrow (r0, w1, r1, r1); \Uparrow (r1, w0, r0, r0); \Downarrow (r0, w1, r1, r1); \Downarrow (r1, w0, r0, r0)\}$	$17n$
33	7	WAW	$\{\Downarrow (w0); \Uparrow (w0, r0, w1); \Uparrow (w1, r1, w0); \Downarrow (w0, r0, w1); \Downarrow (w1, r1, w0)\}$	$13n$
34	7	UARBW	$\{\Uparrow (w0), \Uparrow (r0, w1, r1); \Uparrow (r1, w0, r0); \Uparrow (w1); \Uparrow (r1, w0, r0); \Uparrow (r0, w1, r1); \Downarrow (w0); \Downarrow (r0, w1, r1);$ $\Downarrow (r1, w0, r0); \Downarrow (w1); \Downarrow (r1, w0, r0); \Downarrow (r0, w1, r1)\}$	$28n$
35-38	8		35: SCAN as 21; 36: March C- as 24; 37: PMOVI as 25; 38: March LA as 27	
39	9	DIST	$\{\Uparrow (w0);\ {}_R\Uparrow_{z=0}^{R-1} (T_{REF}(c\Uparrow_{r=z+1} (w1)); Ref;_{C\Uparrow_{r=z+1}}(w0);\ c\Uparrow_{r=z} (r0)); \Uparrow (w1);$ ${}_R\Uparrow_{z=0}^{R-1} (T_{REF}(c\Uparrow_{r=z+1} (w0)); Ref;_{C\Uparrow_{r=z+1}}(w1);\ c\Uparrow_{r=z} (r1))\}$	$8n + t^1$
40	9	DISTW	$\{\Uparrow (wB);_R\Uparrow_{z=0}^{R-1} (c\Uparrow_{r=z} (rB); T_{REF}(c\Uparrow_{r=z} (wD)); Ref;_{C\Uparrow_{r=z-1}}(rB);_{C\Uparrow_{r=z+1}} (rB);$ $c\Uparrow_{r=z} (rD, wB)); \Uparrow (w\overline{B});_R\Uparrow_{z=0}^{R-1} (c\Uparrow_{r=z} (r\overline{B}); T_{REF}(c\Uparrow_{r=z} (w\overline{D})); Ref;_{C\Uparrow_{r=z-1}} (r\overline{B});$ $c\Uparrow_{r=z+1} (r\overline{B});_{C\Uparrow_{r=z}} (r\overline{D}, w\overline{B}))\}$ with $(D = \overline{B})$	$14n + t$
41	9	DISTW1	As 40, but with $D = B$	$14n + t$
42	9	DISTR	$\{\Uparrow (wB);_R\Uparrow_{z=0}^{R-1} (c\Uparrow_{r=z} (wD); T_{REF}(rD_{r=z}); Ref;_{C\Uparrow_{r=z-1}} (rB);_{C\Uparrow_{r=z+1}} (rB);_{C\Uparrow_{r=z}} (wB));$ $\Uparrow (w\overline{B});_R\Uparrow_{z=0}^{R-1} (c\Uparrow_{r=z} (w\overline{D}); T_{REF}(r\overline{D}_{r=z}); Ref;_{C\Uparrow_{r=z-1}} (r\overline{B});_{C\Uparrow_{r=z+1}} (r\overline{B});_{C\Uparrow_{r=z}} (w\overline{B}))\}$ with $(D = \overline{B})$	$12n + t$
43	9	DISTR1	As 42, but with $D = B$	$12n + t$
44	10	Butterfly	$\{\Uparrow (w0); \Uparrow_b (w1_b, \diamond(r0), w0_b); \Uparrow (w1); \Uparrow_b (w0_b, \diamond(r1), w1_b)\}$	$14n$
45	10	GAL5R	$\{\Uparrow (w0); \Uparrow_b (w1_b, \diamond(r0, r1_b), w0_b); \Uparrow (w1); \Uparrow_b (w0_b, \diamond(r1, r0_b), w1_b)\}$	$22n$
46	10	GAL5W	$\{\Uparrow (w0); \Uparrow_b (w1_b, \diamond(w0, r1_b), w0_b); \Uparrow (w1); \Uparrow_b (w0_b, \diamond(w1, r0_b), w1_b)\}$	$22n$
47	10	GAL9R	$\{\Uparrow (w0); \Uparrow_b (w1_b, \square(r0, r1_b), w0_b); \Uparrow (w1); \Uparrow_b (w0_b, \square(r1, r0_b), w1_b)\}$	$38n$
48	10	GAL9W	$\{\Uparrow_b (w0_b); \Uparrow_b (w1, \square(w0, r1_b), w0_b); \Uparrow (w1); \Uparrow_b (w0_b, \square(w1, r0_b), w1_b)\}$	$38n$
49-54	11		49: SCAN as 21; 50: March Y as 26; 51: March C- as 24; 52: PMOVI as 25; 53: Marching 1/0 as 28; 54: March LA as 27	

[1] $t = 2\sqrt{n} \cdot T_{REF}$, or the total time spent hammering the aggressor row.

2. Grp: This is the group number of the BT. A *group* consists of a set of related tests, or is a set of BTs applied using the same set of stress conditions (SCs).
3. Base test: The name of the BT.
4. Algorithm.
5. Length: The number of operations required to apply the BT for a single SC.

For instance, BT 13 is called "BuWRW0" (it is the test BuWRWx with x=0) and has algorithm $\{\Uparrow (w0); \Uparrow (r0, w0)\}$, which has a test length of $3n$; where n is the number of words in the memory array, $\Uparrow$ denotes an increasing address order, $\Downarrow$ denotes a decreasing address order, while $\Updownarrow$ denotes that the to be used address order can be chosen arbitrarily to be $\Uparrow$ or $\Downarrow$.

The used set of 54 BTs is composed of BTs from the following groups (The number between brackets shows the number of BTs the group consists of, while the acronyms *SE* and *SNE* respectively denote whether *scrambling is enabled* or *not enabled* for this group of tests. SE means that a scrambling table has been used during the test to guarantee that adjacent logical addresses are also topologically adjacent [1]):

1. Groups 1-5: Basic march tests (20; SNE)
Basic march tests are very simple march tests. Because of their simplicity they can be used to establish the type of fault occurring in the memory[10]. Each line in the table specifies two similar BTs; e.g., line 2, with # 2,4 specifies the BTs BdWR0 and BdWR1. The character 'd' in BdWR0 means that the $\Downarrow$ address order is used.

2. Groups 6-8: March tests (18; 6-7 SNE, 8 SE)
March tests are very popular tests for functional faults such as address decoder faults, coupling faults, etc [1]. The MATS+ test occurs twice (once denoted as MATS+1 and once as MATS+2), to verify the repeatability of memory

tests. Some of the BTs of Group 7 have a suffix 'R' or 'RR' indicating that their march elements contain one or two extra read operations; this can be verified by inspecting the corresponding algorithm. The WAW test has especially been designed for detecting Write-After-Write recovery faults; while the UARBW test has been taken from an IBM patent on memory BIST [6]. The BTs of Group 8 are identical to the BTs of Group 6; however, they are performed with scrambling enabled.

3. Group 9: Disturb tests (5; SE)

These tests are based on [9]. The assumed fault model is that of a data retention fault linked with a coupling fault: a certain cell has a higher than average leakage (however it passes the regular refresh tests); due to a coupling effect with a neighboring row (This can be with a bit-line, a word-line or a cell in the neighboring row), the leakage is accelerated when the neighboring row has the appropriate logic value. This can be accomplished by repeatedly reading/writing the appropriate value from/into a cell in a neighboring row (called the *aggressor row*). This means that for each row in the memory cell array, a neighboring row will repeatedly be read/written for a duration of T_{REF} sec.

The notation ${}_R\Uparrow_{z=0}^{R-1}(T_{REF}({}_C\Uparrow_{r=z+1}(w1))$, see #39 of Table 1, means: ${}_R\Uparrow_{z=0}^{R-1}$ row addressing used for row z=0 to row z=R-1; for each row, for a time period of T_{REF} sec. the operation ${}_C\Uparrow_{r=z+1}(w1)$ is performed, which means that a w1 operation is performed to all columns of row r=z+1.

The Ref symbol denotes a refresh of the entire array. The DIST (DISTurb) test (#39) performs its disturbing operation by repeatedly writing all columns of the aggressor row for a time period T_{REF}; this is done by the march elements ${}_C\Uparrow_{r=z+1}(w1)$ and ${}_C\Uparrow_{r=z+1}(w0)$. Note that row 'z+1' is the aggressor row, while row 'z' is the victim row. The *data background (DB)* used by DIST is all 0s and all 1s. In BTs 40-43 a DB B is used to write the entire array with background data, while a disturb pattern D is written into or read from the aggressor row. The DISTW and DISTW1 BTs perform write operations to the aggressor row, while the DISTR and DISTR1 BTs perform read operations. Note, that the tests DISTW and DISTW1 appear similar. The difference is in the used DBs for the victim row (B for Background pattern) and the aggressor row (D for Disturb pattern). For DISTW, $D = \overline{B}$, while for DISTW1 $D = B$. The same applies to DISTR and DISTR1.

4. Group 10: Base cell tests (5; SE)

This group of BTs has been designed to detect the influence of a disturbance of the base cell on other cells, or vise versa [1]. Butterfly is described in [1]. The march element $\Uparrow_b(w1_b, \diamond(r0), w0_b)$ means that a $w1$ is performed to some base cell, thereafter a $r0$ is performed from the North, East, South and West (N,E,S,W) neighbor (indicated by the $\diamond$ symbol), and last a $w0$ is performed to the base cell.

The tests GAL5R-GAL9W are simplified versions of the GALPAT test [1]. The '$\diamond$' symbol denotes operations performed on the N, E, S and W neighbor of the base cell; the '$\square$' denotes that operations are performed on the 8 neighbors of the base cell. The GAL5R march element $\Uparrow_b(w1_b, \diamond(r0, r1_b))$ performs the following operations: a w1 is performed to the base-cell; thereafter a r0 is performed on the N neighbor of the base-cell, after which an r1 is performed on the base-cell (these are the r0,r1$_b$ operations). The r0,r1$_b$ operations are thereafter performed on the E, S, and W neighbors of the base-cell. The difference between the GAL5R/GAL9R and the GAL5W/GAL9W BTs is that the first 2 BTs perform read operations to the $\diamond$/$\square$ neighbor cells, while the GAL5W/GAL9W perform write operations to the $\diamond$/$\square$ neighbor cells.

5. Group 11: 2^i tests (6; SE)

These are the same BTs as those of Group 6, except they are $\mathcal{O}(nlog_2n)$ tests because they are repeatedly applied with address increments of 2^i [1][2].

2.2. Used stresses

A *stress* can be *a refinement of a certain operation* of a BT (e.g., the address order or the to-be-written data), or can be *an external condition* applied to the *Device Under Test (DUT)* with the intent to make faults easier detectable. To the latter stress class belong timing, voltage and load stress.

Table 2 shows the stresses for each group of BTs. For instance, for Group 6 (march tests) there are 2 (Load=50,100) $\times$7 (all 7 DBs) $\times$2 (V_{cc}=-V,+V) $\times\{$2 (Addr=xA,yA) $\times$2 (Timing=-T,+T) +2 (pA,qA) $\times$1 (only 1 timing stress for burst mode)$\}$ = 168 possible SCs, as denoted in the column "SC Total". Note that the addressing and timing stresses are divided into two columns: one for word mode and one for burst mode. This is done, because burst mode only allows one timing stress, while word mode allows two.

Below the used stresses are itemized; note that all tests have been performed at room temperature ($\approx$ 20°C).

1. Address stress
   - xA Fast X (word mode): Inc./Dec. column address by 1
   - yA Fast Y (word mode): Inc./Dec. row address by 1
   - pA Fast X (burst mode, burst length is 4 words)
   - qA Fast Y (burst mode, burst length is 4 words)
   - iA Fast X (2^i): Inc./Dec. column address by 2^i
   - jA Fast Y (2^i): Inc./Dec. row address by 2^i
   - -A Addressing of DIST tests. (See Table 1)
2. Data background (DB) stress
   - sD Solid: All 0s, all 1s
   - bD Checkerboard: 01010.../1010...
   - rD Row stripe: 0000.../1111...
   - cD Column stripe: 0101...
   - bbD Double Checkerboard: 0011.../0011.../1100.../1100...
   - rrD Double Row stripe: 0000.../0000.../1111.../1111...
   - ccD Double Column stripe: 0011...

Table 2. Stresses per group of BTs

Grp	Stress conditions: Load	DB	V_{CC}	Word mode: Addr	Word mode: Timing	Burst Addr[1]	SC Total[2]
1	50,100	All	-V,+V	xA,yA	-T,+T	pA,qA	168
2	50,100	All	-V,+V	xA,yA	-T,+T	pA,qA	168
3	50,100	All	-V,+V	xA,yA	-T,+T	pA,qA	168
4	50,100	All	-V,+V	xA,yA	-T,+T	pA,qA	168
5	50,100	All	-V,+V	xA,yA	-T,+T	pA,qA	168
6	50,100	All	-V,+V	xA,yA	-T,+T	pA,qA	168
7	50,100	All	-V,+V	xA,yA	+T	pA,qA	112
8	50,100	All	-V,+V	xA,yA	+T	pA,qA	112
9	50,100	bD	-V,+V	-A	+T		4
10	50	All	-V,+V	xA,yA	+T		28
11	50	bD	-V,+V	iA,jA	+T		4

[1]Burst addressing always uses fT Timing.
[2]SC Total = #Load × #DB × #V_{CC} × (#Addr × #Timing + #Burst addr)

3. Timing stress
   - -T Use minimum RAS to CAS delay $T_{RCD} = 20ns$
   - +T Use maximum $T_{RCD} = 45ns$
   - fT Use burst mode timing; $T_{RCD} = 30ns$
4. Voltage stress
   - -V V_{CC}-min $= 4.6V$
   - +V V_{CC}-max $= 5.4V$
5. Load Stress (The load on the signal pins)
   - 50L 50% load: 2 TTL loads + 100 pF
   - 100L 100% load: 4 TTL loads + 200 pF

3. Test results

The total number of tests applied is 5952; which is the sum of the number of tests in each Grp, in Table 2, multiplied with the corresponding "SC Total" value. The application of these 5952 tests to 800 DUTs resulted in 4,761,600 pass/fail values. The total test time per SIMM for all 54 applied BTs with their SCs was 12 hours and 48 min.

This section describes the results of applying the tests to the 50 SIMMs, of which only 39 have been detected to be faulty. This means that the used BTs, or more likely the used SCs did not allow for 100% *fault coverage (FC)*. The results are presented in five subsections.

3.1. Analysis of BTs

Table 3 shows the *intersections* of the groups of BTs; which are the common defects detected by tests of 2 groups of tests. The first three columns list: the group number, the # of BTs in this group, and the # of SCs used with each BT; the remainder of the columns show the intersections. For instance, the intersection of Group 2 and 7 is 13; which means that 13 DUTs are detected to be faulty by the tests of Group 2 *and* of Group 7. The bold numbers on the diagonal denote the FC of a group. Therefore, the FC of Group 2 is 16 and the FC of Group 7 is 43. Of the 16 DUTs detected by Group 2, 13 are also detected by Group 7.

The groups with the highest FC are: Group 9 (Disturb test, FC=70) and Group 10 (Base cell tests, FC=65). The

Table 3. Intersections of groups of BTs

Grp	BTs	SCs	1	2	3	4	5	6	7	8	9	10	11
1	4	168	**2**	2	2	2	2	2	2	2	2	2	2
2	4	168	2	**16**	13	11	13	15	13	15	13	12	10
3	4	168	2	13	**17**	13	15	17	16	16	15	14	11
4	4	168	2	11	13	**14**	12	14	14	14	11	12	9
5	4	168	2	13	15	12	**20**	19	19	17	16	16	14
6	7	168	2	15	17	14	19	**38**	34	35	31	34	30
7	7	112	2	13	16	14	19	34	**43**	36	30	36	30
8	4	112	2	15	16	14	17	35	36	**55**	37	40	34
9	6	4	2	13	15	11	16	31	30	37	**70**	39	32
10	5	28	2	12	14	12	16	34	36	40	39	**65**	41
11	6	4	2	10	11	9	14	30	30	34	32	41	**46**

following groups are completely covered by other groups: Group 1 is covered by Groups 2-11 (which is not surprising), Group 3 (FC=17) is covered by Group 6 (because the intersection of Group 3 and Group 6 is 17), and Group 4 is covered by Groups 6-8. None of the Groups 5-11 are covered by any other group.

The analysis below shows which *individual BTs* are covered by other BTs. It is based on tables of the intersections of pairs of BTs; see Table 4. The first column of the table shows the test number; the second column the group number. The column "FC" is the FC of the corresponding BT. The BT with the highest FC is GAL9R (FC=61), second highest is DISTR (FC=51), and third is GAL5R (FC=50).

The intersection of each pair of BTs is shown in the remainder of the table. The bold diagonal entries show the FC of the corresponding BTs; which is also listed in the column "FC". For instance, the intersection of tests BuWD0 (#17) and BdW-R0 (#6) is at row 17, column 6 and is 10. This means that both tests cover 10 of the same DUTs.

Note that it is possible to calculate the *union* from the intersection table; this is the total FC of two tests together. Consider the example of BuWD0 (#17) with FC=15 and BdW-R0 (#6) with FC=12; the intersection is 10, and the union of these two tests is: 15+12-10=17.

From Table 4, it is possible to see which BTs cover a specific BT. For instance, the test BuWR0 (#1) detects only 1 DUT, as can be read from the first diagonal element. Almost all other tests have a "1" in column (or row) 1, meaning they cover the DUT detected by BuWR0. March LA (# 27, FC=32) covers many other march tests: SCAN (#21), MATS+1 and MATS+2, and March Y(#26). GAL9R (#47, FC=61) covers GAL5R (as expected), and GAL9W covers GAL5W.

3.2. Analysis of stresses

Table 5 shows the intersections of the 21 used stresses. The column "ST" shows the stress, the column "FC" is the

Table 4. Intersections of BTs

#	Grp	BT	FC	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54
1	1	BuWR0	1	**1**	0	0	0	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2	1	BdWR0	0	0	**0**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3	1	BuWR1	0	0	0	**0**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
4	1	BdWR1	1	0	0	0	**1**	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
5	2	BuW-R0	10	1	0	0	1	**10**	9	6	6	7	7	6	5	4	6	5	5	10	8	6	7	10	9	9	10	9	10	10	8	8	8	9	7	1	9	9	9	9	9	5	6	7	7	8	7	8	3	8	3	8	6	6	8	7	7
6	2	BdW-R0	12	1	0	0	1	9	**12**	7	9	8	10	7	8	5	9	5	8	10	10	7	9	10	9	9	12	12	11	11	8	8	9	11	10	1	11	11	11	10	10	7	7	8	8	9	8	9	3	9	3	7	6	5	7	6	6
7	2	BuW-R1	9	1	0	0	1	6	7	**9**	7	5	6	6	6	4	6	5	6	7	6	8	6	8	6	6	8	8	8	9	7	7	7	8	7	1	8	9	8	9	8	5	6	7	8	8	8	8	3	8	3	6	7	6	7	6	6
8	2	BdW-R1	11	0	0	0	1	6	9	7	**11**	5	7	5	7	3	7	4	7	7	7	7	6	8	6	6	9	10	9	9	7	7	8	10	9	1	10	11	11	9	9	6	6	7	7	7	7	8	2	8	2	6	5	4	6	5	5
9	3	BuWRW01	12	1	0	0	1	7	8	5	5	**12**	9	8	7	8	7	8	6	11	9	8	8	9	12	12	12	12	12	12	11	11	11	11	11	2	11	10	11	11	11	8	10	11	11	12	10	11	7	11	7	9	8	7	9	8	8
10	3	BdWRW01	13	1	0	0	1	7	10	6	7	9	**13**	9	10	6	9	6	9	10	11	8	11	9	10	10	13	13	12	12	9	9	10	12	11	2	12	12	12	11	11	9	9	9	9	10	9	10	6	10	6	8	8	8	8	8	8
11	3	BuWRW10	10	1	0	0	1	6	7	6	5	8	9	**10**	6	6	6	6	8	9	8	8	8	8	9	9	10	10	10	10	8	8	8	9	8	2	9	9	9	9	9	6	7	8	8	9	8	8	5	8	5	7	7	6	7	6	6
12	3	BdWRW10	11	1	0	0	1	5	8	6	7	7	10	6	**11**	5	9	5	7	8	9	8	9	8	7	7	10	11	10	10	8	8	9	11	10	1	11	11	11	10	10	7	8	8	8	8	8	9	5	9	5	7	7	7	7	7	7
13	4	BuWRW0	8	1	0	0	1	4	5	4	3	8	6	6	5	**8**	6	7	6	7	5	6	5	6	8	8	8	8	8	8	8	8	8	8	8	2	8	7	8	8	8	5	7	8	8	8	7	8	5	8	5	6	6	5	6	5	5
14	4	BdWRW0	10	1	0	0	1	6	9	6	7	7	9	6	9	6	**10**	6	8	8	8	7	8	8	7	7	10	10	9	9	7	7	8	10	9	1	10	10	10	9	9	6	6	7	7	7	7	8	4	8	4	6	6	5	6	5	5
15	4	BuWRW1	9	1	0	0	1	5	5	5	4	8	6	6	5	7	6	**9**	6	8	5	7	5	7	9	9	9	8	9	9	9	9	9	9	8	2	9	8	9	9	9	5	7	8	8	8	7	9	6	9	6	7	6	6	7	6	6
16	4	BdWRW1	10	1	0	0	1	5	8	6	7	6	9	8	7	6	8	6	**10**	7	7	7	7	7	7	7	10	10	9	9	7	7	8	10	9	2	10	10	10	9	9	6	6	7	7	7	7	8	**4**	8	4	6	6	5	6	5	5
17	5	BuWD0	15	1	0	0	1	10	10	7	7	11	10	9	8	7	8	8	7	**15**	11	11	10	12	13	13	14	14	14	15	12	12	12	13	12	1	13	12	13	13	13	8	10	11	11	12	10	13	6	13	6	10	9	8	11	9	10
18	5	BdWD0	13	1	0	0	1	8	10	6	7	9	11	8	9	5	8	5	7	11	**13**	8	12	10	10	10	13	13	12	12	10	10	10	12	11	1	12	12	12	11	11	10	10	10	10	11	10	10	5	10	5	9	8	8	9	9	9
19	5	BuWD1	12	1	0	0	1	6	7	8	7	8	8	8	8	6	7	7	7	11	8	**12**	8	9	9	9	10	12	11	12	10	10	10	11	11	1	11	10	11	11	11	6	9	10	10	10	9	11	6	11	6	8	9	7	9	7	8
20	5	BdWD1	14	1	0	0	1	7	9	6	6	8	11	8	9	5	8	5	7	10	12	8	**14**	9	9	9	13	13	12	12	10	9	9	13	11	1	12	11	12	10	11	10	10	10	10	11	10	10	6	10	6	8	9	9	9	9	9
21	6	SCAN	14	1	0	0	1	10	10	8	8	9	9	8	8	6	8	7	7	12	10	9	9	**14**	11	11	13	12	13	14	12	12	11	13	11	1	13	12	13	13	13	8	10	11	11	12	10	12	4	12	4	11	9	9	10	9	10
22	6	MATS+1	18	1	0	0	1	9	9	6	6	12	10	9	7	8	7	9	7	13	10	9	9	11	**18**	18	18	16	15	18	15	13	13	17	13	2	17	15	17	15	17	12	14	16	15	16	15	17	11	17	11	11	13	13	15	14	14
23	6	MATS+2	18	1	0	0	1	9	9	6	6	12	10	9	7	8	7	9	7	13	10	9	9	11	18	**18**	18	16	15	18	15	13	13	17	13	2	17	15	17	15	17	12	14	16	15	16	15	17	11	17	11	11	13	13	15	14	14
24	6	March C-	31	1	0	0	1	10	12	8	9	12	13	10	10	8	10	9	10	14	13	10	13	13	18	18	**31**	22	19	26	20	15	16	27	18	2	25	21	27	21	24	19	20	24	21	22	24	28	16	28	16	14	19	23	20	19	23
25	6	PMOVI	26	1	0	0	1	9	12	8	10	12	13	10	11	8	10	8	10	14	13	12	13	12	16	16	22	**26**	20	24	20	14	16	24	20	2	24	19	23	19	23	15	19	21	19	20	19	23	12	23	12	13	18	16	20	18	18
26	6	March Y	22	1	0	0	1	10	11	8	9	12	12	10	10	8	9	9	9	14	12	11	12	13	15	15	19	20	**22**	22	19	15	17	21	18	2	21	19	21	19	21	12	17	17	18	18	15	20	9	20	9	15	15	15	17	16	16
27	6	March LA	32	1	0	0	1	10	11	9	9	12	12	10	10	8	9	9	9	15	12	12	12	14	18	18	26	24	22	**32**	23	16	17	27	22	2	27	22	27	26	28	17	21	23	23	23	21	29	14	29	14	16	22	22	23	21	24
28	7	March.1/O	30	1	0	0	1	8	8	7	7	11	9	8	8	8	7	9	7	12	10	10	10	12	15	15	20	20	19	23	**30**	17	18	26	21	2	26	18	25	22	26	16	22	23	22	21	21	26	13	26	13	17	20	20	22	21	21
29	7	March Y-R	17	1	0	0	1	8	8	7	7	11	9	8	8	8	7	9	7	12	10	10	9	12	13	13	15	14	15	16	17	**17**	16	17	16	2	17	15	17	17	17	12	15	16	16	16	14	17	8	17	8	15	13	13	14	13	14
30	7	March Y-RR	20	1	0	0	1	8	9	7	8	11	10	8	9	8	8	9	8	12	10	10	9	11	13	13	16	16	17	17	18	16	**20**	19	18	2	19	17	19	18	19	11	17	17	16	15	16	20	8	20	8	16	13	14	16	15	15
31	7	March C-R	35	1	0	0	1	9	11	8	10	11	12	9	11	8	10	9	10	13	12	11	13	13	17	17	27	24	21	27	26	17	19	**35**	24	2	31	24	31	25	31	19	24	26	24	23	24	31	16	31	16	17	22	24	24	23	24
32	7	PMOVI-R	26	1	0	0	1	7	10	7	9	11	11	8	10	8	9	8	9	12	11	11	11	11	13	13	18	20	18	22	21	16	18	24	**26**	2	24	19	23	21	23	15	20	20	20	19	17	24	10	25	10	16	18	16	19	17	18
33	7	WAW	2	0	0	0	1	1	1	1	1	2	2	2	1	2	1	2	2	1	1	1	1	1	2	2	2	2	2	2	2	2	2	2	2	**2**	2	2	2	2	2	1	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2
34	7	UARBW	32	1	0	0	1	9	11	8	10	11	12	9	11	8	10	9	10	13	12	11	12	13	17	17	25	24	21	27	26	17	19	31	24	2	**32**	23	31	25	30	19	24	26	24	23	23	30	16	30	16	18	23	23	25	24	24
35	8	SCAN	28	1	0	0	1	9	11	9	11	10	12	9	11	7	10	8	10	12	12	10	11	12	15	15	21	19	19	22	18	15	17	24	19	2	23	**28**	25	22	23	17	18	18	20	19	19	23	10	23	10	16	18	19	20	19	20
36	8	March C-	40	1	0	0	1	9	11	8	11	11	12	9	11	8	10	9	10	13	12	11	12	13	17	17	27	23	21	27	25	17	19	31	23	2	31	25	**40**	28	32	21	25	27	25	25	25	32	18	32	18	20	24	26	25	24	27
37	8	PMOVI	33	1	0	0	1	9	10	9	9	11	11	9	10	8	9	9	9	13	11	11	10	13	15	15	21	19	19	26	22	17	18	25	21	2	25	22	28	**33**	31	15	19	20	21	21	19	26	12	27	12	18	20	20	21	20	21
38	8	March LA	43	1	0	0	1	9	10	8	9	11	11	9	10	8	9	9	9	13	11	11	11	13	17	17	24	23	21	28	26	17	19	31	23	2	30	23	32	31	**43**	18	26	27	25	24	24	33	16	35	16	19	24	24	25	25	24
39	9	DIST	32	1	0	0	0	5	7	5	6	8	9	6	7	5	6	5	6	8	10	6	10	8	12	12	19	15	12	17	16	12	11	19	15	1	19	17	21	15	18	**32**	29	23	30	24	19	20	12	20	12	11	17	17	17	17	18
40	9	DISTW	38	1	0	0	1	6	7	6	6	10	9	7	8	7	6	7	6	10	10	9	10	10	14	14	20	19	17	21	22	15	17	24	20	2	24	18	25	19	26	29	**38**	30	34	27	23	28	14	28	14	17	20	22	21	22	22
41	9	DISTW1	42	1	0	0	1	7	8	7	7	11	9	8	8	8	7	8	7	11	10	10	10	11	16	16	24	21	17	23	23	16	17	26	20	2	26	18	27	20	27	23	30	**42**	29	31	28	33	19	34	19	17	23	24	23	22	25
42	9	DISTR	51	1	0	0	1	7	8	8	7	11	9	8	8	8	7	8	7	11	10	10	10	11	15	15	21	19	18	23	22	16	16	24	20	2	24	20	25	21	25	30	34	29	**51**	42	22	27	14	27	14	16	23	21	22	21	22
43	9	DISTR1	49	1	0	0	1	8	9	8	7	12	10	9	8	8	7	8	7	12	11	10	11	12	16	16	22	20	18	23	21	16	15	23	19	2	23	19	25	21	24	24	27	31	42	**49**	22	25	15	26	15	16	22	21	22	21	22
44	10	Butterfly	39	1	0	0	1	7	8	8	7	10	9	8	8	7	7	7	7	10	10	9	10	10	15	15	24	19	15	21	21	14	16	24	17	2	23	19	25	19	24	19	23	28	22	22	**39**	36	21	37	21	19	23	26	25	24	27
45	10	GAL5R	50	1	0	0	1	8	9	8	8	11	10	8	9	8	8	9	8	13	10	11	10	12	17	17	28	23	20	29	26	17	20	31	24	2	30	23	32	26	33	20	28	33	27	25	36	**50**	22	50	21	23	27	32	29	28	32
46	10	GAL5W	24	1	0	0	1	3	3	3	2	7	6	5	5	5	4	6	4	6	5	6	6	4	11	11	16	12	9	14	13	8	8	16	10	2	16	10	18	12	16	12	14	19	14	15	21	22	**24**	23	23	11	17	20	18	18	21
47	10	GAL9R	61	1	0	0	1	8	9	8	8	11	10	8	9	8	8	9	8	13	10	11	10	12	17	17	28	23	20	29	26	17	20	31	25	2	30	23	32	27	35	20	28	34	27	26	37	50	23	**61**	22	24	28	33	30	29	33
48	10	GAL9W	24	1	0	0	1	3	3	3	2	7	6	5	5	5	4	6	4	6	5	6	6	4	11	11	16	12	9	14	13	8	8	16	10	2	16	10	18	12	16	12	14	19	14	15	21	21	23	22	**24**	11	17	20	17	18	20
49	11	SCAN	24	1	0	0	1	8	7	6	6	9	8	7	7	6	6	7	6	10	9	8	8	11	11	11	14	13	15	16	17	15	16	17	16	2	18	16	20	18	19	11	17	17	16	16	19	23	11	24	11	**24**	18	20	19	19	21
50	11	March Y	28	1	0	0	1	6	6	7	5	8	8	7	7	6	6	6	6	9	8	9	9	9	13	13	19	18	15	22	20	13	13	22	18	2	23	18	24	20	24	17	20	23	23	22	23	27	17	28	17	18	**28**	25	26	24	26
51	11	March C-M	35	1	0	0	1	6	5	6	4	7	8	6	7	5	5	6	5	8	8	7	9	9	13	13	23	16	15	22	20	13	14	24	16	2	23	19	26	20	24	17	22	24	21	21	26	32	20	33	20	20	25	**35**	26	28	30
52	11	PMOVI	33	1	0	0	1	8	7	7	6	9	8	7	7	6	6	7	6	11	9	9	9	10	15	15	20	20	17	23	22	14	16	24	19	2	25	20	25	21	25	17	21	23	22	22	25	29	18	30	17	19	26	26	**33**	28	28
53	11	March.1/O	30	1	0	0	1	7	6	6	5	8	8	6	7	5	5	6	5	9	9	7	9	9	14	14	19	18	16	21	21	13	15	23	17	2	24	19	24	20	25	17	22	22	21	21	24	28	18	29	18	19	24	28	28	**30**	27
54	11	March LA	34	1	0	0	1	7	6	6	5	8	8	6	7	5	5	6	5	10	9	8	9	10	14	14	23	18	16	24	21	14	15	24	18	2	24	20	27	21	24	18	22	25	22	22	27	32	21	33	20	21	26	30	28	27	**34**

Table 5. Intersections of stresses

#	ST	FC	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
1	+T	106	**106**	5	26	63	62	21	22	38	40	70	106	77	102	90	54	91	50	51	47	53	47
2	-T	5	5	**5**	5	3	5	3	5	3	4	4	5	5	5	5	5	5	5	5	5	5	5
3	fT	36	26	5	**36**	22	24	27	27	15	18	19	34	33	34	30	30	25	25	25	22	27	24
4	xA	63	63	3	22	**63**	50	20	18	36	37	37	63	43	61	53	47	51	41	46	41	45	40
5	yA	62	62	5	24	50	**62**	19	21	35	37	41	62	45	61	58	45	56	47	48	47	49	47
6	pA	27	21	3	27	20	19	**27**	18	13	15	14	26	24	25	24	24	19	20	20	16	22	17
7	qA	27	22	5	27	18	21	18	**27**	14	16	16	26	27	27	24	24	22	23	19	20	23	21
8	iA	38	38	3	15	36	35	13	14	**38**	32	29	38	30	37	35	30	38	30	34	33	31	33
9	jA	40	40	4	18	37	37	15	16	32	**40**	31	40	34	40	38	32	40	31	35	33	33	34
10	-A	70	70	4	19	37	41	14	16	29	31	**70**	70	68	68	69	36	70	36	39	36	37	39
11	50L	114	106	5	34	63	62	26	26	38	40	70	**114**	82	108	95	59	93	52	54	49	57	49
12	100L	84	77	5	33	43	45	24	27	30	34	68	82	**84**	81	79	45	76	42	43	39	45	43
13	4.6V	110	102	5	34	61	61	25	27	37	40	68	108	81	**110**	89	59	90	52	51	48	55	49
14	5.4V	95	90	5	30	53	58	24	24	35	38	69	95	79	89	**95**	49	87	49	50	47	56	47
15	sD	60	54	5	30	47	45	24	24	30	32	36	59	45	59	49	**60**	44	46	41	38	49	41
16	bD	93	91	5	25	51	56	19	22	38	40	70	93	76	90	87	44	**93**	46	48	48	49	47
17	rD	52	50	5	25	41	47	20	23	30	31	36	52	42	52	49	46	46	**52**	37	37	48	37
18	cD	54	51	5	25	46	48	20	19	34	35	39	54	43	51	50	41	48	37	**54**	44	42	44
19	bbD	49	47	5	22	41	47	16	20	33	33	36	49	39	48	47	38	48	37	44	**49**	41	44
20	rrD	57	53	5	27	45	49	22	23	31	33	37	57	45	55	56	49	49	48	42	41	**57**	40
21	ccD	50	47	5	24	40	47	17	21	33	34	39	49	43	49	47	41	47	37	44	44	40	**50**

FC for all tests using SCs of which the corresponding ST is one of the stresses. E.g., row #4, ST=xA (fast X addressing); FC=63, means that in total 63 faulty DUTs have been detected by all tests using ST=xA; i.e., each SC used xA for the address stress. Note that some tests (for instance the disturb tests) have only been performed with a small number of SCs (see Table 1 and 2). Therefore, some stresses appear to be much more effective than others in terms of FC. Most notably, the high FC of bD (93) is due to the fact that the disturb tests have only been executed with bD; see Table 2. Since these BTs have a high FC, the FC of bD is higher than any of the other DBs.

Inspecting Table 5, the following can be said: -T is covered by +T, xA (FC=63) and yA (FC=62) have almost the same FC (however their intersection is only 50), 50L has a much higher FC than 100L (while 50L almost covers 100L), the FC of 4.6V is much higher than that of 5.4V.

Table 6 shows the unions and intersections of various stresses for the BTs. Each BT has been performed once for each SC. For example, March C- (#24) has been performed SC=168 times. The column "Total" contains two subcolumns. The subcolumn "Uni" shows the union of the fault coverages of the SC tests; the subcolumn "Int" shows the intersection of the SC tests. For March C- Uni=31, while Int=1; which means that of the total FC of 31 (by applying the BT 168 times; once for each SC), only a single faulty DUT is jointly detected by each of the 168 tests. This shows the importance of the SC!

In addition to the column "Total", Table 6 contains one column for each stress. E.g., the column "50L" also has subcolumns "Uni" and "Int" whereby the FC of only tests are taken into consideration with a load stress of 50%. A "-" in the table entry means that the BT has not been applied with the corresponding stress.

From Table 6 one can see, for instance, that test #27 (March LA) detects a total of 32 DUTs, of which only 1 DUT is found by all 168 SCs. At 50% load (50L), 30 of the 32 DUTs are detected. The last seven columns of Table 6, the ones with the DB unions, show that the most efficient DB for March LA is rrD (FC=23). Note that the values in the "Total Uni" columns are the highest reachable values; values in other "Uni" columns will be the same or lower because they represent the results of the corresponding BT using fewer SCs.

From Table 6, it can be deduced, that using -T is less efficient than using either +T or fT.

3.3. Effect of scrambling

Some BTs have been performed both with (SE) as well as without scrambling (SNE). Most noticeably, the BTs of Group 8 have been performed with SE, while the same BTs have been performed (as part of Group 6) with SNE. Table 7 gives a detailed overview of the DUTs detected by each of those BTs. Each BT is listed three times: once with

Table 6. Unions & intersections of BTs & SCs

#	BT	SCs	Total Uni	Total Int	50L Uni	50L Int	100L Uni	100L Int	4.6V Uni	4.6V Int	5.4V Uni	5.4V Int	-T Uni	-T Int	+T Uni	+T Int	fT Uni	fT Int	xA Uni	xA Int	yA Uni	yA Int	pA Uni	pA Int	qA Uni	qA Int	sD Uni	sD Int	bD Uni	bD Int	rD Uni	rD Int	cD Uni	cD Int	bbD Uni	bbD Int	rrD Uni	rrD Int	ccD Uni	ccD Int
1	BuWR0	168	1	0	1	0	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
2	BdWR0	168	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3	BuWR1	168	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
4	BdWR1	168	1	0	1	0	1	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
5	BuW-R0	168	10	0	8	0	9	0	8	0	10	0	4	0	7	0	5	0	5	0	8	0	0	0	5	0	2	2	2	4	4	2	5							
6	BdW-R0	168	12	0	11	0	10	0	11	0	7	0	2	0	7	0	7	0	5	0	6	0	0	0	7	0	1	3	4	5	3	2	4							
7	BuW-R1	168	9	0	8	0	7	0	9	0	7	0	2	0	6	0	5	0	3	0	5	0	1	0	5	0	2	5	4	3	3	1	3							
8	BdW-R1	168	11	0	10	0	9	0	9	0	9	0	1	0	7	0	5	0	4	0	4	0	1	0	5	0	4	5	3	5	2	2	3							
9	BuWRW01	168	12	1	9	1	11	1	11	1	9	1	4	1	8	1	9	1	5	1	9	1	4	1	7	1	4	3	4	6	6	6	7							
10	BdWRW01	168	13	1	9	1	12	1	11	1	11	1	3	1	8	1	8	1	4	1	7	1	3	1	7	1	7	5	6	7	5	6	7							
11	BuWRW10	168	10	1	7	1	9	1	9	1	10	1	3	1	7	1	5	1	4	1	8	1	2	1	5	1	4	5	7	3	3	3	6							
12	BdWRW10	168	11	1	10	1	10	1	11	1	8	1	2	1	4	1	8	1	4	1	3	1	3	1	8	1	4	8	5	4	4	3	4							
13	BuWRW0	168	8	0	6	0	7	0	6	0	8	0	2	0	5	0	6	0	3	0	5	0	2	0	5	0	0	3	2	4	4	3	5							
14	BdWRW0	168	10	0	10	0	9	0	10	0	7	0	2	0	4	0	7	0	3	0	3	0	1	0	6	0	3	2	4	5	3	5	3							
15	BuWRW1	168	9	0	6	0	8	0	8	0	7	0	3	0	4	0	6	0	2	0	5	0	2	0	4	0	2	6	4	5	3	1	4							
16	BdWRW1	168	10	0	8	0	9	0	9	0	9	0	2	0	6	0	5	0	3	0	4	0	1	0	5	0	4	6	4	5	3	3	3							
17	BuWD0	168	15	1	13	1	15	1	15	1	11	1	5	1	8	1	11	1	7	1	10	1	5	1	10	1	6	6	7	6	8	5	8							
18	BdWD0	168	13	1	11	1	12	1	13	1	13	1	3	1	9	1	7	1	6	1	8	1	3	1	7	1	8	5	6	7	5	7	6							
19	BuWD1	168	12	1	10	1	10	1	12	1	8	1	3	1	6	1	9	1	6	1	6	1	4	1	7	1	4	5	6	5	4	4	6							
20	BdWD1	168	14	1	12	1	12	1	13	1	11	1	2	1	8	1	8	1	5	1	8	1	3	1	8	1	6	6	9	4	6	5	4							
21	SCAN	168	14	0	12	0	13	0	14	0	12	0	3	0	11	0	5	0	9	0	10	0	0	0	5	0	2	7	7	10	10	4	7							
22	MATS+1	168	18	1	16	1	16	1	18	1	17	1	5	1	16	1	12	1	10	1	14	1	6	1	8	1	9	8	10	11	13	10	12							
23	MATS+2	168	18	1	18	1	15	1	18	1	17	1	5	1	15	1	10	1	12	1	14	1	5	1	8	1	7	10	12	11	14	10	12							
24	March C-	168	31	1	28	1	27	1	31	1	27	1	5	1	26	2	14	1	19	1	24	1	7	1	11	2	18	17	20	17	21	20	20							
25	PMOVI	168	26	1	25	1	21	1	23	1	22	1	3	1	20	1	15	1	13	1	18	1	6	1	12	2	16	14	17	13	17	17	16							
26	March Y	168	22	1	20	1	21	1	20	1	18	1	5	1	18	1	13	1	14	1	16	1	6	1	10	1	9	9	12	13	15	12	12							
27	March LA	168	32	1	30	1	26	1	29	1	24	1	5	1	26	1	20	1	19	1	24	1	10	1	14	2	20	18	19	18	18	23	19							
28	March.1/O	112	30	3	26	3	23	3	29	3	21	3	0	0	28	3	12	3	20	3	23	4	8	3	10	3	21	13	17	17	17	17	19							
29	March Y-R	112	17	2	16	2	15	2	15	2	16	2	0	0	14	2	12	2	10	3	13	2	10	2	7	2	9	8	8	12	11	8	13							
30	March Y-RR	112	20	2	17	2	19	2	20	2	16	2	0	0	17	2	12	2	12	3	15	2	8	2	10	2	10	10	10	14	12	13	14							
31	March C-R	112	35	2	33	3	29	2	34	3	26	2	0	0	29	3	18	2	23	3	26	4	11	2	14	4	21	17	20	19	25	22	25							
32	PMOVI-R	112	26	2	24	2	23	3	25	3	19	2	0	0	22	3	17	2	17	3	20	3	13	2	12	3	17	12	15	15	15	16	14							
33	WAW	112	2	0	2	0	1	0	2	0	2	0	0	0	1	0	1	0	0	0	1	0	0	0	1	0	1	1	2	1	1	2	1							
34	UAREW	112	32	2	29	2	25	2	29	3	28	2	0	0	30	3	15	2	20	3	27	4	12	2	11	4	22	17	21	19	20	21	20							
35	SCAN	224	28	0	20	0	26	0	27	0	22	0	0	0	21	0	14	0	18	0	14	0	6	0	13	0	10	19	17	14	18	16	15							
36	March C-	224	40	2	34	2	38	2	37	2	32	2	0	0	32	2	20	2	25	2	29	2	14	2	16	2	29	19	30	22	23	27	27							
37	PMOVI	224	33	2	32	2	28	2	28	2	29	2	0	0	24	2	24	2	18	2	22	3	20	2	17	2	26	15	24	17	17	28	18							
38	March LA	224	43	2	37	2	31	2	39	2	33	2	0	0	30	2	26	2	18	2	28	3	20	2	18	2	33	18	29	21	21	30	23							
39	DIST	8	32	3	31	3	26	4	20	4	29	6	0	0	32	3	-	-	-	-	-	-	-	-	-	-	-	32	-	-	-	-	-							
40	DISTW	8	38	11	34	13	34	11	31	11	35	12	0	0	38	11	-	-	-	-	-	-	-	-	-	-	-	38	-	-	-	-	-							
41	DISTW1	8	42	13	37	15	38	14	33	13	39	16	0	0	42	13	-	-	-	-	-	-	-	-	-	-	-	42	-	-	-	-	-							
42	DISTR	8	51	17	49	19	46	18	43	19	49	21	0	0	51	17	-	-	-	-	-	-	-	-	-	-	-	51	-	-	-	-	-							
43	DISTR1	8	49	18	48	19	43	18	45	19	44	21	0	0	49	18	-	-	-	-	-	-	-	-	-	-	-	49	-	-	-	-	-							
44	Butterfly	56	39	0	39	0	-	-	39	0	30	0	0	0	39	0	-	-	30	0	33	1	-	-	-	-	26	21	20	30	29	23	29							
45	GAL5R	56	50	0	50	0	-	-	49	0	40	1	0	0	50	0	-	-	41	0	50	2	-	-	-	-	31	25	30	38	31	38	37							
46	GAL5W	56	24	3	24	3	-	-	21	3	23	4	0	0	24	3	-	-	23	4	22	3	-	-	-	-	22	6	18	17	16	20	19							
47	GAL9R	56	61	8	61	8	-	-	59	9	53	9	0	0	61	8	-	-	50	9	56	10	-	-	-	-	33	45	39	37	40	43	40							
48	GAL9W	56	24	12	24	12	-	-	21	12	23	13	0	0	24	12	-	-	24	13	22	12	-	-	-	-	22	17	18	19	18	20	19							
49	SCAN	80	24	0	24	0	-	-	22	0	19	0	0	0	24	0	-	-	20	0	19	0	-	-	-	-	-	24	-	-	-	-	-							
50	March Y	80	28	3	28	3	-	-	25	4	22	3	0	0	28	3	-	-	20	3	24	4	-	-	-	-	-	28	-	-	-	-	-							
51	March C-	80	35	4	35	4	-	-	30	4	27	4	0	0	35	4	-	-	31	6	26	4	-	-	-	-	-	35	-	-	-	-	-							
52	PMOVI	80	33	4	33	4	-	-	31	5	27	5	0	0	33	4	-	-	26	5	32	5	-	-	-	-	-	33	-	-	-	-	-							
53	March.1/0	80	30	4	30	4	-	-	26	5	25	4	0	0	30	4	-	-	24	5	28	4	-	-	-	-	-	30	-	-	-	-	-							
54	March LA	80	34	4	34	4	-	-	31	4	29	4	0	0	34	4	-	-	25	6	32	4	-	-	-	-	-	34	-	-	-	-	-							

SNE (e.g., "SCAN"), once with SE using scrambling table "a" ("SCANa") and once with SE using scrambling table "b" ("SCANb"). Note that two scrambling tables have been used, because SIMMs with DUTs from two different manufacturers were used. All DUTs on a single SIMM are equal; therefore they require the same scrambling table. However, different SIMMs require different scrambling tables. The column of DUT 16 contains a single "X" symbol in the row of March C-a, indicating that it is the only test detecting DUT 16. The results suggest that both tables are necessary; i.e., some DUTs are laid out according to table "a" and others are laid out according to table "b".

All four BTs have the highest FC when scrambling table "b" is used. For SCAN and March C-, the test with SNE has a higher FC than using scrambling table "a". However, Table 7 shows that there is a big difference in the DUTs detected without scrambling and with table "a". Therefore, it is not possible to simply conclude that using scrambling table "a" is worse than using no scrambling table at all by looking at the FC alone.

For all four BTs, there is at least one DUT that is only detected with a single scrambling table (or none). Therefore, all three possible scrambling methods should be tested for full FC. These results show however, that if a choice has to be made, SE is to be preferred over SNE, as could be expected.

The tests of Group 8, as well as the tests in the Groups 9, 10 and 11, have been performed with two different scrambling tables. Table 8 shows the FC of these tests for the two scrambling tables. The column "Uni" means the union (the total number of DUTs detected by the BT), the column "STa" the number of DUTs detected by the BT using scrambling table "a", the column "STb" the number of DUTs detected by the BT using scrambling table "b", and the column "Int" the intersection (the number of DUTs detected by both scrambling tables). For instance, BT 42 of Group 8, DISTR, detected 39 DUTs when executed with scrambling table "a". With table "b", 40 DUTs were detected. In total, 51 DUTs are detected by DISTR, of which 28 are detected with both scrambling tables.

The results, as given in Table 8, indicate that the choice of scrambling table matters. This is logical, since it is more likely for physically neighboring cells to affect each other than it is for non-neighboring cells. The low values of

Table 7. Overview of tests with scrambling

```
                DUT#          1111111113344444444455666666666666677777777777777
                          11224446601235555648112677779050123444456679111344478888999
 # Grp BT         FC 61619379082786145836913201459353483702465476707961269235715 9
-------------------------------------------------------------------------------------
21  6  SCAN       14          XXX  X     X   XXX  X XX           X X X
35  8  SCANa      18          XX   X X X X X  X   X XX  XX X    X X X    X
35  8  SCANb      21          XX  XX XX XX XXXXXXXX  X       X    X X       X
24  6  March C-   31       XXXXXXXXX     X XXXXXXXX  X   X X X  X X XXX  X   X XX
36  8  March C-a 33 X X   XXXXX  XX X   XXXXXXXXXX XX  XX   X  X X XX      XX XX
36  8  March C-b 33 X   X X XXX  XX  X XX XXXXXXXX  X X     X XXXX XXX     XX XX
25  6  PMOVI      26          XXX XXXX   X X  XXXXX XX   X   X  X X XX    X  X XX
37  8  PMOVIa     24 X        XX  XX XX  X X XXX  XXXX       X    X XX   X  XX  X
37  8  PMOVIb     27 X  X X   XX  XX  X XX XXXXX  X  X       X XXXX X X     XXX
27  6  March LA   32          XXXXXXXXX  X XXXXXXXX XX       X XX X XXX  X   XXXX
38  8  March LAa  29  X    X  XX  XX X   X XXXXXXXXXX       X    X XX  X X XX XX
38  8  March LAb  37 X    XX  XX  XX  X XX XXXXXXXX  XX   X XX XXXXXXXXX    XXXXX
```

Table 8. FC of tests per scrambling table

#	Grp	BT	Uni	STa	STb	Int
35	8	SCAN	28	18	21	11
36	8	March C-	40	33	33	26
37	8	PMOVI	33	24	27	18
38	8	March LA	43	29	37	23
39	9	DIST	32	23	19	10
40	9	DISTW	38	32	22	16
41	9	DISTW1	42	35	28	21
42	9	DISTR	51	39	40	28
43	9	DISTR1	49	40	36	27
44	10	Butterfly	39	35	28	24
45	10	GAL5R	50	45	41	36
46	10	GAL5W	24	21	22	19
47	10	GAL9R	61	53	50	42
48	10	GAL9W	24	21	22	19
49	11	SCAN	24	18	15	9
50	11	March Y	28	21	21	14
51	11	March C-	35	31	24	20
52	11	PMOVI	33	29	24	20
53	11	March.1/O	30	26	25	21
54	11	March LA	34	31	27	24

the intersections show that both scrambling tables definitely find different DUTs. If it would have been precisely known, on a per SIMM basis which scrambling table was necessary, only one table would have been used per DUT, effectively halving the test time.

3.4. Effect of burst mode

Table 9 shows the intersection of each pair of *addressing orders (AOs)* xA, yA, pA and qA. Also included are the intersections of AOs with either the union of xA and yA (denoted as "xAyA") and the union of pA and qA (denoted as "pAqA"). It should be noted that this table is compiled only from tests that have been performed with the four AOs: Groups 1 through 8. Therefore, results from, for instance, DISTR have been omitted, resulting in a lower FC than the 116 DUTs detected by the union of all BTs. The FC of the union of Groups 1 to 8 is 64.

What can be seen from Table 9 is that the intersections of xA-pA and yA-qA are not 100%. The intersection of xA and pA is 17, while the FC of xA is 40 and that of pA is 27. Therefore, $27 - 17 = 10$ DUTs are only detected by pA and $40 - 17 = 23$ DUTs are only detected by xA. The intersection of yA and qA is 21, while the FC of yA is 43 and the FC of qA is 27, leaving $43 - 21$ DUTs only detected by yA and $27 - 21 = 6$ DUTs only detected by qA.

Note that the FC of the unions xAyA and pAqA can be calculated from the table as follows; here "(xA,yA)" denotes the intersection of xA and yA:

$$xAyA = (xA,xA) + (yA,yA) - (xA,yA) = 40 + 43 - 31 = 52$$
$$pAqA = (pA,pA) + (qA,qA) - (pA,qA) = 27 + 27 - 18 = 36$$

Likewise, the total FC of 64 can be calculated by:

$$FC = (xAyA,xAyA) + (pAqA,pAqA) - (xAyA,pAqA)$$
$$= 52 + 36 - 24 = 64$$

The fact that the intersections are not 100% shows that burst mode tests detect additional faults over word mode tests. Note that burst mode tests detect $64 - 52 = 12$ DUTs that are not detected by word mode tests.

3.5. Effect of data background

Table 10 shows the intersections of each pair of DBs. Note that only BTs executed with all 7 DBs have been used to calculate the table: Groups 1 to 8 and 10. The FC of

Table 9. Addressing order intersections

	xA	yA	pA	qA	xAyA	pAqA
xA	**40**	31	17	16	40	19
yA	31	**43**	18	21	43	23
pA	17	18	**27**	18	19	27
qA	16	21	18	**27**	21	27
xAyA	40	43	19	21	**52**	24
pAqA	19	23	27	27	24	**36**

Table 10. Data background intersections

	sD	bD	cD	rD	bbD	ccD	rrD
sD	**60**	42	41	46	38	41	49
bD	42	**56**	46	44	44	43	45
cD	41	46	**54**	37	44	44	42
rD	46	44	37	**52**	37	37	48
bbD	38	44	44	37	**49**	44	41
ccD	41	43	44	37	44	**50**	40
rrD	49	45	42	48	41	40	**57**

the union of these groups is 116 DUTs. Table 10 shows, that sD is the best overall DB (FC=60) and that bbD is the worst overall DB (FC=49). Furthermore, it shows that the minimum intersection is 37. This means, that 37 of the 116 DUTs are detected regardless of the DB used. Also, because the maximum intersection is (only) 60, there are at least two DBs necessary to have 100% FC.

4. Test optimization

There are many possible ways to choose a new Testset from the total Testset of 5952 tests, while the new set retains 100% FC. The problem however, is to create the shortest Testset that still has 100% FC. This shortest Testset is the *Initial Production Test Set (IPTS)*.

There are $5952!/(5852! \cdot 100!)$ possible Testsets of 100 tests to select from a set of 5952 tests. Therefore several strategies can be used to select not the *exact* shortest, but an approximation which will still have 100% FC. The strategy to construct the IPTS is simple: 1) Determine the set of tests that detect single fails, and 2) establish the minimum Testset. First, the tests that detect single fails are added to the Testset, then tests with the highest FC and the shortest test length are continually added until 100% FC is achieved.

Some faulty DUTs are only detected by a single test; these DUTs are called *single fails*. Table 11 lists the set of 14 tests detecting 16 single fails, together with their SCs; these tests are always required for 100% FC. Note that PMOVI occurs 4 times, and March C- 3 times; -T is absent, while 50L and -V are more prominent.

Table 12 shows the minimum Testset, consisting of 29

Table 11. Tests that detect single fails

Test	Stress condition	Time
Marching 1/0	50L xA sD +T -V	$14n$
March C-	50L xA cD +T -V	$10n$
March LA	50L pA cD fT +V	$22n$
DISTR1	50L -A bD +T -V	$440n$
Butterfly	50L xA sD +T -V	$14n$
GAL9R	50L yA cD +T -V	$38n$
March C-	50L iA bD +T -V	$10n$
PMOVI	50L yA bD +T -V	$13n$
March LA	50L pA sD fT -V	$22n$
GAL9R	50L xA rrD +T -V	$38n$
PMOVI	50L iA bD +T -V	$13n$
PMOVI	50L jA bD +T -V	$13n$
March C-	100L qA ccD fT -V	$10n$
PMOVI	100L pA sD fT -V	$13n$

tests, and a total test time of $1829n$. The suffix 'a', 'b' or 'n' behind the BT names indicates whether scrambling table 'a', 'b' or no scrambling table has been used with the corresponding test. The "`i=8`" in line #16 indicates that the corresponding test is from Group 11 (2^i addressing), and that the fault has been detected when an address increment/decrement of $2^i = 2^8 = 256$ has been used. The column "C_FC" shows the cumulative FC, which becomes 116 DUTs (100% FC); the column "C_LNG" shows the cumulative required test time. Note the high frequency of occurrence of the GAL9R, PMOVI, March C- and March LA.

5. Conclusions

This paper summarizes the results of applying 54 base tests, each with up to 168 different stress combinations; resulting in a total of 5952 tests applied to 50 SIMMs with a total of 800 chips. From this the following can be concluded:

1. Fault coverage of a test is not always the same. If exactly the same test is run twice, the results may vary. To show this the BT MATS+ has been performed twice (as MATS+1 and MATS+2, respectively). From Table 6, #22 and #23, we can see that although the Total FC=18 for both BTs, a difference in FC by as much as 2 can be observed; e.g., in the columns fT-Uni, xA-Uni, sD-Uni, bD-Uni, and rD-Uni. Such a difference may be explained from temperature variations in the chip, and signal noise. Therefore, conclusions based on small variations (e.g., 2 DUTs) in fault coverage are not justifiable and should be avoided.

2. Word mode tests detect fundamentally different faults than burst mode tests. Therefore, both types of tests are required to increase fault coverage.

Table 12. Minimum Testset

#	C_FC	C_LNG	BT	Stress condition	Length
1	38	440n	DISTRb	50L -A bD +T 5.4V	440n
2	56	478n	GAL9Ra	50L yA bD +T 4.6V	38n
3	65	500n	MarchLAb	50L pA sD fT 4.6V	22n
4	73	940n	DISTR1a	50L -A bD +T 4.6V	440n
5	79	978n	GAL9Rb	50L yA rD +T 4.6V	38n
6	83	992n	March.1/0n	50L xA sD +T 4.6V	14n
7	86	1005n	PMOVIb	100L qA sD fT 4.6V	13n
8	89	1019n	Butterflya	50L xA sD +T 4.6V	14n
9	92	1041n	GAL5Ra	50L yA ccD +T 5.4V	22n
10	94	1045n	SCANa	50L xA bD +T 4.6V	4n
11	96	1067n	MarchLAa	50L pA cD fT 5.4V	22n
12	98	1105n	GAL9Ra	50L yA rD +T 4.6V	38n
13	100	1143n	GAL9Ra	50L yA cD +T 4.6V	38n
14	101	1147n	SCANa	100L xA bD +T 5.4V	4n
15	102	1157n	MarchC-a	50L xA cD +T 4.6V	10n
16	103	1167n	MarchC-ia	50L iA bD +T 4.6V i=8	10n
17	104	1177n	MarchC-ib	50L iA bD +T 5.4V i=5	10n
18	105	1187n	MarchC-a	100L qA ccD fT 4.6V	10n
19	106	1200n	PMOVIia	50L jA bD +T 4.6V i=9	13n
20	107	1213n	PMOVIib	50L iA bD +T 4.6V i=6	13n
21	108	1226n	PMOVIib	50L jA bD +T 4.6V i=1	13n
22	109	1239n	PMOVIb	100L pA sD fT 4.6V	13n
23	110	1254n	MarchC-Rn	50L qA bD fT 4.6V	15n
24	111	1269n	MarchC-Rn	100L qA ccD fT 4.6V	15n
25	112	1291n	GAL5Wa	50L xA sD +T 5.4V	22n
26	113	1313n	MarchLAb	100L pA sD fT 4.6V	22n
27	114	1351n	GAL9Ra	50L yA bD +T 5.4V	38n
28	115	1389n	GAL9Rb	50L xA rrD +T 4.6V	38n
29	116	1829n	DISTR1b	50L -A bD +T 4.6V	440n

Total 29 tests, detecting 116 DUTs, cost 1829n

3. For most tests, Fast-Y addressing is more efficient than Fast-X addressing, because Fast-Y addressing creates more of a refresh problem (see Table 6).

4. More faults are detected with a low voltage (4.6V) than with a high voltage (5.4V). However, 6 faults are detected only at 5.4V; see Table 5.

5. Disturb tests such as DIST, DISTR or DISTW detect faults, that would otherwise go unnoticed. However, they take way too long (in the order of 10's of minutes) to be useful in a production environment, where the maximum test time is only a few minutes per module.

6. The best BT is GAL9R, because its FC=61, which is the highest, and it also detects many unique faults (Table 4 shows that its highest intersection is only 50). The BT GAL9W however, detects considerably fewer faults. This may be due to the fact that GAL9R performs more reads than GAL9W; only reads can detect faults.

Recommendations

More variations of GAL9R should be constructed. For instance, GAL9RW can be the following:

GAL9RW ($46n$): $\{\Uparrow (w0); \Uparrow_b (w1, \square(r0, w0, r1_b), w0); \Uparrow (w1); \Uparrow_b (w0, \square(r1, w1, r0_b), w1)\}$

Other variations like GAL9RW (with r0, w0 changed into w0, r0) are also possible.

From the proposed IPTS, a production test set has to be made by replacing the longer tests with subsets with the same FC. Of the total of $1829n$ of Table 12, the 3 DISTR tests require a total of $3 \times 440 = 1320n$. A SIMM is organized as 8M·32 bits; which means that, using word-mode, for one pass through the memory (which is $1 \cdot n$) 8M accesses of 110 nsec. have to be performed. This takes $8M \cdot 110 \cdot 10^{-9}$=0.92 sec. If the IPTS could be simplified to $1829n$-$1320n$=$509n$, the test time would be 509·0.92=468 sec., which is still quite long. However, this testset detects escapes from the regular production testset. In order to further reduce the total test time, tests should be performed at high temperature; this stress has shown to be effective, especially for DRAMs [2].

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