Statistical Reliability Analysis of NBTI Impact on FinFET SRAMs and Mitigation Technique Using Independent-Gate Devices

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***Abstract*—As planar MOSFETs is approaching its physical scaling limits, FinFET becomes one of the most promising alternative structure to keep on the industry scaling-down trend for future technology generations of 22 nm and beyond. In this paper, we propose a statistical model of Negative Bias Temperature Instability (NBTI) tailored for FinFET SRAM Arrays. The model build upon an extension of the reaction-diffusion theory such that it can cover the natural variations encountered in nanoscale MOSFET circuits. Dynamic NBTI stress on SRAM cells is modeled by using stochastic input signals. A mitigation technology for minimizing the NBTI aging is also demonstrated by taking advantage of the independent-gate FinFET device structure using threshold voltage adjustment. We evaluated the impact of our proposal on the RAM stability by means of SPICE simulations with the BSIM-IMG Model for 22nm FinFET devices. Our simulations conducted at an accelerated temperature $125^{\circ}C$ for 10^8 seconds ($\sim$3 years) indicate that a V_{th} compensation of 0.2V can almost preserve the WRITE and HOLD stability of the fresh device even after 3 years, while for the READ stability the compensation mechanism is less effective. However, the READ Static Noise Margin (SNM) experiences an insignificant decrease over the 3 years time span in the presence of a V_{th} compensation, while without compensation it decreases by a x4 factor. Thus we can conclude that the proposed technique can improve the stability of SRAM array during its operational life, hence improve the performance and reliability of the system.**

I. Introduction

As technology scaling continues, the Integrated Circuits (IC) feature size has been driven into the physical limitation edge of conventional MOSFET device. In order to keep technology scaling down further, two major issues have to be properly addressed: (i) the excessive leakage power and (ii) the device/circuit reliability. Given that those have to be dealt with in the context of uncontrollable statistical process variations, the continuation of technology scaling seems to be more difficult than ever.

In order to keep on the industry scaling-down trend, novel devices and structures were proposed as potential candidates to replace the conventional planar MOSFET device. Among the proposed novel devices, FinFET seems to be one of the most promising alternative structure for future technology generations of 22 nm and beyond, owing to its fabrication process simplicity and good electrical characteristics [1]. Contributed to its device structure consisting of single/multiple vertical fin(s), the FinFET has better electrostatics on Short-Channel Effect (SCE), thus less static leakage current and power consumption. However, FinFET also experiences multiple temporal degradations, e.g., Negative Bias Temperature Instability (NBTI), Hot Carrier Injection (HCI). In other words, on top of the spatial uncertainty caused by process variations, various temporal degradations hold back the feature size of technology from further scaling.

In view of the previous argument, in this paper, we address the following aspects: (i) the modeling of the spatial and temporal reliability behavior of FinFET SRAM arrays under NBTI stress and (ii) the investigation of a mitigation method which can take advantage of the FinFET's special device structure.

NBTI is prominent in PMOS devices along the entire channel when negative gate-to-source voltage is applied, and it causes a threshold voltage (V_{th}) shift, which results in poor drive current and shorter device and circuit lifetime. Recent experimental investigations indicate that Multi-Gate FET devices with standard orientation exhibit worse NBTI than planar devices due to the higher availability of Si-H bonds at the (110) oriented fin sidewalls [2]. Depending on the electrical connection, i.e., shorted or isolated, between its gates, FinFET can operate at either on Shorted-Gate (SG) mode or Independent-Gate (IG) mode. In the shorted-gate operating mode the gates of the FinFET device are biased together to switch the channel conduction. In the independent-gate operating mode, one gate can be used to adjust the threshold voltage and the other gates are used to control the channel conduction. This offers a dynamic control-ability to mitigate or eliminate the damage caused by NBTI stress.

In this line of reasoning, we first investigate the influence of stochastic input signal on long-term reliability under NBTI stress. Furthermore, the effect of random process variations on NBTI degradation, as well as the statistical characteristic of temporal degradation induced by NBTI are also discussed and analyzed. After that, we propose an NBTI mitigation

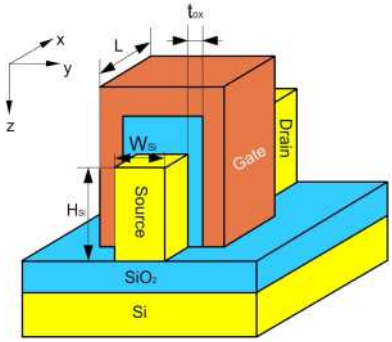


Fig. 1. SOI FinFET Schematic View.

technique based on an I_{DDQ} current sensor, utilizing threshold voltage compensation in an IG-FinFET SRAM. The proposed technique can improve the stability of SRAM array during its operational life, hence improve the system performance and reliability.

The rest of this paper is organized as follows: In Section 2 we introduce the temporal V_{th} degradation induced by NBTI under dynamic stress; In Section 3 we analyze the V_{th} variations caused by process variations and non-uniform degradation of NBTI and their impact on the stability of an SRAM cell; In Section 4 we propose a V_{th} compensation technique using IG-FinFET to improve SRAM's stability and the proposed scheme is evaluated in Section 5 by means of SPICE simulations; In Section 6 we concludes our work.

II. Temporal V_{th} Degradation under NBTI

NBTI has been addressed in many works, and the NBTI caused degradation becomes a major reliability concern for nanoscale CMOS technology. In most literature, V_{th} has been chosen as the indicating parameter of NBTI induced degradation. In this section, we present a simple analysis on the temporal degradation of V_{th} for long-term random stress condition.

NBTI occurs in negatively biased transistors at elevated temperature. Holes from the inversion layer can tunnel into the gate oxide, break the Si-H bond leaving behind an interface trap (N_{it}), which results in a positive shift in V_{th}. Traditionally, the interface trap generation is modeled successfully in the Reaction-Diffusion (R-D) framework [3]. In this model, the interface trap increment under static stress condition can be expressed as

$$\Delta N_{it}(t) = (\frac{k_f N_0}{2k_r})^{\frac{2}{3}}(D_H t)^{\frac{1}{6}}, \quad (1)$$

where molecular hydrogen diffusion is assumed and the time exponent is $n = 1/6$. N_0 is the initial number of Si-H bonds available at the interface and D_H is the diffusion constant of hydrogen specie in the oxide and/or poly gate. k_f and k_r are the reaction rate of Si-H bond dissociation and passivisation. The dissociation reaction rate k_f depends on the hole density in the inversion layer and the probability of tunneling holes into the oxide. This dependence can be written as

$$k_f \propto \sigma_0 p T_p,$$

where σ_0 is the hole capture cross section, $p = C_{ox}(V_{gs} - V_{th}) \propto E_{ox}$ is the hole density in the inversion layer, and $T_p \propto exp(E_{ox}/E_0)$ is the tunneling coefficient. Moreover, the reaction rates also have a Arrhenius-like temperature dependence $\sim exp(E_a/k_B T)$, where Ea is the activation energy and k_B and T are the Boltzmann constant and temperature, respectively. Submitting all the relations into Eq. (1) yields

$$\Delta N_{it}(t) = A_0(V_{gs} - V_{th})^{\frac{2}{3}} exp(\gamma E_{ox}) exp(\frac{E_{aa}}{k_B T}) \cdot t^{\frac{1}{6}}, \quad (2)$$

where A_0 is a field and temperature independent pre-factor, $E_{aa} = E_{a,f} - E_{a,r}$ is the activation energy for the reversible progress of Si-H dissociation and passivisation. The threshold voltage degradation due to interface traps can be computed as

$$\Delta V_{th}(t) = \frac{q \Delta N_i t(t)}{C_{ox}}. \quad (3)$$

Furthermore, the interface traps degrades the carrier mobility by increasing scattering in the channel, which results in an additional V_{th} shift [4]. Taking this effect into account, the threshold voltage degradation can be expressed as [5]

$$\Delta V_{th}(t) = (1 + m)\frac{q \Delta N_i t(t)}{C_{ox}}, \quad (4)$$

where m is a constant representing the equivalent V_{th} shift due to mobility degradation for a given technology.

When the NBTI stress, i.e., the negative bias, is removed, the V_{th} degradation will recover because of the Si-H bond annealing. According to [6], the dynamic ΔV_{th} under AC stress can be expressed as

$$Stress: \quad \Delta V_{th} = (K_v(t - t_0)^{1/2} + \sqrt[2n]{V_{th0}})^{2n} \quad (5)$$

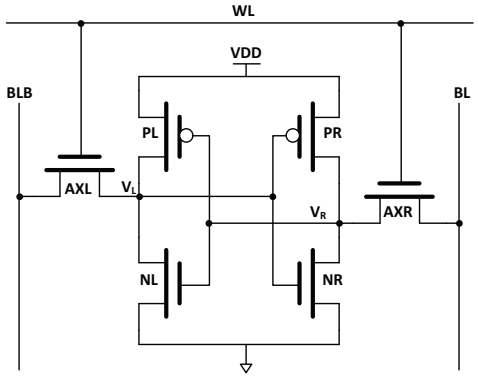
$$Recovery: \quad \Delta V_{th} = V_{th0}(1 - \frac{2\xi_1 t_e + \sqrt{\xi_2 C(t - t_0)}}{2t_{ox} + \sqrt{Ct}}), \quad (6)$$

where ξ_1 and ξ_2 are constants and t_e is the effective diffusion distance. C is the diffusion temperature-dependent coefficient, and K_v is given by

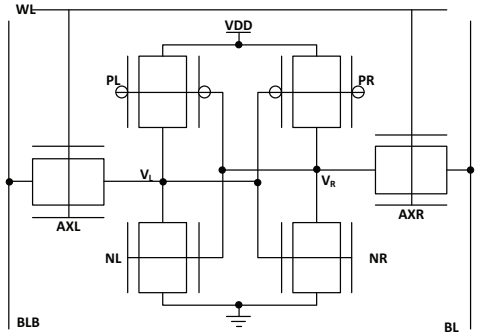
$$K_v = (\frac{q t_{ox}}{\epsilon_{ox}})^3 K^2 C_{ox}(V_{gs} - V_{th})\sqrt{C} exp(\frac{2E_{ox}}{E_0}). \quad (7)$$

III. Statistical Analysis of V_{th} with Process Variation and NBTI Stress

As a major part of modern processors, SRAM drives the technology scaling direction in industry. Hence, understanding the impact of NBTI on SRAM cells is critical to the technology scaling, because the small area size and low power consumption of SRAM cell makes it more sensitive to the temporal degradation than other components. Another reliability concern caused by technology scaling is the Process-Variation (PV), which introduces spatial uncertainty to the performance parameters of devices. In this section, we analyze the statistical impact of process variation and NBTI on threshold voltage in FinFET based SRAM cells.



(a) SRAM based on Conventional Single-Gate Planar CMOS.



(b) SRAM based on Gate Tied Double-Gate(DG)/Triple-Gate(TG) FinFET CMOS.

Fig. 2. Schematic of the 6T SRAM cell, based on different devices.

A. V_{th} Variation by Process Variations

Process variations become particularly important at smaller technology node (<65nm) as feature size is scaling down and variations become significant when compared with the full device size. Process variations are typically divided into two components: inter-die/global and intra-die/local. Inter-die accounts for chip- or wafer-level variations, while intra-die accounts for variations between different devices.

V_{th} under process variations and NBTI can be expressed as

$$V_{th} = V_{th0} + \Delta V_{th,g} + \Delta V_{th,l} + \Delta V_{th,nbti}(t), \quad (8)$$

where V_{th0} is the nominal value of V_{th}, and $V_{th,g}$ and $V_{th,l}$ are V_{th} change of due to global and local variations, respectively.

Since our research on SRAM is addressing only chip-level issues, we only focus on the local variations. Among all local variation sources Random Dopant Fluctuation (RDF), Line-Edge Roughness (LER), and gate critical dimension, are considered to be the major variations affecting the stability of SRAM cells.

According to [7], the V_{th} mismatch caused by intra-die Process Variations can be expressed by

$$\sigma_{V_{th},PV} = \frac{A_{VT}}{\sqrt{WL}}, \quad (9)$$

where A_{VT} is a technology conversion constant proportional to the oxide thickness and the channel doping, and WL denotes the transistor's active area.

Similar to the conventional one, a 6T gate-tied FinFET SRAM cell is depicted in Fig. 2(b). FinFETs have a better electrostatic control on the channel than planar structure devices resulting in reduced short-channel effects. The major variations sources in a FinFET are considered to be the gate-length variation ΔL and the fin thickness variation ΔT_{fin} [8], which influence device V_{th} through short-channel effects. The channel width of FinFET device is estimated by

$$W_{fin} = N \cdot (2H_{si} + W_{si}), \quad (10)$$

where H_{si} and W_{si} are the fin height and thickness, respectively, and N is the number of fins in a single device.

B. V_{th} Variation With PV and NBTI Stress

The PV-induced V_{th} variations define the statistical reliability profile of SRAM cells at time 0, i.e., when devices are fresh. As known, NBTI induces a temporal degradation on V_{th} and for an individual device, the evolution in time of this progress is governed by Eq. (4). However, due to the RDF effect, the Si-H bonds dissociation and re-passivisation processes experience stochastic fluctuations. The numbers of broken bonds are assumed as a Poisson random variable. As a result, the V_{th} degradation caused by N_{it} given in [9] and revisited to adjust mobility degradation inhere can be expressed as

$$\sigma_{\Delta V_{th}(t)} = \sqrt{\frac{qt_{ox}\mu\Delta V_{th}}{(1+m)\epsilon_{ox}A_G}} \propto \frac{t^{1/12}}{A_G}, \quad (11)$$

where A_G is the effective area.

We note that the temporal degradation discussed above doesn't consider the workload difference yet. From previous section discussions we know that the V_{th} degradation induced by NBTI highly depends on the stress condition the device experiences. In the case of the 6T SRAM cell, there are two PMOS in the circuit, which will suffer NBTI degradation during operation. The NBTI stress conditions for these two devices are determined by the data values at the storage nodes V_L and V_R, respectively. The random workload leads to a further fluctuation of V_{th} degradation in different SRAM cells. The standard deviation (STD) of ΔV_{th} of this progress depends on the specific bit pattern stored into the SRAM cells, and it is difficult to capture it by means of an analytical expression. If we denote this STD as $\sigma_{\Delta V_{th}(w)}$, the degradation variation induced by NBTI is

$$\sigma_{NBTI(t)} = \sqrt{\sigma^2_{\Delta V_{th}(t)} + \sigma^2_{\Delta V_{th}(w)}}. \quad (12)$$

Finally, the variation of V_{th} considering both PV and NBTI effects can be given as

$$\sigma_{V_{th}} = \sqrt{\sigma^2_{V_{th},PV} + \sigma^2_{NBTI(t)}}. \quad (13)$$

From this we can see that, NBTI stress will increase the STD of V_{th}, hence affects the performance of circuits dynamically. The variation of ΔV_{th} comes from two parts: one is caused by the non-uniform reaction rate of Si-H bonds dissociation, which is related to the process variation; and the

other one is caused by the workload difference of individual device.

C. NBTI Impact on V_{th} Variation and SRAM Cell Performance

A conventional basic 6T SRAM cell is presented in Fig. 2(a). AXL, PL, and NL are the access, pull-up, and pull-down transistor on the left side of the cell, respectively. Similarly, AXR, PR, and NR are the corresponding ones on the right side. VR and VL are the cell storage nodes. Under NBTI stress, the V_{th} absolute value of the two PMOS transistors PL and PR in the SRAM cell increases with time. Hence, the performance of the SRAM cell will be affected by NBTI accordingly. Note that the V_{th} value is critical to the stability of the SRAM cell, which is conventionally evaluated by the Static Noise Margin (SNM) defined using the input voltage to output Voltage Transfer Characteristic (VTC).

If we assume 50% signal probability for both VL and VR nodes, the $|V_{th}|$ increase of PL and PR will be almost the same, thus SNM of HOLD won't be affected by NBTI. In reality, the signal probabilities S_L, S_R for VL and VR are different (but $S_L + S_R = 1$), which results in an SNM degradation under NBTI. However, simulation results reported in [9] suggest that the impact of NBTI on SRAM cell is not significant during standby. For read stability, as NBTI increases the $|V_{th}|$ of PMOS in the "0" node (say VR in Fig. 2), it increases the output voltage to the load inverter (PL-NL inverter in this case) hence increases the read failure probability. But for write stability, as PMOS V_{th} increases with time, the node storing "1" gets weaker and writing "0" to that node becomes easier. In other words, NBTI increases the write stability but decrease the read stability.

It's also worth to mention that because the values stored in the storage nodes V_L and V_R are complementary, from Eq. (5) and Eq. (6) we further know that the two PMOS will experience asymmetrical degradation unless the value stored in the cell is periodically flipped.

IV. NBTI Mitigation in FinFET SRAM Arrays

As discussed in previous sections, V_{th} degradation caused by NBTI stress is a dynamic variable process, which decreases the efficiency of the design-time optimization on circuits' performance and reliability margins. In order to maintain the expected performance and reliability during ICs' lifetime, online low area and energy overhead compensation/elimination techniques able to circumvent the consequences of NBTI stress are highly desirable for advanced technology nodes. In this section, we propose a V_{th} compensation technique that makes use of IG-FinFETs in SRAM cells to compensate NBTI-induced degradation and thus to increase the SRAM array reliability.

A. IG-FinFET Based V_{th} Compensation Scheme for SRAM Cells

In order to minimize the damage caused by NBTI and increase the read stability of the SRAM cell, in this section we demonstrate an NBTI mitigation technique applicable to independent-gate (IG) FinFET based SRAM implementations. In the IG-FinFET, a separated back gate can be used to control the threshold voltage in the channel, which give us the possibility to compensate the V_{th} degradation in PMOS and to maintain the circuit performance at its expected value.

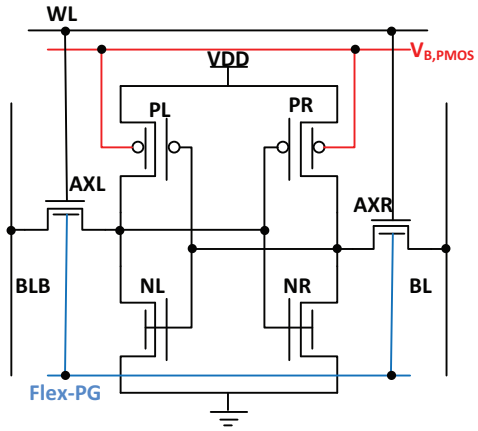


Fig. 3. IG-FinFET 6T SRAM with V_{th} Compensation/Adjustment for PMOS and Pass Gates: signal line "$V_{B,PMOS}$" is used to compensate the V_{th} degradation caused by NBTI in PMOS, and signal line "Flex-PG" is used to adjust the V_{th} of pass gates in the cell to improve the READ stability.

Fig. 3 presents the configuration of a 6T SRAM cell formed by IG-FinFET with V_{th} compensation for PMOS and V_{th} adjustment for the pass gates AXL and AXR (by the signal line "Flex-PG") to improve its stability. Though the Positive Bias Temperature Instability (PBTI) effect is not considered in this paper, we still adapt the V_{th} adjustment scheme from [10] to improve the READ stability.

As V_{th} degrades with time in PMOS, we can put a reverse adjust bias onto $V_{B,PMOS}$ line. Hence, the degradation can be compensated/eliminated, and the cell stability and performance is improved/preserved. As we have already discussed before, the V_{th} and the NBTI-induced degradation is a statistical distribution, so the value of $V_{B,PMOS}$ needs to be carefully chosen in order to get a global optimization for the SRAM array. This aspect is discussed in details in the next section.

B. V_{th} Compensation Using Leakage Monitoring

In [11] the authors have analyzed and proposed to use the standby leakage current I_{DDQ} to monitor and characterize the NBTI induced temporal performance degradation. As shown in their work, a current sensor monitoring I_{DDQ} for SRAM array is a good indicator of NBTI degradation. In this section we further extended this idea in order to introduce an NBTI mitigation technique. The specific schematic of our proposal is depicted in Fig. 4.

In the proposed scheme, a leakage current sensor formed by transistors $M2 \sim M4$ is attached to an SRAM array. The leakage current of the entire array is collected by M2 and then mirrored into M3, generating an output signal "V_{out}", which is proportional to the leakage value. The output signal is subsequently compared with a reference voltage to evaluate the degradation induced by NBTI. The comparison result is

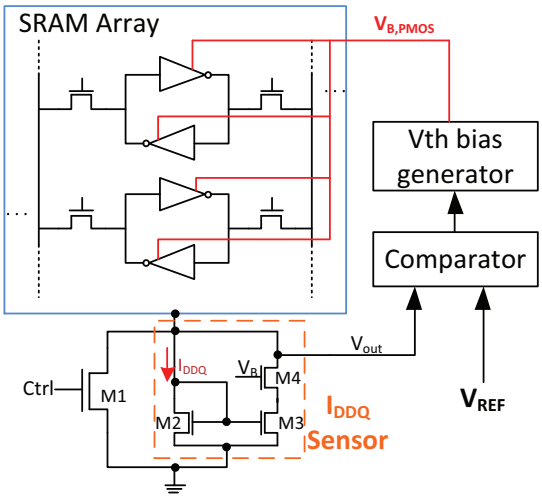


Fig. 4. NBTI Mitigation Using I_{DDQ} Monitor.

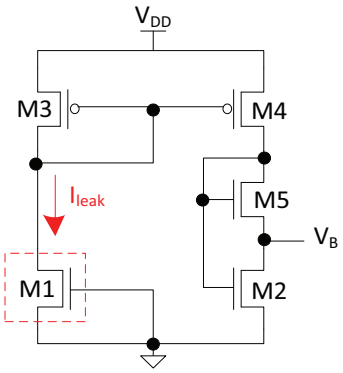


Fig. 5. V_B Generation Circuit.

used as basis to a voltage generator, which produces a proper voltage signal and sends it to the $V_{B,PMOS}$ line. To avoid the temperature influence, a carefully selected "V_B" signal is applied to the M4 gate to adjust the output signal of the current sensor. Considering that the NBTI induced degradation is a relatively slow progress, the value of V_{th} compensated to the SRAM array just needs to be calibrated only form time to time. Hence, a bypass gate M1, which is controlled by the signal "Ctrl" is introduced to bypass the current sensor during SRAM normal operation.

The standby leakage current, which is defined as the total leakage current during standby, can be expressed as follows:

$$I_{DDQ} = \sum_{i=1}^{n} I_{i0} e^{\left(-\frac{V_{thi}}{m v_T}\right)}, \tag{14}$$

where $I_{i0} = k_i(m-1)(1-exp(-V_{ds}/v_T))$, m is the body effect coefficient and v_T is the thermal voltage (k_BT/q). Submitting Eq. (8) into the previous equation, we get

$$I_{DDQ} = \sum_{i=1}^{n} I_{DDQ,i0} e^{\left(-\frac{\Delta V_{th,g}+\Delta V_{th,l}+\Delta V_{th,nbti}}{m v_T}\right)}, \tag{15}$$

where $I_{DDQ,i0} = I_{i0}exp(-V_{th0}/mv_T)$ is the nominal I_{DDQ} at time 0.

From Eq. (15) we can observe that the temporal degradation of I_{DDQ} has an exponential dependence on the ΔV_{th} induced by NBTI. The variation of I_{DDQ} induced by local process variations can be eliminated by including large number of cells in the SRAM array to achieve/approach an average value of I_{DDQ}. The global variation can be eliminated by using the V_{REF} sent to the voltage comparator as indicated in Fig.4.

C. Bias Generation and V_{th} Compensation

In order to get an accurate measurement on the value, the I_{DDQ} current sensor should be insensitive to the intra-die process and temperature variations. This can be achieved by adding an active NMOS load, which is controlled by a carefully selected V_B bias. The bias generator circuit for V_B is designed as presented in Fig.5. In this generator, the leakage current of M1 is mirrored to M4 through M3. M2 and M5 are a stacked NMOS load and their size are asymmetrically designed in order to enlarge the intra-die variations. The generated V_B is smaller than $V_{th,nmos}$, so it drives the active load in the I_{DDQ} sensor (i.e., M4 in Fig.4) to work in sub-threshold range. In such a way, the output voltage V_{out} is proportional to the V_{ds} of M3 in Fig.4 determined by I_{DDQ}, plus a temperature-process-variation compensation by V_{ds} of M4. As temperature or intra-die variations increase, the resistance of M4 in Fig.4 decreases, hence the V_{out} decreases. In such a way, the temperature and process variations are reduced in the I_{DDQ} sensor.

The global variations can be eliminated in a similar way by V_{REF}, but it requires a global voltage or current reference, which is out the scope of this work. In fact, the global variation cause a parameter shift to all the devices in a die, hence we can ignore its impact since our investigations are constrained to within-die phenomena.

The actual calculation of the V_{th} compensation value for the SRAM array can be carried out in multiple ways [12]–[14]. Considering the relative simplicity of SRAM array structure, we adapt a bias generator as shown in Fig. 6. This generator uses global band-gap circuits to generate the global voltage references of $V_{th,PMOS}$ and V_{REF}, which stand for the threshold voltage of PMOS and the V_{out} of the I_{DDQ} sensor of fresh devices.The global band-gap circuits could be designed largely enough so that they are insensitive to NBTI degradation. And these circuits are turned off most of the time and are only turned on when a calibration is required, so the aging effect of these circuits can be neglected. Two operational amplifiers are used to generate a compensating bias voltage $V_{B,PMOS}$ for the SRAM array under monitoring. The bias voltage can be calculated by the equation as follows

$$\Delta V_{B,PMOS} = V_{th0} - k_2(V_{REF} - k_1 \cdot V_{out}), \tag{16}$$

where V_{th0} is the desired V_{th} value determined at design-time, k_1 and k_2 are the amplifying magnitudes of operating amplifier *Amp1* and *Amp2* , respectively. The values of k_1 and k_2 are constants related to the sizing of transistors utilized

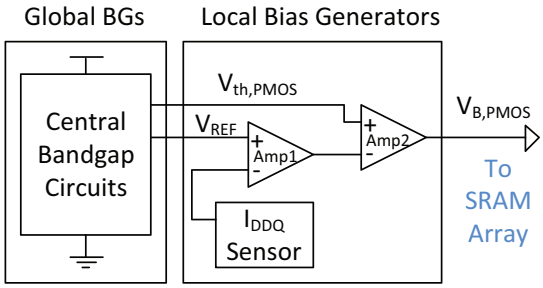


Fig. 6. The V_{th} Bias Generator for SRAM Arrays.This generator uses global band-gap circuits to generate the global voltage references of $V_{th,PMOS}$ and V_{REF}, which are used for NBTI mitigation using I_{DDQ} monitor.

in the I_{DDQ} sensor and bias generator. As SRAM array degrades due to NBTI effect with time, the leakage current I_{DDQ} will increase. Consequently, the value of V_{out} will increase correspondingly, as well as the absolute value of the compensating bias voltage V_{out}. Hence, the SRAM cells are biased dynamically according to the severity of the NBTI degradation.

V. Results and Discussion

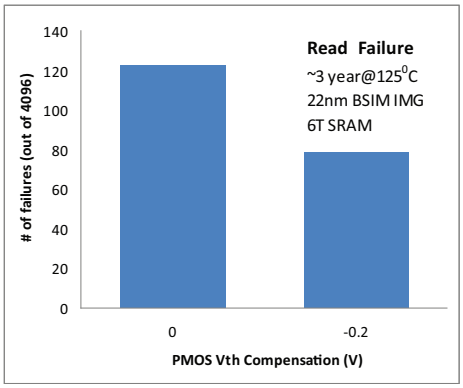
In order to evaluate the efficiency of the proposed compensation technique, we run circuit simulations using the BSIM CMG/IMG Models [15] [16] for 22nm FinFET devices. The failure probability of SRAM cells and SNM are used as evaluation metrics. The PV variations are generated using a Guassian distribution for RDF-induced V_{th} variation and the dynamic workload condition are simulated by different signal probability ratio of the stored value into the value nodes of the SRAM cell.

First, we investigate the improvements induced by the proposed scheme on different operation modes of the SRAM array. The simulation is conducted at an accelerated temperature $125°C$ for 10^8 seconds ($\sim$3 years). From Fig. 7 we can clearly observe that with the proposed V_{th} technique, the stability of the SRAM cells for READ, WRITE, and HOLD operations is significantly improved.

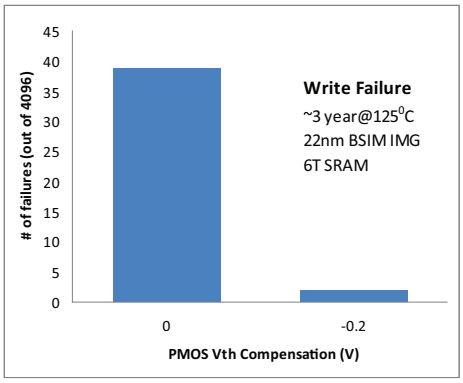
As we can deduce from Fig. 7, the READ stability is the major remaining reliability issue even if V_{th} compensation is utilized. For that reason, we further investigate the SNM degradation during time with/without V_{th} compensation, and the results are graphicaly presented in Fig. 8. We assumed a balanced signal probability for both V_L and V_R nodes and, as one can observe in the figure, our experiments suggest that: (i) without V_{th} compensation, READ SNM degrades with time significantly; and (ii) with V_{th} compensation introduced, the SNM degradation is reduced in a very limited range during the operational lifetime. As a result, by introducing a V_{th} compensation technique into the SRAM array, we can extend its lifetime for longer operational duration and improved reliability.

VI. Conclusions

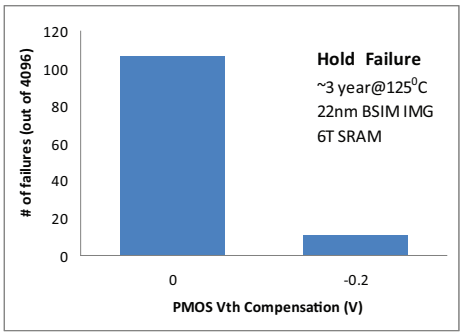
In this paper, we investigated the influence of stochastic input signal on long-term reliability under NBTI stress and



(a) Read Stability



(b) Write Stability



(c) Hold Stability

Fig. 7. Stability Improvements by V_{th} Compensation using IG-FinFET 6T SRAM Cell.

the effect of random process variations on NBTI degradation. We also propose an NBTI mitigation technique based on an I_{DDQ} current sensor, utilizing threshold voltage compensation in an IG-FinFET SRAM structure. We evaluated the impact of our proposal on the RAM stability by means of SPICE simulations with the BSIM-CMG/IMG models for 22nm FinFET devices. Our simulations conducted at an accelerated temperature $125°C$ for 10^8 seconds ($\sim$3 years) indicate that a V_{th} compensation of 0.2V can almost preserve the WRITE and HOLD stability of the fresh device even after 3 years, while for the READ stability the compensation mechanism is less effective. However the READ Static Noise Margin

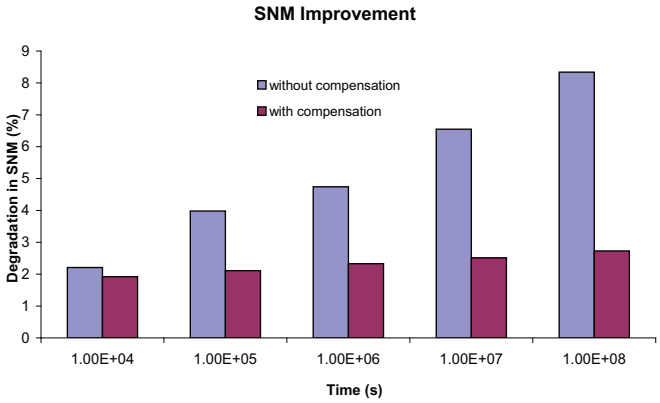


Fig. 8. NBTI Induced READ SNM Degradation (in percentage) Over 3 Years Time Period, with/without V_{th} Compensation.

(SNM) experiences an insignificant decrease over the 3 years time span in the presence of a V_{th} compensation, while without compensation it decreases by a x4 factor. Thus we can conclude that the proposed technique can improve the stability of SRAM array during its operational life, hence improve the performance and reliability of the system.

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