On Optimizing Test Cost for Wafer-to-Wafer 3D-Stacked ICs

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***Abstract*— The increasing demand for more sophisticated ICs with more functionality mostly was realized by downscaling and increasing the number of transistors. A technology that promises further increase of transistor density (in addition with heterogeneous integration, better performance and less power dissipation at a smaller footprint) is the three-dimensional stacked ICs (3D-SICs). Several stacking approaches are under development to manufacture such 3D-SICs. Wafer-to-Wafer (W2W) stacking seems the most favorable approach when high manufacturing throughput, thinned wafers and small die handling is required. However, efficient and optimal test approaches to satisfy the required quality are still subject to research. Each manufactured 3D-SIC undergoes a test and therefore optimizing test cost will have a large overall impact. This paper discusses test cost optimization for W2W 3D-SICs. It first introduces a framework covering different test flows for 3D W2W ICs. Test flows that include pre-bond tests can benefit from wafer matching; in wafer matching a software algorithm is used to increase the compound yield by stacking wafers with similar fault distributions. Subsequently, the paper proposes a cost model to evaluate and estimate the impact of test flows on the overall 3D-SIC cost. Our simulation results show that test flows with pre-bond testing in general significantly reduce the overall cost. These test flows benefit mostly from the yield increase due to wafer matching.**

Keywords: *W2W, 3D W2W test flows, pre-bond testing, wafer matching*

I. Introduction

The increasing demand for more functionality on ICs has been met by the semiconductor industry adhering to Moore's law. Recent enhancements in process development enable the fabrication of three dimensional stacked ICs (3D-SICs), which are electrically interconnected by Through Silicon Vias (TSV). This opened up new research directions that could be investigated to continue the trend of performance increase. A TSV based 3D-SIC is an emerging technology that provides a smaller footprint, higher interconnect density between stacked dies, higher performance and lower power consumption due to shorter wires as compared to planar ICs [1]. Moreover, heterogeneous integration in 3D-SICs allows dies to be manufactured with dissimilar processing and technology nodes; for example, memory layers can be stacked on a processor.

The key manufacturing steps in assembling 3D-SICs are the stacking and the bonding of dies. The three existing bonding methods are Die-to-Die (D2D), Die-to-Wafer (D2W) and Wafer-to-Wafer (W2W) bonding [2]. High alignment accuracy is feasible in D2D and D2W bonding, but it impacts the throughput negatively. In D2D and D2W bonding, Known Good Die (KGD) stacking can be applied to prevent faulty dies from being stacked [2]. W2W stacking allows for (a) high manufacturing throughput due to single wafer alignment, and (b) thinned wafers and small die handling. Due to their regularity, memories and FPGAs are very attractive to be used in W2W stacking. However, the major drawback of W2W stacking is the low compound yield especially with increased number of stacked layers.

Increasing compound yield in W2W stacking has been addressed recently by some authors [3–6]; all of them use wafer matching; i.e., a technique in which wafers with similar die fault distributions are stacked. To use wafer matching, wafers must be tested before bonding them; i.e., pre-bond test. Using appropriate test strategies/flows will therefore have a large impact on the compound yield. This topic is also discussed in [5,6]. However, the works presented by the authors have many limitations. For instance, they consider only three test flows; in addition, not all cost components were considered when the overall 3D-SIC cost was determined, etc.

This paper explores the whole space of test flows for W2W 3D-SICs and their impact on the overall cost and compound yield, while considering all cost components such as manufacturing, test, packaging etc. The main contributions of this paper are:

- A classification of 3D W2W test flows.
- An analytical model that formulates the cost of 3D-SICs for W2W stacked ICs.
- Analysis of the impact of test flows on the compound yield and overall cost.

The remainder of this paper is organized as follows. Section II discusses the related prior work in wafer matching and 3D-SIC testing. Section III discusses the test framework. Section IV presents the cost model. Section V describes the performed experiments. The simulation results are analyzed in Section VI. Finally, Section VII concludes this paper.

II. Related Prior Work

This section discusses the prior work in wafer matching and 3D-SIC testing in Sections II-A and II-B respectively.

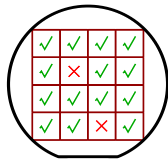

Fig. 1. Pre-bond tested wafer with good and bad dies.

A. Wafer matching

Wafer matching is a technique to improve the compound yield by stacking wafers with the same or similar die fault distributions (fault maps). This technique has been addressed recently by some authors [3–6]; different wafer matching techniques have been introduced.

The authors in [3–5] use static repositories to perform the wafer matching, while in [6] the authors use running repositories. In [6], the authors consider different matching criteria as well. In a static repository, wafers are only replenished after the whole cassette is empty, while in a running repository selected wafers are immediately replenished. In addition, [4] uses the symmetrical structure of a wafer to increase the matching combination (by rotating wafers).

Wafer matching necessitates pre-bond tests to obtain the fault map distributions of the dies on the wafer. Figure 1 shows an example of a wafer with sixteen dies, where two dies have been identified faulty during pre-bond testing. After collecting several wafers of each layer of the stack in different repositories, matching between the repositories can take place.

The pre-bond test cost only pays off in case sufficient compound yield is realized. This yield improvement can be significant in case of a large stack size or low die yield [5]. However, this yield improvement decreases for higher die yield. For example, for a stack size of two layers with a die yield of 85% and 1278 dies per wafer, wafer matching is able to increase the compound yield from 72.3% (for random stacking) to 73.1% [6]. This dilemma motives us to analyze the cost trade-off between pre-bond test cost and yield increase for the different test flows.

B. Testing

Optimizing test cost is a challenge that can significantly contribute to the overall cost reduction. Choosing an optimal and efficient test flow requires the analysis of all possible flows using an appropriate test cost model. Research on this topic is still in its infancy stage and very limited work is published [7–9]. In [7], the author considered a manufacturing cost model for 3D monolithic memory integrated circuits; cost improvement of 3D with respect to 2D (for different 3D stack sizes) was modeled. In [8], the authors developed a 3D-cost model to determine the optimal stack size for a given 3D-SICs circuit, where they restricted the variable parameters to only die yield and die size. In [9], the authors proposed a 3D cost model for Die-to-Wafer (D2W) and Wafer-to-Wafer (W2W) stacking. However, none of these published work is able to model the impact of the test cost

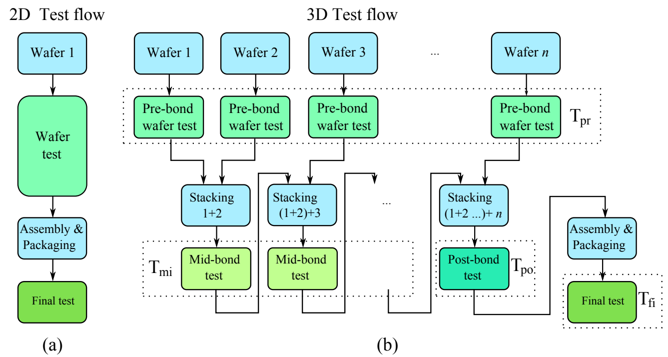

Fig. 2. 2D versus 3D D2W test flows

on the overall 3D-SIC cost since none of them considers the different test moments and test flows. In our previous work [10], a basic cost model considering the impact of different test flows on the overall 3D-SIC cost was presented. A refined version of such a model, where many limitation are addressed, is presented in [11]. However, both were limited to D2W stacking in which a freedom exist to perform Known Good Die (KGD) stacking.

III. W2W Test Framework

In this section, we derive a test framework consisting of test flows for W2W stacked 3D-SICs. First, Section III-A describes the possible test moments in time. Thereafter, test flows are compiled into a framework in Section III-B by applying different tests at the considered test moments.

A. 3D Test Moments

For conventional testing of 2D ICs, two types of tests can be defined (as shown in Figure 2(a) [12]): a wafer test and a final test. A wafer test screens out faulty ICs prior to assembly and packaging in order to prevent unnecessary packaging costs, while a final test guarantees the quality of the packaged chip to reduce test escapes. A trade-off between the additional wafer test costs versus savings in packaging cost determines the applicability of this test. Furthermore, the test decision is based on the manufacturing yield and fault coverage. In case the yield is high enough, the test can be skipped or performed at low cost (i.e., low fault coverage).

For 3D SICs, additional tests -such as partial created stack tests- be defined. Figure 1(b) shows the natural test moments during the manufacturing of 3D-SICs. Four test moments can be distinguished in time, as depicted in Figure 2(b) and explained next.

1) T_{pr}: n pre-bond wafer tests, since there are n layers to be stacked. T_{pr} tests prevent faulty dies entering the stack. Two different types of test can be applied here. Traditional functionality of the chip can be tested for, but also preliminary TSV tests can be applied (in case of via-first [13]) as well.
2) T_{mi}: $n-2$ mid-bond tests applicable for partial created stacks. In this case, either dies, interconnects formed by the TSVs between them, a combination of the former two or none of them can be tested. Good tested dies in the pre-bond test phase could get corrupted

TABLE I
3D Test Flows

Flow	Pre-bond	Post-bond	Final
t1	-	-	int $\rightarrow$ die
t2a	-	int	int $\rightarrow$ die
t2b	-	die	int $\rightarrow$ die
t2c	-	int $\rightarrow$ die	int $\rightarrow$ die
t3	yes	-	int $\rightarrow$ die
t4a	yes	int	int $\rightarrow$ die
t4b	yes	die	int $\rightarrow$ die
t4c	yes	int $\rightarrow$ die	int $\rightarrow$ die

during the stacking process as a consequence of e.g., die thinning, and bonding [14].

3) T_{po}: one post-bond test. This test can be applied after the complete stack is formed. Analogous to wafer testing in the 2D test flow, T_{pr} can be applied to save unnecessary assembly and packaging costs. Here, both dies and interconnects between them can be tested for.
4) T_{fi}: one final test can be applied after assembly and packaging to ensure the required quality of the complete 3D-SIC. Other specific packaging related tests could be applied at this test moment as well.

Note that in total $2{\cdot}n$ different test moments can be identified versus 2 test moments for planar ICs. A 3D test flow can be defined as a combination of tests applied at the four test moments.

However, in this paper, mid-bond tests T_{mi} are ignored as dies are stacked based on the wafer level. Intermediate tests can not prevent faulty dies to be stacked as the case is for D2W stacking.

B. W2W Testflows

From the test moments of the previous section, 8 test flows are derived and depicted in Table I. The first column denotes the name of the particular test flow. The second column specifies whether a pre-bond test is performed or not. This pre-bond test consists of either a die, TSV or die and TSV test. The more sophisticated the pre-bond test, the more faulty dies can be identified. This increases the effectiveness of wafer matching at a higher test cost.

The third column presents the performed test during post-bond. Here, the option exist to skip this test, or to test for interconnects, dies, or both of them. In case both interconnects and dies are tested, the symbol $\rightarrow$ is used to denote the test sequence order, i.e., for int $\rightarrow$ die interconnects are tested prior dies. We do no consider the die $\rightarrow$ int for three reasons: (1) testing of dies is assumed to be much more expensive (more test vectors), (2) prior to test the dies in the 3D stack, interconnects that access that die must be tested, (3) to obtain a manageable space of test flows.

The last column of the table specifies the final test after IC packaging. The applied test in this stage determines the quality, test escapes of the product. We assume that a full test is performed in this final test phase.

IV. Cost Model

Obviously, in order to determine the most cost-effective test flow the test cost should be specified. However, this is by far not enough to produce a fair comparison of test flows. Other cost classes have to be specified as input requirements as they have a large impact on the overall cost as well. We consider three classes: manufacturing, test and packaging as depicted in Figure 3.

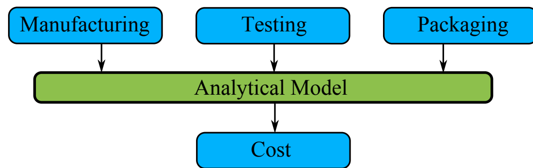

Fig. 3. Cost Model Interface.

- Manufacturing cost: it covers two types of parameters and are related to cost and yield. The most obvious ones related to 3D are the die size/cost and stacking operation. The stack yield is determined by the yield of the dies that enter the stack, the yield of the interconnects between the dies and the yield of the stacking operation.
- Test cost: this is related to the required cost associated with (a) pre-bond test, (b) mid-bond test, (c) post-bond test and (d) final test as defined previously. A test consists of two parts, a test for interconnects between the stacked dies and the dies themselves. The vertical interconnects are new in the stack and testing them after stacking seems rational.
- Packaging cost: the assembly and packaging cost.

The parameters used to define these classes are described in Section V-A. In the remainder of this section we define the cost evaluation.

The cost per good 3D-SIC C_{GD} can be defined by:

$$C_{GD} = \frac{\sum_{i=1}^{n} C_{die,i} + \sum_{i=1}^{n-1} C_{3D,i} + C_t + C_p}{Y_s} \quad (1)$$

Here, $C_{die,i}$ represents the manufacturing cost of the die on layer i; in total there are n stacked layers. The parameter $C_{3D,i}$ denotes the stacking cost for a 3D-SIC. Note that an n-layered stack only requires n-1 stacking operations. C_t represents the test cost, C_p the packaging cost and Y_s is the overall stack yield per 3D-SIC.

Equation 1 can be written into:

$$C_{GD} = \frac{n \cdot C_w + (n-1) \cdot \gamma \cdot C_w + r_p \cdot \beta \cdot C_w + C_t}{Y_s \cdot d} \quad (2)$$

Here, $\gamma = \frac{C_{3D}}{C_w}$ the ratio between the 3D stacking and wafer cost, $\beta = \frac{C_p}{C_w}$ the ratio between packaging and the wafer cost. Here, C_w is the cost per wafer (we assume this is equal for each layer as in memories), r_p the fraction of 3D-SICs that are packaged per stacked wafer set, C_p the packaging cost per 3D-SIC, C_t the test cost. Finally, Y_s and d represent the overall yield of the 3D-SIC and the number of dies per wafer respectively.

V. Case-study

A. Experiment setup

a) Manufacturing: The manufacturing class includes parameters related to the manufacturing of 3D-SICs such

as wafer cost, costs required for wafer processing, TSV fabrication and 3D stacking/bonding. However, it includes also parameters related to the die and stack yield.

For wafers and their processing, we used the cost models of [15] and [16]; the total price of a 300 mm wafer is estimated at approximately \$2779. The model in [15] considers a variety of costs, including installation, maintenance, lithography and material. For TSV fabrication, the work of EMC-3D consortium [17] is used; the cost to fabricate 5 μm TSVs in a single wafer is assumed to be \$190 and these cost are additive to the wafer cost. We assume the cost of manufacturing TSVs to be 60% of the total 3D cost [18].

The die yield is based on the stacking process in [5], where a standard 300 mm diameter wafer is used with an edge clearance of 3 mm. The work assumes a defect density of d_0 = 0.5 defects/cm^2 and a defect clustering parameter $\alpha = 0.5$. With a die area $A = 50\ mm^2$, the number of Gross Dies per Wafer (GDW) are estimated to be d=1278 [19]. With the negative binomial formula for yield, a die yield of $Y_D = (1 + \frac{A \cdot d_0}{\alpha})^{-\alpha}$ = 81.65% is expected [20]. For the stack size we assume a default stack size n=2. The stacking yield is composed out of two parameters: the interconnect (TSV) yield Y_{INT} and the stacked-die yield Y_{SD}. In our simulations, the interconnect yield Y_{INT} is considered to be 97%. For the good dies that enter the stack, a small probability exists that they get corrupted during stacking; this is modeled by the stacked-die yield Y_{SD} and is assumed to be 99%, similar as in [5].

The compound yield of a 3D-SIC can be formulated as follows in case no wafer matching is used:

$$Y_s = Y_D^n \cdot Y_{SD}^{(n-1)} \cdot Y_{INT}^{(n-1)} \quad (3)$$

In case wafer matching is used, this expression can formulated by

$$Y_s = Y(n,k) \cdot Y_{SD}^{(n-1)} \cdot Y_{INT}^{(n-1)} \quad (4)$$

where $Y(n,k)$ the compound yield of the dies after being matched using a repository with k wafers. In case the repository size is k=1, $Y(n,k) = Y_d^n$.

b) Test: The test class consists of parameters that are related to the test cost of dies and interconnects in the stack and to the test flows.

To estimate the test cost per die, the model in [20] is used; it includes depreciation, maintenance and operating cost and assumes five ATE machines operating simultaneously. The derived test cost equals t_{die}=3.82 \$cent/second per die. Assuming a test time of 6 seconds per die, the test cost will be t_{int}=\$0.23 per die. To estimate the interconnect test cost, a ratio of 1:100 between the test time of dies and interconnects is assumed (as in [5]).

The cost related to each test flow depends on the number of tests that are performed. The test cost for each test flow is the sum of the test costs in the pre-bond (t_{pr}), in the post-bond (t_{po}) and final phase (t_{fi}), hence $C_t = t_{pr} + t_{po} + t_{fi}$. Table II shows this cost. For example, in test flow t1a only a final test is applied. Here, all the interconnects are tested at a cost equal to $n_i = (n-1) \cdot d \cdot t_{int}$. After the interconnects are tested, only the non-faulty dies are further tested at a cost equal to $Y_{INT}^{(n-1)} \cdot n_d$. Here, $n_d = n \cdot d \cdot t_{die}$ presents the test cost for all the dies. As a second example, consider the test flow t3a that contains a pre-bond test. All dies are tested at a cost of n_d in this phase. Due to wafer matching, it already know that the yield of the dies that enter the stack equals $Y(n,k)$. Therefore, in the final test stage only the interconnects of the good stacks have to be tested at a cost $Y(n,k) \cdot n_i$. After new faulty interconnects have been detected the cost to test the remain dies equals $Y(n,k) \cdot Y_{INT}^{(n-1)} \cdot n_d$.

c) Packaging: The packaging cost forms a significant fraction of the overall cost and depends on the used technique [21]. In this paper, we assume the packaging cost to be 50% of the wafer cost. The overall packaging cost depends on the number of packaged ICs which depends on the selected test flow. For example, in test flow t1a where only a final test is applied, all ICs are packaged (i.e., the packaging ratio r_p=1). Table III summarizes the packaging ratios of each test flow. The table consists of 3 columns; the first column depicts the test flow, the second column shows whether it is pre-bond tested or not, and the last column contains the ratio of packaged 3D-SICs. The ratio of packaged 3D-SICs depends on both the yield and the applied test. For example, test flow t3a contains a pre-bond test and a final test. The yield of the dies that enter the stack equals $Y(n,k)$ after applying wafer matching and thus some of the faulty stacks are known at this time. Since no other tests are performed only the fraction of 3D-SICs that are considered good are packaged (i.e., $Y(n,k)$). If for example also an interconnect test is performed in the post-bond test (test flow t4a), then 3D-SICs with faulty interconnects can also be detected and prevented from being packaged, leading to a packaging ratio of $Y(n,k) \cdot Y_{INT}^{(n-1)}$.

TABLE II
TEST COST

flow	t_{pr}	t_{po}	t_{fi}
t1a	-	-	$n_i + Y_{INT}^{(n-1)} \cdot n_d$
t2a	-	n_i	$Y_{INT}^{(n-1)} \cdot (n_i + n_d)$
t2b	-	n_d	$Y_D^n \cdot Y_{SD}^{(n-1)} \cdot \left\{n_i + Y_{INT}^{(n-1)} \cdot n_d\right\}$
t2c	-	$n_i + Y_{INT}^{(n-1)} \cdot n_d$	$Y_D^n \cdot Y_{SD}^{(n-1)} \cdot Y_{INT}^{(n-1)} \cdot \{n_i + n_d\}$
t3a	n_d	-	$Y(n,k) \cdot \left\{n_i + Y_{INT}^{(n-1)} \cdot n_d\right\}$
t4a	n_d	$Y(n,k) \cdot n_i$	$Y(n,k) \cdot Y_{INT}^{(n-1)} \cdot (n_i + n_d)$
t4b	n_d	$Y(n,k) \cdot n_d$	$Y(n,k) \cdot Y_{SD}^{(n-1)} \cdot \left\{n_i + Y_{INT}^{(n-1)} \cdot n_d\right\}$
t4c	n_d	$Y(n,k) \cdot \left\{n_i + Y_{INT}^{(n-1)} \cdot n_d\right\}$	$Y(n,k) \cdot Y_{SD}^{(n-1)} \cdot Y_{INT}^{(n-1)} \cdot \{n_i + n_d\}$

TABLE III
PACKAGING COST

Test flow	Pre-bond	Post-bond	r_p
t1a	no	no	1
t2a	no	int	$Y_{INT}^{(n-1)}$
t2b	no	die	$Y_D^n \cdot Y_{SD}^{(n-1)}$
t2c	no	int + die	$Y_D^n \cdot Y_{SD}^{(n-1)} \cdot Y_{INT}^{(n-1)}$
t3a	yes	no	$Y(n,k)$
t4a	yes	int	$Y(n,k) \cdot Y_{INT}^{(n-1)}$
t4b	yes	die	$Y(n,k) \cdot Y_{SD}^{(n-1)}$
t4c	yes	int + die	$Y(n,k) \cdot Y_{SD}^{(n-1)} \cdot Y_{INT}^{(n-1)}$

TABLE IV
YIELD WAFER MATCHING VS RANDOM W2W STACKING

wafer matching	$n = 2$	$n = 3$	$n = 4$	$n = 5$	$n = 6$
no	66.67	54.43	44.45	36.29	29.63
yes	67.61	56.25	47.12	39.68	33.54

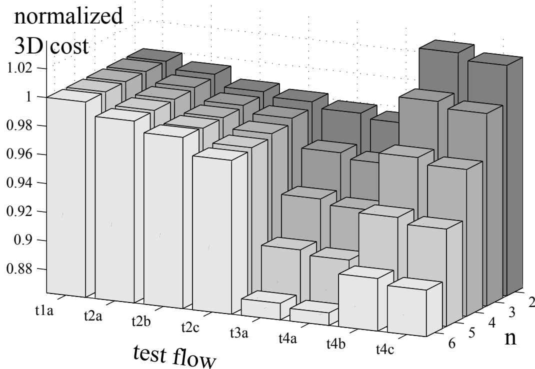

Fig. 4. Normalized 3D cost versus stack size.

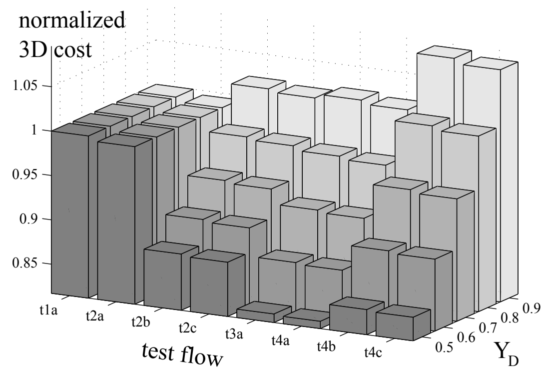

Fig. 5. Normalized 3D cost versus die yield.

B. Experiments

In this subsection, we describe the experiments performed using the test flows of Table I and there cost calculation calculation of Section IV. The parameters considered so far are the default values for each experiment. In addition, the following experiments have been conducted:

1) **Impact of stack size:** In this experiment, the impact of different test flows will be investigated while considering different stack sizes $2 \leq n \leq 6$. Table IV shows the stack yield belonging to this stack size with and without wafer matching [6]. These yields do not include the stacked-die and interconnect yield.
2) **Impact of die yield:** A similar experiment as the previous one, but now by having a fixed stack size of n=2, and variable die yield Y_D: 60%$\leq Y_D \leq$90%
3) **Impact of stacking yield:** In this case, the default process parameters are used (e.g., n=2, Y_D=81.65%, etc.), but the stacking yield is varied; this yield consists of interconnect yield Y_{INT} and stacked-die yield Y_{SD}: 91%$\leq Y_{INT}, Y_{SD} \leq$99%
4) **Impact of packaging cost:** To simulate a different packaging cost we consider $0.2 \leq \beta \leq 0.8$, while fixing all the other parameters to their default values.

The results of the experiments are described in the next section.

VI. SIMULATION RESULTS

In this section, the simulation results are presented. The impact of different test flows are analyzed for each experiment.

A. Impact of stack size

Figure 4 depicts the relative overall 3D-SIC cost of the test flows for a stack size between $2 \leq n \leq 6$. Here, the 3D cost for each test flow is normalized to the 3D cost of TF1 for each stack size. The following conclusions can be drawn from the figure:

- Test flows with pre-bond tests (e.g., t3a and t4a) can reduce the overall cost. The larger n, the larger this reduction.
- Test flow t4a is the most cost-effective test flow irrespective of n.
- Test flows t2a, t2b, t2c have a marginal impact on the cost reduction irrespective of n. The difference with the remaining test flows is due to the yield increase achieved by wafer matching (see Table IV).
- Re-testing dies in the post-bond phase for t4b and t4c only adds to the cost when compared to t4a. Due to a high stacking yield, re-testing of dies is not beneficial.

B. Impact of die yield

Figure 5 depicts the relative 3D cost of the test flows with a die yield varying between 50%$\leq Y_D \leq$90% for the default parameters. Here, the 3D cost for each test flow is normalized to the 3D cost of TF1. From the figure we conclude the following.

- Test flows with pre-bond tests significantly reduce the overall cost for die yields lower than 90%. The lower the die yield the larger the reduction (except for t2a since this test flow does not test for dies during the pre-bond and post-bond phase).
- Test flow t2a has a marginal impact on the cost, irrespective of the die yield. This is not the case for t2b and t2c, as they both test for dies in the post-bond phase. The lower the die yield, the more faulty ICs are detected prior to packaging.
- Similar conclusions can be drawn as those from Figure 4 for the test flows enabled with pre-bond testing. Applying a pre-bond test (thus wafer matching), and testing only for the interconnects during the post-bond phase results in most cases into the overall lowest cost.

C. Impact of stacking yield

The stacking yield consists of the interconnect yield and stacked die yield. Due to space shortage only the results of the stacked die yield experiment are shown.

Figure 6 depicts this experiment and shows the overall 3D cost versus stacked die yield for the test flows. The 3D cost of the flows are normalized to the cost of TF1 for each stacking yield.

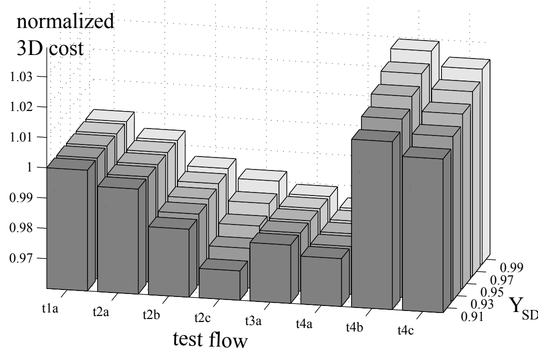

Fig. 6. Normalized 3D cost versus stacked die yield.

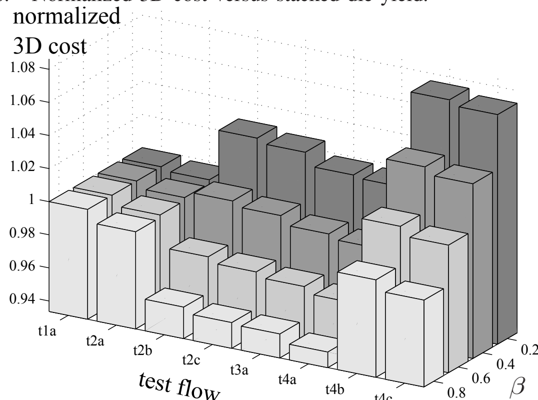

Fig. 7. Normalized 3D cost versus packaging cost.

From the figure we conclude that t2c and t4a are the most cost-effective test flows. If Y_{SD} is very high (i.e., 99%), then t4a perfroms best. However, when Y_{SD} reduces t2c becomes most cost efficient. In this case, the benefit of wafer matching reduces due to a larger number of stack faults.

D. Impact of packaging cost

Figure 7 depicts the relative 3D cost of the test flows for $0.2 \leq \beta \leq 0.8$. From the figure we conclude the following.

- For very low packaging costs (β=0.2), test flows that test dies in the pre-bond phase (t3a, t4a, t4b and t4c) and and mid-bond phase (t2b, t2c, t4b and t4) negatively impact the 3D cost. The cost of testing the dies is not preventing enough faulty 3D-SICs to be packaged. For a low packaging cost it is more advantageous to skip die tests in the pre-bond and post-bond phase.
- For increasing β, test flow t4a becomes the most efficient one. This test flow significantly reduce the overall cost for $\beta \geq 0.8$.
- Test flow t2a again has a marginal impact on the cost, irrespective of the packaging cost. The high interconnect yield and the testing of interconnects only during the post-bond test impacts the 3D cost minimally.

In order to optimize the overall test cost, the appropriate test flow should be selected to reduce the 3D-SIC cost. Therefore, cost modeling is very important.

VII. Conclusion

This paper investigated the impact of several 3D test flows on the total 3D cost in W2W stacking. It introduced a framework of test flows for 3D-SIC testing; each test flow is based on a combination of tests applied at three test moments, i.e., the pre-bond wafer test, the post-bond test and the final test. A model that considers manufacturing, test and packaging cost is presented in order to evaluate the impact of different test flows on the overall cost.

The simulation results showed that the pre-bond testings is extremely important in order to reduce overall cost. The benefit of having pre-bond tests is a yield increase due to wafer matching. In most of the cases, this approved to be beneficial. In the post-bond test phase, primarily interconnect test are of relevance. In some cases, also die tests proved to be cost effective. The final test phase included both tests for interconnects and dies.

The conclusion of the paper indicates that in order to manufacture 3D-ICs at optimum cost for W2W stacking, any DFT has to consider not only the infrastructure for pre-bond tests, but also take into consideration to test for interconnects during the post-bond phase.

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