Analyzing Combined Impacts of Parameter Variations and BTI in Nano-scale Logical Gates

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Abstract Bias Temperature Instability (BTI) and parameter variations are threats to reliability of CMOS circuits. This paper presents analyses of BTI and parameter variations on delay, static and dynamic power consumptions of logic gates. The results show that for BTI only case, the impact on delay is strongly temperature and duty cycle dependent. For example, in a NOR gate the delay at 75^{o}C is 56% higher than at 25^{o}C; and at 40% duty cycle is 67% higher than at 60%. The results also show that BTI causes static and dynamic power reduction. The analysis is redone for BTI by incorporating parameter variation. Monte Carlo simulation results reveal that BTI impact is exacerbated by the parameter variations with up to 15%.

1 Introduction

CMOS technology miniaturization has caused variability and reliability issues in the scaled technologies [1]. From the variability perspective, magnitudes of the parameter (process and temperature) variations are growing in scaled technologies. The process variation is due to the imperfection in the fabrication [1]. Similarly, temperature variation results from the changing inputs and operational conditions. On the other hand, among the reliability issues, Bias Temperature Instability (BTI) -Negative BTI (NBTI) in PMOS transistors and Positive BTI (PBTI) in NMOS transistors- has drawn attention [2]. Both parameter variations and BTI can impact key performance parameters, such as, delay, static and dynamic powers.

Recently, few papers have addressed combined impacts of variability and NBTI at different levels [3,4]. For instance, Kumar et al., in [3] investigated the effect in ring oscillators and SRAM cells. Siddiqua et al., in [4] explored both NBTI and process variation in an SRAM cell array and other benchmark circuits. Although the aforementioned work analyzed combined impacts of NBTI and process variations at circuit levels. They did not consider the parameter variations (both process and temperature); in addition they restrict their analysis to NBTI rather than covering both NBTI and PBTI.

This paper presents a simulation based analysis for logic gates that encompasses both parameter variations (process and temperature) and BTI (NBTI and PBTI). The main contributions of this paper are:

- Incorporate both NBTI and PBTI in simulation and analyze their impacts on gate delays.
- Investigate BTI impacts on the static and dynamic power consumptions of the gates.
- Explore the impacts of parameter variations and their combined effect with the BTI at the gate level.

The rest of the paper is organized as follows: Section 2 presents background. Section 3 analyzes *only* BTI impact. Section 4 analyzes the combined impact of BTI and parameter variations and Section 5 presents conclusions.

2 Background and Analysis Framework

Fig. 1(a) shows the threshold voltage increment (ΔV_{th}) due to BTI, parameter variations and their interaction. This section reviews BTI mechanism, parameter variation, delay model, and presents the analysis framework.

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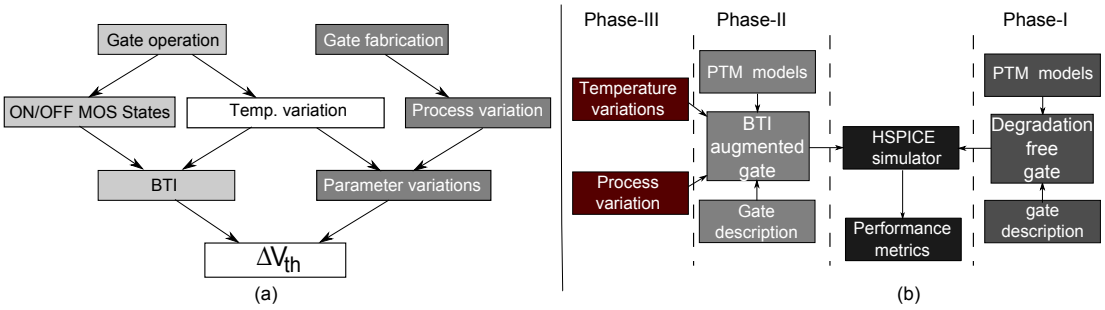


Fig. 1 (a) ΔV_{th} due to BTI and parameter variations (b) BTI and parameter variations analysis framework

2.1 BTI Mechanism:

BTI degradation produces traps at the Si-SiO_2 interface. The interface interface traps oppose the applied gate stress resulting in the threshold voltage increment (ΔV_{th}) of MOS transistors [5]. The relation between the number of the traps (N_{IT}) and ΔV_{th} is:

$$\Delta V_{th} = (1+m).q.N_{IT}/C_{ox}.\gamma.\chi, \quad (1)$$

where m, q, and C_{ox} are the holes/mobility degradation that contribute to the V_{th} increment, electron charge, and oxide capacitance, respectively. Moreover, γ represents the stress duration of the transistor with respect to the total input period and χ is a BTI coefficient.

2.2 Parameter variations:

As shown in Fig. 1, parameter variations may be a result of either the process variation or the temperature variation. These two variations are described as follows:

Process variation:

The variations in process parameters (e.g., channel effective length (L_{eff}), width (W_{eff})) affect the V_{th} of the MOS transistor, as given by Stolk's formula [6]:

$$\sigma_{V_{th}} = C.\frac{1}{\sqrt{W_{eff}.L_{eff}}}, \quad (2)$$

where C is a technology dependent constant.

Temperature variation:

The generalized expression for MOS transistor V_{th} is given by [7]:

$$V_{th} = C_{vt} - \frac{Q_{ss}}{C_o} + \Phi_{ms}, \quad (3)$$

where C_{vt} is a constant and Q_{ss} is the surface charge at the Si-SiO_2 interface. Moreover, Φ_{ms} is a temperature dependent Si-SiO_2 work function difference as claimed in [7]. The temperature increment reduces the work function difference and consequently lowers the V_{th} and speed-up the transistor.

2.3 Gate Delay Model

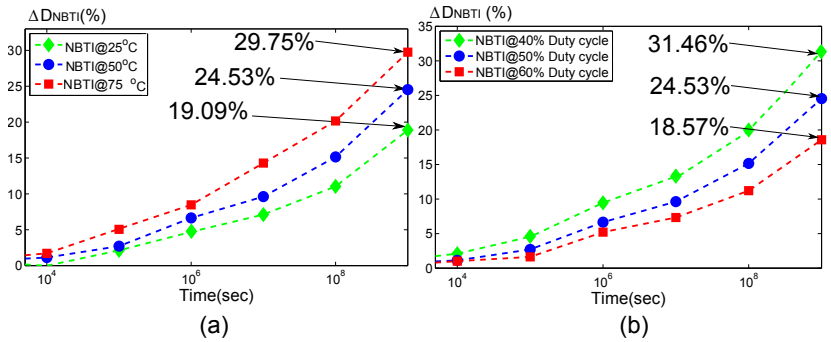
Threshold voltage variation of the MOS transistor either due to BTI or parameter variations has its impact on the gate delay. A generalized formula that relate V_{th} variations (ΔV_{th}) in a transistor to the gate delay is given by:

$$\Delta D = \frac{n.\Delta V_{th}}{(V_{gs} - V_{th})}, \quad (4)$$

where n is a constant representing the velocity saturation index of carriers in the MOS transistor channel.

2.4 Analysis Framework

The analyses presented in this paper address the impacts of both BTI and parameter variations in the gates. For this analysis, a framework shown in Fig. 1(b) has been developed. Phase-I of the figure is used for degradation free simulation of the gates. For this case, the gates are synthesized using 45nm PTM transistor models [10] and simulated using HSPICE to get a reference for analyses. Thereafter, at Phase-II of the figure Verilog-A modules are added to each transistor to get BTI augmented gates. Depending on biasing input of each transistor, the Verilog-A module produces ΔV_{th} that binds BTI impact to the additional gate delay (ΔD). Finally, parameter variations are introduced in Phase-III to investigate the combined impacts of BTI and parameter variations.



Delay increment (%) in logic gates

Temp	D.C	NOR	OR	NAND	AND
25°C	40	23.88	6.04	9.88	14.57
	50	19.09	8.79	7.49	16.88
	60	14.49	12.87	6.43	21.47
50°C	40	29.51	9.98	16.07	17.32
	50	24.53	14.19	14.75	19.68
	60	23.14	18.36	12.70	28.93
75°C	40	34.12	12.26	18.58	22.77
	50	29.75	16.87	16.60	22.48
	60	24.56	25.66	15.94	30.84

(c)

Fig. 2 (a) BTI induced ΔD in NOR gate at different temperatures (b) BTI induced ΔD in NOR gate at different duty cycles (c) BTI induced ΔD in other gates at different temperatures and duty cycles

3 BTI Impacts

This section analyzes BTI impacts in logic gates. Initially, it presents BTI impact on delay degradation of the gates. Thereafter, it investigates BTI impacts on static and dynamic powers of the gates.

3.1 Delay Degradation:

Analyses in this paper are inspired by the observations that the duty cycle and temperature have *significant* contributions to the BTI induced delay in the gates.

Let us consider a two inputs NOR gate that is analyzed for worst case BTI impact using the previously mentioned framework. The analyses are carried out for both NBTI and PBTI in the transistors at various temperature and results are shown in Fig. 2(a). The figure shows that BTI causes only 19.09% additional delay to gate at 25^{o}C. However, when the temperature increases to 75^{o}C, BTI induced delay approaches to 29.75%. Fig. 2(b) shows that BTI induced delay variation in a NOR gate under the three duty cycles has a significant impact on the BTI induced delays. For example, at 50% duty cycle BTI cause 24.53% additional delays to the gate. However, at 40% duty cycle, it increases to 31.46%, while the delay due to BTI becomes only 18.57% at 60% duty cycle.

The analyses are extended to other logic gates(i.e., OR, NAND and OR) and the results are shown in Fig. 2(c). Comparison of the impacts reveals that elevation in the temperature exacerbate the BTI impact in all gates. However, increment in the duty cycle lowers the impact in NOR gate, while causes increment in the impact on OR gate. For example, the in NOR gate at 75^{o}C and 40% duty cycle, the additional delay is 31.46%, while it reduces to 34.12% at 60% duty cycle. However, the duty cycle increment from 40% to 60% causes additional delay increment from 12.26% to 25.66%.

3.2 Power Degradation:

Power consumption in a gate comes from two parts i.e., Static power and Dynamic power. BTI impact on them can be described as:

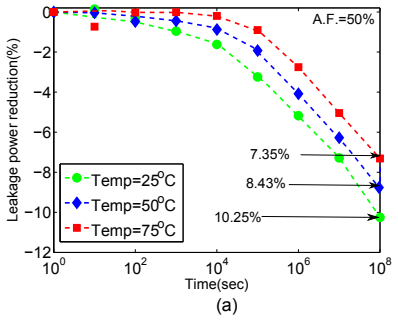
Static Power:

Static power results from leakage current that that flow when all the inputs are in state. The NOR gate is again analyzed using the framework mentioned in the previous section for static power at various temperatures and 50% duty cycles, and the results are shown in Fig. 3(a). The figure shows that static power reduction follows a trend opposite to that of the delay increment. For example, the reduction is 10.25% at 25^{o}C, however, the reduction is only 7.35% at 75^{o}C.

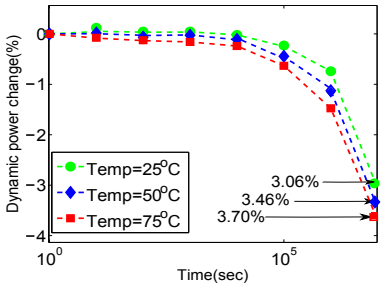
Dynamic power:

The dynamic power consumption of a gate is due to the current that flows during switching of the gate from one state to another. Results of the BTI induced dynamic power variation in a NOR gate at various temperatures and 50% duty cycle are shown in Fig. 3(b). The result shows that dynamic power also follow the reduction trend and can approach up to 3.70% lower than the reference fresh gate at 75^{o}C. However, unlike the static power, the dynamic power degradation increases with temperature. The trend can be attributed to the reduction in the saturation current of the transistors during the switching.

The analysis are extended to other logic gates that are simulated at different temperature (25^{o}C, 50^{o}C, 75^{o}C) and 50% duty cycles. Table 3 shows BTI induced static power (columns 2,4,6, and 8) reduction becomes less significant at higher temperature. However, BTI induced reduciotn in dynamic power increases with temperature elevation.



(a)



(b)

Static and dynamic power variation (%) in logic gates due to BTI

Temp	NOR		OR		NAND		AND	
	*SP	†DP	SP	DP	SP	DP	SP	DP
25	10.25	3.06	12.66	3.53	11.41	3.30	13.06	3.81
50	8.43	3.46	9.80	3.74	9.73	3.71	10.34	4.23
75	7.35	3.70	8.42	4.17	8.30	3.92	8.74	4.57

*SP= Static Power, †DP=Dynamic Power

(c)

Fig. 3 (a) Static power reduction in as a function of time (b) Dynamic power reduction in as a function of time

4 BTI and Parameter Variations Impact

This section analyzes the combined impacts of BTI and parameter variations. Initially, it analyzes impact of the variations and then combine with BTI.

4.1 Parameter Variations:

Parameter variation is a combination of temperature and process variations. These variations and their impact on a NOR gate are described as follows:

- Fig. 4(a) plot the distribution of operational temperature using Gaussian's distribution. Delay of the NOR gate is analyzed using Monte Carlo simulations for the temperature distribution and result are shown in Fig. 4(b). The figure shows that fluctuations in the delay linearly follows the temperature variation, the peak-to-peak variation in the delay is 10%, however, the mean value of variation in the delay is only 0.46% than the reference.
- The process parameters considered for the variation in the analysis include PMOS and NMOS channel lengths, and widths. Fig. 4(c) shows an example of the variations i.e., PMOS channel length variation in 45nm PTM [10] transistors. Results of Monte Carlo simulations of the NOR gate is shown Fig. 4(d). The figure shows distribution of the delay approaches 20% with variation in the process paremeters. However, unlike the temperature variation, the mean value of the delay variation is about 5%.
- To observe the combined effects of temperature and process variation, simulations are performed on the NOR gate. Results of the simulation are presented in Fig 4(e) which shows that peak-to-peak variation in the delay become approaches 20% and the mean value of delay increment is about 6%.

4.2 BTI and Parameter Variation:

The final step of the analysis is to observe the combined effects of BTI and process variation on logical gates. Fig. 4(f) shows the percentage increment in the delay of gate. Analysis of the results reveal that:

- Mean increment in the delay changes with respect to the variation free case. The figure shows that the mean increment in the delay is about 34.56%. However, in the variation free case, it is only 29.75%.
- The additional delay becomes more distributed in the presence of the parameter variation. For example, outliers in the additional delay can become as low as 19% and may approach as high as 52%. The delay distribution due to parmeters variation when analyzed in the presence of the varying duty cycles will further increase the span of the delay.

In conclusion, it can be argued that variations exacerbate BTI impacts. The variations have two fold effects, i.e., the increase the mean value and increase span of the additional gate delay.

5 Conclusion

This paper presented a simulation based analysis to address the combined impacts of BTI and parameter variations in logic gates. First, without considering the parameter variations, the results shows increment in delays and its dependency on the duty cycles and operational temperature. Second, it shows that BTI causes a reduction in the static and dynamic power consumptions of the gates. Third, it shows that without considering BTI, parameter variations has an impact on the delay of the gates. Finally, it showed that combined effects of BIT and parameter variations exacerbate the delay increments in the gates.

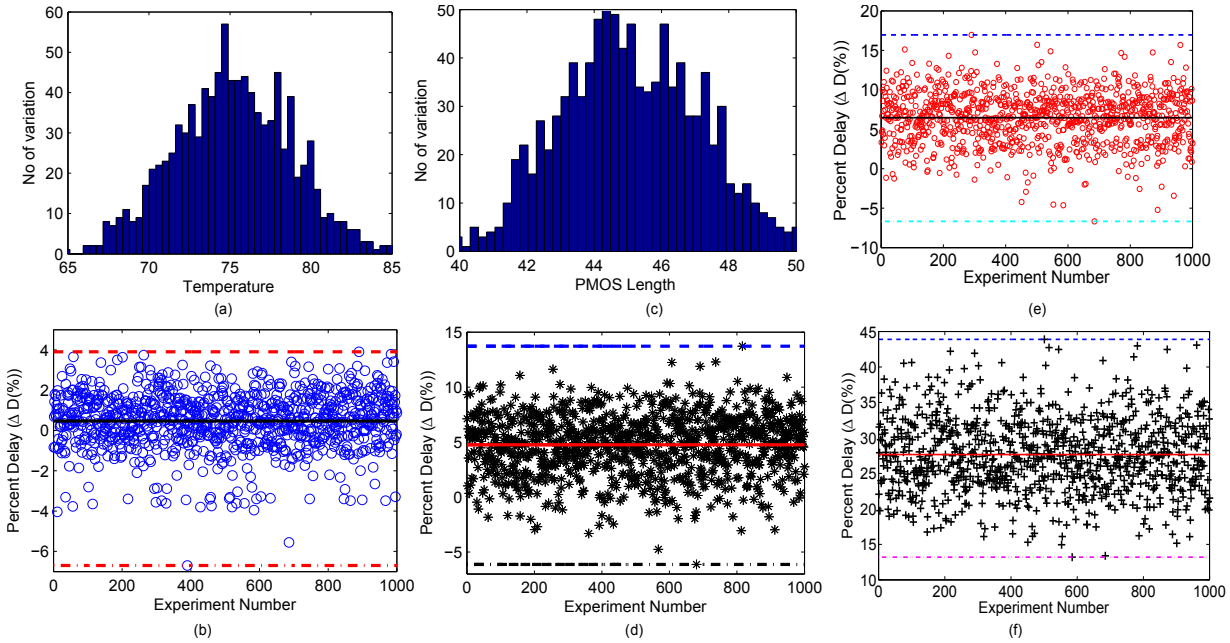


Fig. 4 (a) Variations in temperature (b) ΔD in the NOR gate under temperature variation (c) Variation in the process parameter (PMOS length) of NOR gate (c) (d) ΔD in the NOR gate under process parameter variations (e) ΔD due to temperature and process variations (f) ΔD due to BTI and parameter variations

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