

# Incorporating Parameter Variations in BTI Impact on Nano-scale Logical Gates Analysis

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**Abstract**—As semiconductor manufacturing has entered into the nanoscale era, Bias Temperature Instability (BTI) became a major threat to reliability of CMOS circuits. This threat may even be more severe in the presence of parameter variations such as temperature and process. This paper presents simulation based analysis of BTI and parameter variations in logic gates. Delay, static and dynamic power consumptions are the metrics considered in the analysis. The simulation results show that while considering BTI only, the impact on delay is strongly temperature and duty cycle dependent. For example, in a NOR gate the delay at 75°C and 50% duty cycle is 56% higher than at 25°C; and at 40% duty cycle is 67% higher than at 60%. The results also show that BTI reduced the static and dynamic power. The analysis is redone for BTI by incorporating parameter variation. Monte Carlo simulation results reveal that BTI impact is exacerbated in the presence of parameter variations with up to 15%.

**Index Terms**—: NBTI, PBTI, Complex gates, duty cycle, frequency, stress location

## I. INTRODUCTION

The unabated CMOS technology miniaturization has resulted in higher IC performance and density; however, it has caused variability and reliability issues in the scaled technologies [1]. These issues make it difficult to maintain the performance throughout the operational lifetime of the IC.

From the variability perspective, magnitudes of the parameter (process and temperature) variations are growing drastically in scaled technologies. The process variation is a consequence of the unavoidable imperfection in the MOS transistors fabrication process [3]. Similarly, temperature variation results from the changing inputs and operational conditions of the MOS transistors. On the other hand, among the reliability issues, Bias Temperature Instability (BTI) -Negative BTI (NBTI) in PMOS transistors and Positive BTI (PBTI) in NMOS transistors- has drawn attention. BTI degrades the performance of MOS transistors during “ON” states at elevated temperatures. A unique property of BTI is annealing during the transistor “OFF” state. Therefore, depending on the “ON/OFF” states, MOS transistors experience *variable* BTI impacts [2]. Both parameter variations and BTI can impact key performance parameters of a MOS transistor, such as, delay, static and dynamic powers, and effective lifetime.

Many researchers have explored the impact of BTI and/or parameter variations separately [3–8]. However, they did not consider them simultaneously, and the possible interaction

between BTI and parameter variations. For example, Paul et al., in [4] pioneered BTI analysis by performing NBTI analysis for the continuous inputs that results in the worst degradation. Kumar et al., in [5] and Khan et al., in [6] presented NBTI analysis for dynamic inputs. Rakesh et al., in [7] introduced various process and design parameters into the analysis. Similarly, Borkar et al., in [3] analyzed the impact of parameter variations on circuits. Hamid et al., in [8] analyzed delay fluctuation due to process variations. Since both BTI and parameter variations affect the threshold voltage of MOS transistors, their combined impacts may be severe; considering them in isolation could be too optimistic.

Recently, few papers have addressed combined impacts of variability and NBTI at different levels [9,10]. For instance, Kumar et al., in [9] investigated the effect in ring oscillators and SRAM cells. Siddiqua et al., in [10] explored both NBTI and process variation in an SRAM cell array and other benchmark circuits. Although the aforementioned work analyzed combined impacts of NBTI and process variations at circuit levels. They do not consider the parameter variations (both process and temperature); in addition they restrict their analysis to NBTI rather than covering both NBTI and PBTI.

This paper presents a simulation based analysis for logic gates that encompasses both parameter variations (process and temperature) and BTI (NBTI and PBTI). The main contributions of this paper are:

- Incorporate both NBTI and PBTI in simulation and analyze their impacts on gate delays. Additionally, analyze the impacts of duty cycle and temperature on BTI.
- Investigate BTI impacts on the static and dynamic power consumptions of the gates.
- Explore the impacts of parameter variations and their combined effect with the BTI at the gate level.

The rest of the paper is organized as follows: Section II presents an overview of BTI and parameter variations along with the analysis framework. Section III analyzes BTI impact on delays, static and dynamic power consumptions of the logic gates. Section IV analyzes the combined impact of BTI and parameter variations in the gates and discuss the results. Finally, Section V concludes the paper.

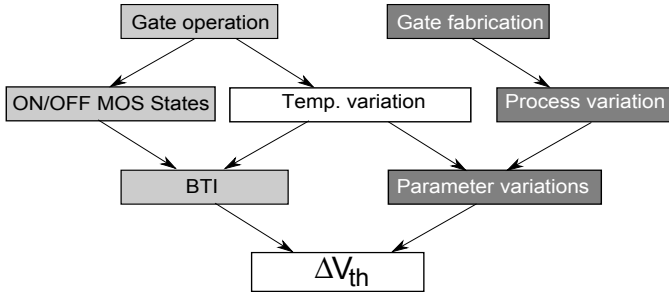


Fig. 1.  $\Delta V_{th}$  due to BTI and parameter variations

## II. BACKGROUND AND ANALYSIS FRAMEWORK

Fig. 1 shows the threshold voltage increment ( $\Delta V_{th}$ ) due to BTI, parameter variations and their interaction. The rest of this section describes BTI mechanism and parameter variations in MOS transistors in perspective of their contribution to the threshold voltage increment.

### A. BTI Mechanism

BTI degradation results from several electro-chemical processes in the MOS transistors under different stress conditions. The processes that take place in a PMOS transistor under *negative* gate stress cause NBTI, and those taking place in an NMOS transistor under *positive* gate stress cause PBTI.

During BTI, the Silicon Hydrogen bonds ( $\equiv\text{Si-H}$ ) breaking take place at the Silicon-Silicon dioxide ( $\text{Si-SiO}_2$ ) interface. The broken Silicon bonds ( $\equiv\text{Si-}$ ) trap at the  $\text{Si-SiO}_2$  interface, thus known as interface traps and the released H atoms/molecules diffuse toward the poly gate. The *number of interface traps* ( $N_{IT}$ ) depends on  $\equiv\text{Si-H}$  bond breaking rate ( $k_f$ ), H and  $\text{H}_2$  diffusion rates ( $D_H$  and  $D_{H_2}$ ), and  $\equiv\text{Si-}$  bond recovery rate ( $k_r$ ). The overall process has been described by a well-known Reaction-Diffusion (RD) model [2] as follows:

$$N_{IT}(t) = \left( \frac{k_f \cdot N_o}{k_r} \right)^{2/3} \cdot \left( \frac{k_H}{k_{H_2}} \right)^{1/3} \cdot (6 \cdot D_{H_2} \cdot t)^{1/6}, \quad (1)$$

where  $N_o$ ,  $k_H$ ,  $k_{H_2}$  and  $t$ , represent initial bond density, H to  $\text{H}_2$  conversion rate,  $\text{H}_2$  to H conversion rate inside  $\text{SiO}_2$  layer, and time, respectively. It has been argued in [2,12,13] that  $k_f$ ,  $k_H$  and  $D_H$  are temperature dependent and so is BTI. Similarly,  $N_o$  parameter depend on the process and operational temperature.

Interface traps at the  $\text{Si-SiO}_2$  interface oppose the applied gate stress resulting in the threshold voltage increment ( $\Delta V_{th}$ ) of MOS transistors. The relation between  $N_{IT}$  and  $\Delta V_{th}$  is:

$$\Delta V_{th} = (1 + m) \cdot q \cdot N_{IT} / C_{ox} \cdot \gamma \cdot \chi, \quad (2)$$

where  $m$ ,  $q$ , and  $C_{ox}$  are the holes/mobility degradation that contribute to the  $V_{th}$  increment [14], electron charge, and oxide capacitance, respectively.  $\gamma$  represents the stress duration of the transistor with respect to the total input period (i.e., *duty cycle*). Moreover,  $\chi$  is a BTI coefficient with  $\chi=1$  for NBTI and  $\chi=0.5$  for PBTI [15].

### B. Parameter variation

As shown in Fig. 1, parameter variations may be a result of either the process variation or the temperature variations. These two variations are described as follows:

#### Process variation

These are one time variations that occur during the fabrication and cause deviation of process parameters from their designated values [19]. Examples of process variations include drift in parameters such as, channel effective length ( $L_{eff}$ ), width ( $W_{eff}$ ), oxide thickness, and dopant concentration. Variations in the process parameters are usually described by some probability density functions such as, Gaussian distribution. Variation in the process parameters affect the  $V_{th}$  of the MOS transistor by the given Stolk's formula [17]:

$$\sigma_{V_{th}} = C \cdot \frac{1}{\sqrt{W_{eff} \cdot L_{eff}}}, \quad (3)$$

where  $C$  is a technology dependent constant. The above relation reveals that variations in the process parameters have complementary impacts on  $V_{th}$  of the MOS transistor.

#### Temperature variation

This is a dynamically varying parameter that reflects the changing operating conditions of the transistor. Temperature variation has widely diverse impacts on the MOS transistor. For instance, temperature increment causes  $V_{th}$  reduction that speed up the transistor. Moreover, temperature elevation causes increasing trend in the leakage current of the transistor.

Temperature dependence of the  $V_{th}$  can be extracted from the generalized analytical formulation of  $V_{th}$  as given by [18]:

$$V_{th} = C_{vt} - \frac{Q_{ss}}{C_o} + \Phi_{ms}, \quad (4)$$

where  $C_{vt}$  is a constant and  $Q_{ss}$  is the surface charge at the  $\text{Si-SiO}_2$  interface. Moreover,  $\Phi_{ms}$  is a temperature dependent  $\text{Si-SiO}_2$  work function difference and is given by [18].

$$\Phi_{ms} = -0.61 - \Phi_F(T), \quad (5)$$

$\Phi_F(T)$  is Fermi potential. The above equation shows that temperature increment reduces the work function difference and consequently lowers the  $V_{th}$ . Temperature impacts on leakage currents and power are also reported in [19].

### C. Gate Delay Model

Threshold voltage variation of the MOS transistor either due to BTI or parameter variations has its impact on the gate delay [12]. A generalized formula that relate  $V_{th}$  variations ( $\Delta V_{th}$ ) in a transistor to the gate delay is given by [4]:

$$\Delta D = \frac{n \cdot \Delta V_{th}}{(V_{gs} - V_{th})}, \quad (6)$$

where  $n$  is a constant representing the velocity saturation index of carriers in the MOS transistor channel.

#### D. Analysis Framework

The analyses presented in this paper address the impacts of both BTI and parameter variations in the gates. For this analysis, a framework shown in Fig. 2 has been developed. Stage(A) of the figure is used for degradation free simulation of the gates. For this case, the gates are synthesized using 45nm PTM transistor models and simulated using HSPICE to get a reference for analyses. Thereafter, at Stage(B) of the figure Verilog-A modules are added to each transistor to get BTI augmented gates. Depending on biasing input of each transistor, the Verilog-A module produces  $\Delta V_{th}$  that binds BTI impact to the additional gate delay ( $\Delta D$ ). Finally, variations of Stage(C) are introduced to investigate the combined impacts of BTI and parameter variations.

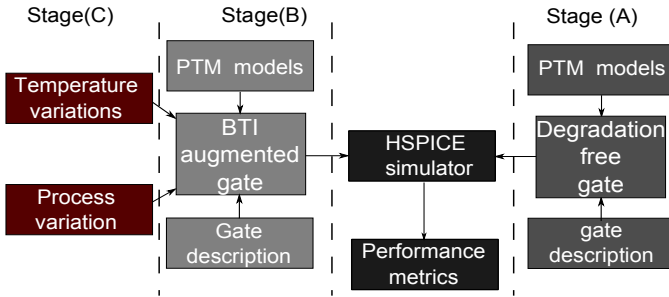


Fig. 2. Schematics of the BTI analysis framework

### III. BTI IMPACTS

This section analyzes BTI impacts in logic gates such as, NOR, OR, NAND, AND. Initially, it presents BTI impact on delay degradation of the gates. Thereafter, it investigates BTI impacts on static and dynamic powers of the gates.

#### A. Delay Degradation

Sakuri et al., in [20], argued that the gate output rise and fall transition times depend on the  $V_{th}$  of the PMOS and NMOS transistors, respectively. Since NBTI causes  $\Delta V_{th}$  to PMOS transistor, and PBTI causes  $\Delta V_{th}$  to NMOS transistors [11]. Therefore, analysis in this section considers gate rise transition times for estimating BTI impact. However, PBTI impact is augmented in the analysis and can be measured by focusing on the falling transition time of the gates.

Analyses in this paper are inspired by the observations that the duty cycle and temperature have *significant* contributions to the BTI induced delay in the gates. We argue that impact of the duty cycle on the delay is strongly gate type dependent. A given duty cycle can result in lower or higher additional in different gates. On the other hand, temperature increment results in higher BTI impacts regardless of the gate type.

Let us consider a two inputs NOR gate that is analyzed using the previously mentioned framework. The analyses are carried out at various temperature and duty cycles, and the results are shown in Fig. 3. In Fig. 3(a) BTI induced delay variation in the gate under three different temperatures is shown. The figure shows that BTI causes only 19.09% additional delay

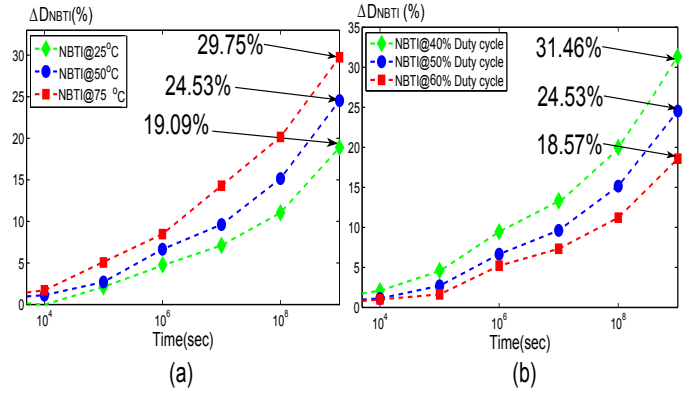


Fig. 3. (a) BTI induced delay increment in NOR gate at different temperatures as a function of time (b) BTI induced delay increment in NOR gate at different duty cycles as a function of time

to gate at 25°C. However, when the temperature increases to 75°C, BTI induced delay approaches to 29.75%. The 56% increment in BTI induced delay with the temperature elevation can be justified by  $k_f$ ,  $k_H$ , and  $D_{H_2}$  (see Eq. 1) dependence on temperature [2].

In addition to the temperature dependence, BTI induced delay dependence on duty cycle of the gate inputs is explored. Duty cycle is the percentage of a period that the inputs of gate remain high. Fig. 3(b) shows the BTI induced delay variation in a NOR gate under the three duty cycles. The figure shows that variation in the duty cycle has a significant impact on the BTI induced delays. For example, at 50% duty cycle BTI cause 24.53% additional delays to the gate. However, at 40% duty cycle, additional delay due to BTI increases to 31.46%, while the delay due to BTI becomes only 18.57% at 60% duty cycle.

The analyses are extended to other logic gates(i.e., OR, NAND and OR). It is observed that OR is synthesized from a NOR gate with a NOT gate at its output. Therefore, rising transition at the OR output results from combined PBTI impacts in NOR part and NBTI impact in NOT part. Similarly, falling transition at the OR output results from combined PBTI impacts in NOR part and NBTI impact in NOT part.

TABLE I  
BTI IMPACT (% INCREMENT) ON DELAY OF THE LOGIC GATES AT DIFFERENT TEMPERATURES AND DUTY CYCLES (D.C.)

Temp	D.C	NOR	OR	NAND	AND
25°C	40	23.88	6.04	9.88	14.57
	50	19.09	8.79	7.49	16.88
	60	14.49	12.87	6.43	21.47
50°C	40	29.51	9.98	16.07	17.32
	50	24.53	14.19	14.75	19.68
	60	23.14	18.36	12.70	28.93
75°C	40	34.12	12.26	18.58	22.77
	50	29.75	16.87	16.60	22.48
	60	24.56	25.66	15.94	30.84

The analyses are performed at different temperature (25°C, 50°C, 75°C) and duty cycles (40%, 50%, 60%). Table I shows the simulation results of the analyses. Column 2 shows BTI

impact the NOR gate and column 3 presents BTI impact in OR gate under the mentioned conditions. Comparison of the impacts reveals that elevation in the temperature exacerbate the BTI impact in both gates. However, increment in the duty cycle lowers the impact in NOR gate, while causes increment in the impact on OR gate. For example, the in NOR gate at 75°C and 40% duty cycle, the additional delay is 31.46%, while the additional delay reduces to 34.12% at 60% duty cycle. However, the duty cycle increment from 40% to 60% causes additional delay increment from 12.26% to 25.66%.

It can be concluded that impact of duty variation depend on the gate type and that temperature increment exacerbates BTI impact regardless of the gate type.

### B. Power Degradation

Power consumption in a gate comes from two parts i.e., Static power and Dynamic power. The static power consumption is a result of leakage current that occurs when all inputs hold some stable logic levels. With switching at the inputs, charging and discharging take place in the MOS capacitances that result in dynamic power consumption. The static and dynamic power consumption of NOR and OR gates are given in Table 4. The table shows that without considering BTI in the gates, the absolute values of both static and dynamic powers increase with the temperature elevation.

TABLE II  
STATIC AND DYNAMIC POWER (WATT) IN A NOR AND OR GATES  
WITHOUT CONSIDERING BTI

Temp°C	NOR		OR	
	SP	DP	SP	DP
25	13.8n	2.48μ	12.1n	4.93μ
50	16.2n	2.59μ	14.5n	5.13μ
75	18.3n	2.62μ	16.4n	5.31μ

\*SP= Static Power, +DP=Dynamic Power

#### Static Power

Static power results from leakage current that consists of various components, such as sub-threshold leakage, gate leakage, reverse-biased junction leakage, punch-through leakage, and gate-induced drain leakage. Among these sub-threshold leakage and gate leakage are dominant and they are temperature dependent. Column 2 of Table II shows the leak power in the NOR gate when the PMOS transistors are in the OFF state. The power shows an increasing trend with the temperature elevation.

The NOR gate is again analyzed using the framework mentioned in the previous section for static power. The analyses are carried out at various temperatures and 50% duty cycle, and the results are shown in Fig. 4(a). The figure shows that static power reduction follows a trend opposite to that of the delay increment. For example, the static reduction is 10.25% at 25°C, however, the reduction is only 7.35% at 75°C. *The lower reduction in static power at higher temperature can be attributed to the higher static power in the absence of BTI in the gate as shown in columns 2 and 4 of Table II.*

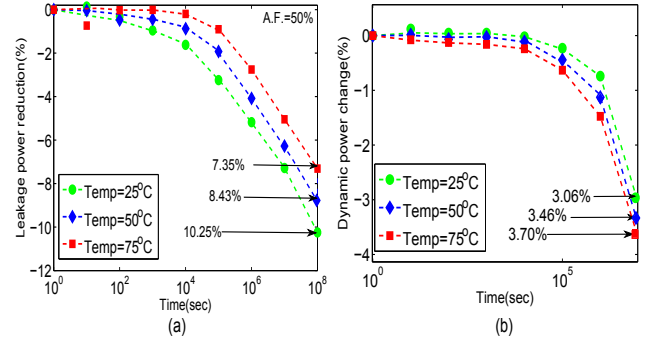


Fig. 4. (a) Static power reduction in as a function of time (b) Dynamic power reduction in as a function of time

#### Dynamic power

The dynamic power consumption of a gate is due to the current that flows during switching of the gate from one state to another. This current charges the internal nodes of the transistors and flows from the *supply* to the *ground* when the p-channel transistor and n-channel transistor turn on simultaneously during the transition.

Results of the BTI induced dynamic power variation in a NOR gate at various temperatures and 50% duty cycle are shown in Fig. 4(b). The result shows that dynamic power also follow the reduction trend and can approach up to 3.70% lower than the reference fresh gate at 75°C. However, unlike the static power, the dynamic power degradation increases with temperature. The trend can be attributed to the reduction in the saturation current of the transistors during the switching.

The analysis are extended to other logic gates that are simulated at different temperature (25°C, 50°C, 75°C) and 50% duty cycles. Table III shows BTI induced static power (columns 2,4,6, and 8) reduction becomes less significant at higher temperature. However, BTI induced reduction in dynamic power increases with temperature elevation. The impact of temperature on the dynamic power reduction is too small in our preliminary analysis. *we plan to investigate reason of the smaller temperature impact on the dynamic power and include it in the final paper.*

TABLE III  
STATIC AND DYNAMIC POWER REDUCTION (%) IN A NOR GATE

Temp	NOR		OR		NAND		AND	
	*SP	+DP	SP	DP	SP	DP	SP	DP
25	10.25	3.06	12.66	3.53	11.41	3.30	13.06	3.81
50	8.43	3.46	9.80	3.74	9.73	3.71	10.34	4.23
75	7.35	3.70	8.42	4.17	8.30	3.92	8.74	4.57

\*SP= Static Power, +DP=Dynamic Power

It can be concluded that in the absence of BTI, static power increases with the temperature elevation. Therefore, BTI induced static power will be smaller in percent but its absolute value will be higher. On the other hand, dynamic power has a weak dependence on the operational temperature.

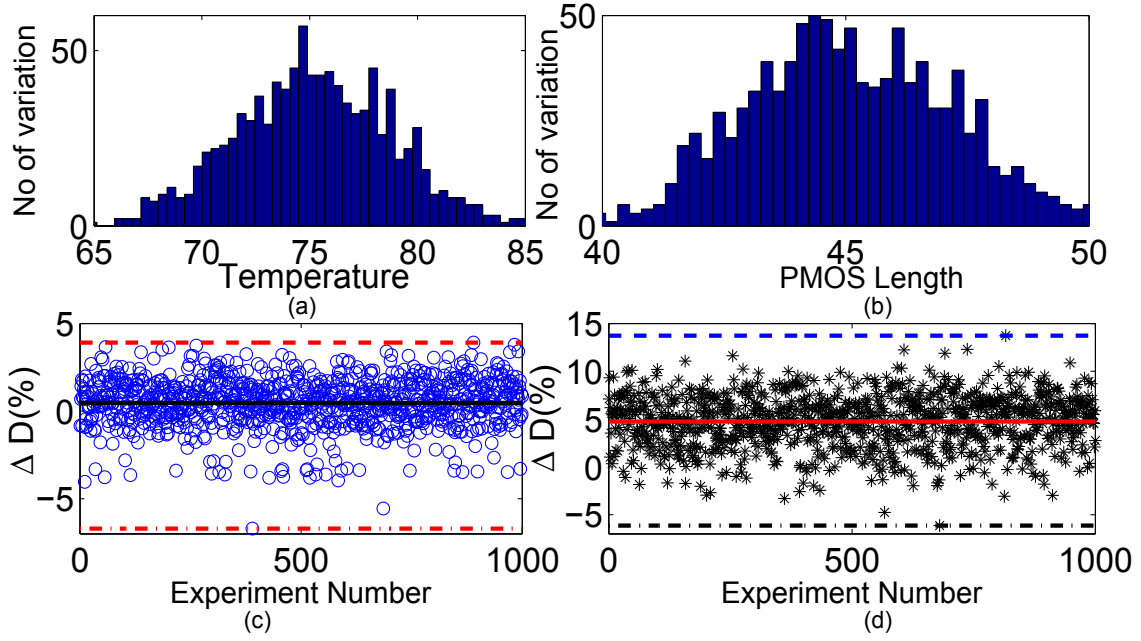


Fig. 5. (a) Variations in temperature of a gate (b) Variation in the process parameter (PMOS length) of NOR gate (c) Percent delay variation in the NOR gate under temperature variation (d) Percent delay variation in the NOR gate under process parameter variations

#### IV. BTI AND PARAMETER VARIATIONS IMPACT

This section analyzes the combined impacts of BTI and parameter variations. Initially, it analyzes impact of the variations and then combine with BTI.

##### A. Parameter Variations

Parameter variation is a combination of temperature and process variations. The spread in the temperature and process parameters represent variation in junction temperature due to variation in the gate inputs and process parameters, respectively. These variations and their impact on a NOR gate are described as follows:

- Different inputs at the gate cause variation in the junction temperature. Capturing the exact variations are strongly the workload dependent, however, Gaussian's distribution is suitable enough to for approximating the impacts. Fig. 5(a) plot the distribution of operational temperature using Gaussian's distribution. Delay of the NOR gate is analyzed using Monte Carlo simulations for the temperature distribution and result are shown in Fig. 5(c). The figure shows that fluctuations in the delay linearly follows the temperature variation, the peak-to-peak variation in the delay is 10%, however, the mean value of variation in the delay is only 0.46% than the reference.
- The imperfection in the fabrication process results in the process parameters variations. The process parameters considered for the variation in the analysis include PMOS and NMOS channel lengths, and widths. Fig. 5(b) shows an example of the variations i.e., PMOS channel length variation in 45nm PTM [22] transistors. Results of Monte

Carlo simulations of the NOR gate is shown Fig. 5(d). The figure shows distribution of the delay approaches 20% with variation in the process parameters. However, unlike the temperature variation, the mean value of the delay variation is about 5%. Francky et, al., in [21] have also reported a similar trend, however the exact physical mechanism is not understood yet.

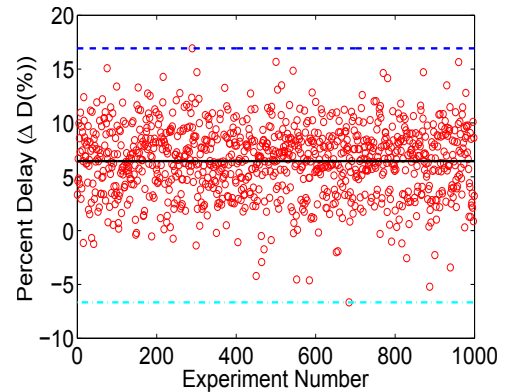


Fig. 6. Delay variation in a NOR gate under the parameters variations

- To observe the combined effects of temperature and process parameter variation, simulations are performed on the NOR gate. Results of the simulation are presented in Fig 6 which shows that peak-to-peak variation in the delay become approaches 20% and the mean value of delay increment is about 6%.



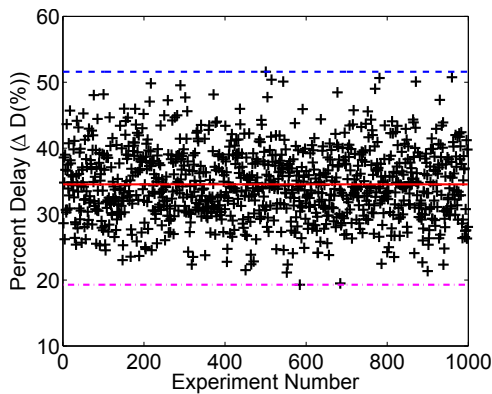


Fig. 7. (a) Percent delay variation of a NOR gate under BTI and parameter variations

Therefore, it can be concluded that variation in the process parameters have more significant impact than temperature variation.

### B. BTI and Parameter Variation

The final step of the analysis is to observe the combined effects of BTI and process variation on logical gates. Monte Carlo simulations are performed on a the reference NOR gate and can be easily extended to the other gates. Fig. 7 shows the percentage increment in the delay of gate. Analysis of the results reveal that:

- Mean increment in the delay changes with respect to the variation free case. The figure shows that the mean increment in the delay is about 34.56%. However, the delay increment in the variation free case is only 29.75%. The additional delay results from the positive interference between BTI and the variation induced delay increments.
- The additional delay becomes more distributed in the presence of the parameter variation. For example, outliers in the additional delay can become as low as 19% and may approach as high as 52%. The delay distribution due to parameters variation when analyzed in the presence of the varying duty cycles will further increase the span of the delay.

In conclusion, it can be argued that parameter variations exacerbate BTI impacts in the gates. The variations have two fold effects: (a) the increase in the mean value of the additional delay (b) the increase in the span of the additional gate delay.

## V. CONCLUSION

This paper has presented a simulation based analysis to address the combined impacts of BTI and parameter variations in logic gates. First, without considering the parameter variations, the results show an increment in delays and its dependency on the duty cycles and operational temperature. Second, the results show that BTI causes a reduction in the static and dynamic power consumptions of the gates. Third, they show that even in the absence of BTI, parameter variations has an impact on the delay of the gates. Finally, the simulation

revealed that combined effects of BIT and parameter variations exacerbate the delay increments in the gates.

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