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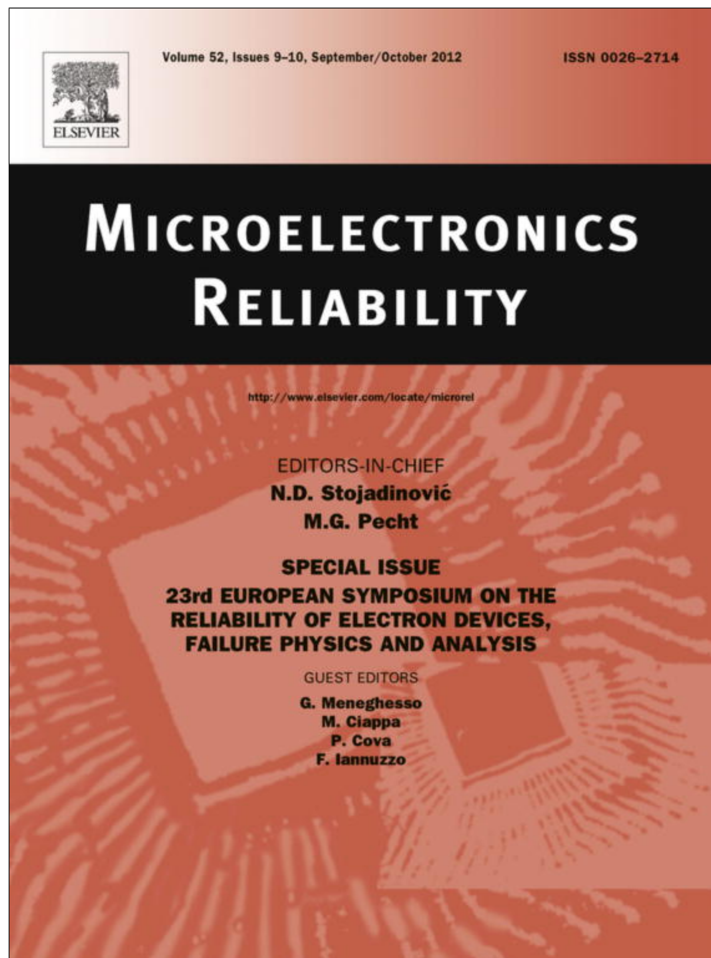

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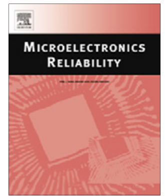

Variation tolerant on-chip degradation sensors for dynamic reliability management systems

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ABSTRACT

Aggressive technology scaling has inevitably led reliability become a key concern for modern ICs. With commonly existing Process, Voltage, and Temperature (PVT) variations inside a chip, lifetime reliability assurance becomes hardly possible without Dynamic Reliability Management (DRM). In order to maintain a chip's lifetime reliability specification, we propose a novel DRM framework in this paper, which predicts hardware aging and take the necessary actions in order to extend the system lifetime and/or prevent system failure. To collect reliability data from the circuits we introduce aging sensor circuitries able to sense transistor's threshold voltage degradation caused by NBTI/HCI stresses. Aging sensors are carefully designed under the context of severe PVT variations for current and future technologies, and simulations based on the TSMC 65 nm technology library show that a low temperature sensitivity as low as 0.29 mV/°C is achieved by our design, compared with 0.51 mV/°C for NBTI sensor and 0.325 mV/°C for HCI sensor from prior work; and a VDD variation sensitivity of 0.24 mV/mV is achieved by our design. The temperature deviation of our design is limited to 17% for extreme conditions and is about 5% at room temperature range, and the deviation of voltage is maximum 7% for extreme conditions and it is negligible at standard VDD.

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1. Introduction

With aggressive scaling of MOSFET technology for the past decades, reliability has becoming a rising concern both at design and run-time. Transistors suffer from multiple degradation mechanisms during operation, which includes Negative Bias Temperature Instability (NBTI), Hot Carrier Injection (HCI), and so on. As a result, device performance degrades and eventually devices might ceased to properly function during their expected lifetime [1]. Among all the failure mechanisms, NBTI stress on PMOS transistors have been considered to be a dominant limiting factor of device's lifetime. NBTI is prominent in PMOS devices along the entire channel when negative gate-to-source voltage is applied. It causes a positive shift in the absolute value of threshold voltage ($|V_{th}|$) with time [2], thereby resulting in a poor drive current and circuit delay degradation. Traditionally, HCI stress is considered to be less critical than NBTI stress, but with decreasing gate thickness and length, and increasing channel electrical field, HCI remains as a major reliability concern. Moreover, variations from process technology, as well as dynamic environment like supply voltage and temperature, cause a statistical degradation across circuits and chips, thus ensuring lifetime reliability for IC at design time becomes more difficult than ever. Consequently, introducing a Dynamic Reliability Management (DRM) scheme to assure IC's lifetime specifications in advanced process nodes becomes necessary.

The DRM concept was first introduced in [3], which attempted to boost performance in an acceptable reliability margin. The idea was then extended by other works like [4], which introduces task scheduling and dynamic voltage/frequency scaling (DVFS) into the DRM system. The influence of process and temperature variation in DRM is considered for the first time in the work [5]. However, most of these proposals end up with a "blind" optimization for reliability without aging information being provided. Recently, a novel DRM system with aging sensor designed to detect delay violations was proposed in [6]. The central point behind their proposal is a stability checker able to detect delay violation caused by circuit aging effects. Any instability appearing in a "guard-band" is considered to be an aging failure, and then self-adaptive procedures are taken to adjust the system's configuration. However the proposed aging sensor is built on a binary detection of timing violation in the critical path, so its efficiency and adaptivity is limited.

Given that existing DRM approaches have different limitations, especially they don't consider the non-uniform dynamic aging progress on chip, we introduce in this paper a novel DRM framework for reliability-aware applications tailored for current and future

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technologies. The proposed DRM utilize online aging sensor circuitries to measure the NBTI/HCI degradation. These on-chip aging sensors monitor threshold voltage of transistors, which is a direct indication of the aging severity in the circuit. Subsequently, the collected aging profiling data are further processed by a reliability assessment module to determine the current reliability state, which is a key information for reliability management. Furthermore, based on the same data, a reliability prediction module gives a forecast on "future" reliability state of the system, which serves as a more indicative information for reliability optimization. The major contributions of the paper can be summarized as follows.

A new DRM framework with quantitive degradation measurement is introduced, which employs new aging sensors for NBTI/HCI degradation, monitoring the V_{th} degradation caused by dynamic environmental stresses. Different than aforementioned prior works, our approach can quantitively analyze the system aging status, which gives a deeper insight on the degradation progress and eventually leads to a better optimization for reliability.

Novel NBTI and HCI sensors are proposed with good Process, Voltage, and Temperature (PVT) variation tolerance. The proposed aging sensors are the key part of the DRM system, since the reliability optimization highly rely on the accuracy of the data they provide. Though, thus far, substantial work have been done on designing different kinds of aging sensors and circuits, most of them are targeted on the characterization of failure mechanisms. On the contrary, our work focus on designing aging sensor for lifetime reliability management. To achieve a better performance and accuracy, the environmental variations are considered in our design.

Circuit simulations based on the TSMC 65 nm technology library suggests that our designs accurately capture the aging phenomenon and have low sensitivity 0.29 mV/°C to temperature and 0.24 mV/mV to voltage, respectively, when compared with 0.51 mV/°C for NBTI sensor and 0.325 mV/°C for HCI sensor from prior work [7].

2. DRM overview and aging sensor

Fig. 1 presents an overview of the aging sensor and related components in the DRM system. The proposed aging sensors measure the threshold voltage of NBTI/HCI stressed MOSFET devices and convert it into a *Delay* signal, which is further converted into the digital domain by an asynchronous counter. NBTI has a well known recovery effect [8], which partially heals the damage caused by NBTI after the stress is removed. Experiment results show that AC degradation maintains a similar time exponent as the DC degradation, however, absolute magnitude is scaled down by a constant value [9]. Since our DRM system is targeted on the long-term reliability, the fast recovery effect of NBTI is not considered in this work.

As indicated in left bottom of Fig. 1, the V_{th} sensor is the main part of the aging sensor, as it extracts the system aging information. The output of the V_{th} sensor is sent to a Voltage Controlled Delay Line (VCDL) as control signal. The VCDL generates a delayed *Pulse* signal during the measurement. The time delay added by the VCDL is proportional to the input V_{th} signal and it represents the aging status of the circuit.

The aging sensors are connected at the end of a combinational logic path in order to sample its activity and environmental stresses. In [10] an algorithm to find critical aging path was presented and can be utilized in our system as well. Note that variations are commonly existing on a chip, thus a certain number of sensors have to be embedded into the chip to capture the statistical nature of degradation, which puts severe constraints on sensor area and power consumption. On the other hand, the sensor circuitry should

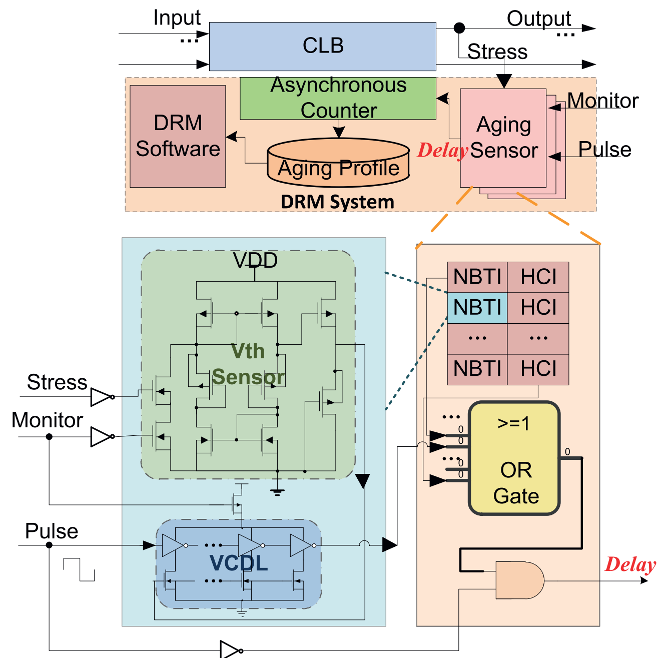

Fig. 1. Schematic of the proposed DRM system and aging sensor.

be insensitive to the environment variations to provide a precise measurement.

Fig. 2 depicts the signal waveform for the delay measurement. A *Pulse* signal triggers the VCDL in the aging sensor, and the output of the V_{th} sensor is used as VCDL control signal. The VCDL propagation delay is proportional to the V_{th} signal magnitude, which directly reflects the aging status of the logic under observation. In order to reduce the area consumption, measurements from multiple sensors are fused into one output signal using an OR gate as indicated in Fig. 1, which selects the most aged path as representative for the entire aging sensor bank inside the same logic block. The *OR* signal in Fig. 2 presents the degenerated signal for multiple sensors. This idea is based on the assumption that combinational logics inside a same Function Unit (FU) experience similar environmental conditions, like temperature activity ratio, and voltage variation, etc. This assumption is generally true based on the correlation of hardware in the same FU. Violations on this assumption could be eliminated by a careful selection of sensor's placement, i.e. on the critical paths of the FU. The degenerated *OR* signal is further *AND* with an inverted *Pulse* signal as shown by *Monitor* signal in Fig. 1. Finally, the outputted *Delay* signal is extracted and sent to an asynchronous counter and could be digitized using the system clock signal.

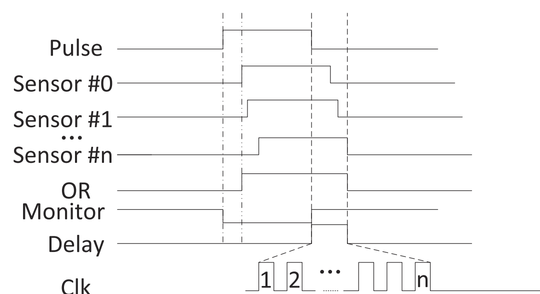

Fig. 2. Signal waveform for degenerated delay measurement of aging sensors.

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3. Circuit design of aging sensors

Fig. 3a depicts the proposed sensor circuit able to detect long-term V_{th} degradation due to NBTI, where M1 is the Device Under Test (DUT). The basic idea of this design is to integrate an V_{th} extractor circuit like [11] to detect and monitor the V_{th} from the DUT. In order to do that, transistors M9, M10, and M11 are used to control the working mode of the sensor, where *MS* is the control signal. When *MS* is set to "1" and enable signal $\overline{En}$ is set to "0" the sensor works on *Measure* mode, in which M9 is closed and M11 is open, then the stress signal through M10 is detached from the sensor and a current path through M11 is open, allowing the V_{th} extractor formed by M1–M8 to work. The absolute V_{th} value of M1 can be extracted at the "*Vout*" terminal. On the opposite, if *MS* is set to "0", sensor works on *Stress* mode, and then M11 is closed and no current can flow in the V_{th} extractor, and M1 is attached to a pull-down path controlled by the "stress" signal through M9. Since M10 is on because $\overline{En}$ is set to be "1", when $\overline{stress}$ is "1", M9 is turned on, then the gate voltage of M1 is pulled down to "0"; when $\overline{stress}$ is "0" and M9 is turned off, the input of M1 will be charged to VDD by itself. The inverted stress signal is used to expose M1 to the same aging experience as the logic path under observation.

To extract the V_{th} from M1, transistors M1, M2, M5, and M6 are connected head to tail to form a closed-loop current mirror, then the currents flow through these transistors are forced to be identically equal by the feed back loop. M3 and M4 are used to eliminate the body effect. This circuit structure has a good tolerance on PVT variations, and it is portable to different technologies, which increase the accuracy and flexibility of the sensor design.

Fig. 3b depicts an HCI sensor circuit similar with the proposed NBTI sensor above. In the HCI sensor, M1 is the DUT, and transistors M7, M8, and M9 are used to control the working mode of the sensor, where *MS* is the control signal. When *MS* is set to "0" and enable signal $\overline{En}$ is set to "1" the sensor works in measure mode, where M8 is closed and M9 is open, and the stress signal through M7 is detached from the sensor, allowing the V_{th} extractor formed by M1–M6 to work; The absolute V_{th} value of M1 can be extracted at the "*Vout*" terminal. On the opposite, if *MS* is set to "0", then M9 is closed and no current can flow in the V_{th} extractor, and M1 is attached to a pull-up path controlled by the "stress" signal through M7, so M1 degrades due to HCI stress.

4. Simulation results

To evaluate PVT-variation influence on the proposed circuits, simulations are run using the TSMC 65 nm technology library (V_{DD} = 1.2 V). Temperature variation is set to be −40 to 150 °C; and voltage variation is set to be 1.1–1.3 V, which is about 10% deviation from the standard VDD value. Process variation are simulated using a Monte-Carlo simulation in Cadence Virtuoso environment. As a comparison, we performed the same simulations for the aging sensor from work [7]. A normal V_{th} value under condition (*T* = 27 °C and *VDD* = 1.2 V) is extracted from each sensor's implementation using Cadence Virtuoso tools and these values are used as the reference baseline.

Fig. 4a presents the dependence of the V_{th} measurement to temperature variation of the aging sensors. We can observe that the output voltage of our sensors varies from about 280 mV to 350 mV as temperature increases from −40 °C to 150 °C, with a temperature sensitivity around 0.29 mV/°C. The deviation is maximum 15% for extreme conditions and about 5% at room temperature range. As comparison, the temperature sensitivity of [7] is about 0.51 mV/°C for NBTI sensor and 0.325 mV/°C for HCI sensor. The deviation of their design is up to 30% for NBTI and 40% for HCI, even the minimum deviation is about 30% for their HCI sensor and 8% for the NBTI sensor.

Fig. 4b presents the dependence of the V_{th} measurement to supply voltage variations. It shows that the output voltage of our sensors have a VDD-variation sensitivity around 0.24 mV/mV. The deviation is maximum 7% for extreme conditions and about 0% at standard VDD. As comparison, the VDD-variation sensitivity is about 0.23 mV/mV for the NBTI sensor and 0.25 mV/mV for the HCI sensor of [7]. The deviation of their design is up to 18% for NBTI and 35% for HCI, even the minimum deviation is about 30% for their HCI sensor and 8% for NBTI sensor.

Monte-Carlo simulation proves our sensors are process mismatch tolerant, as depicted in Fig. 5.

Fig. 6a and b shows the deviation of the measured threshold voltage relative to normal operating condition, i.e., *T* = 27 °C and VDD = 1.2 V, in the presence of both temperature and supply voltage variations. As one can observe in the Figures, for the extreme conditions, the deviation is about 16% for the NBTI sensor, and 17% for the HCI sensor. If we assume temperature range (10 °C, 60 °C) and ±0.05 V of VDD as being a normal variation range for daily operating environments, the worst case of error produced

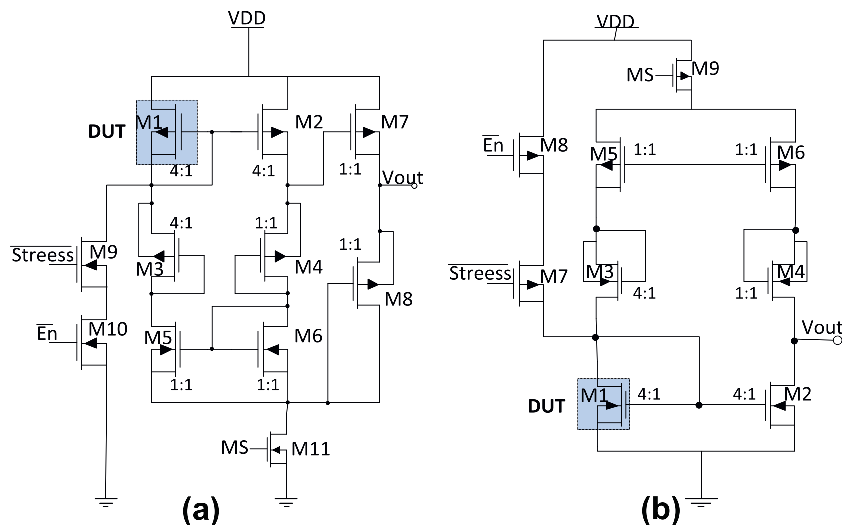

Fig. 3. Circuit schematic of aging sensors: (a) NBTI sensor. (b) HCI sensor. The size ratio of transistors for V_{th} are shown as in the figure.

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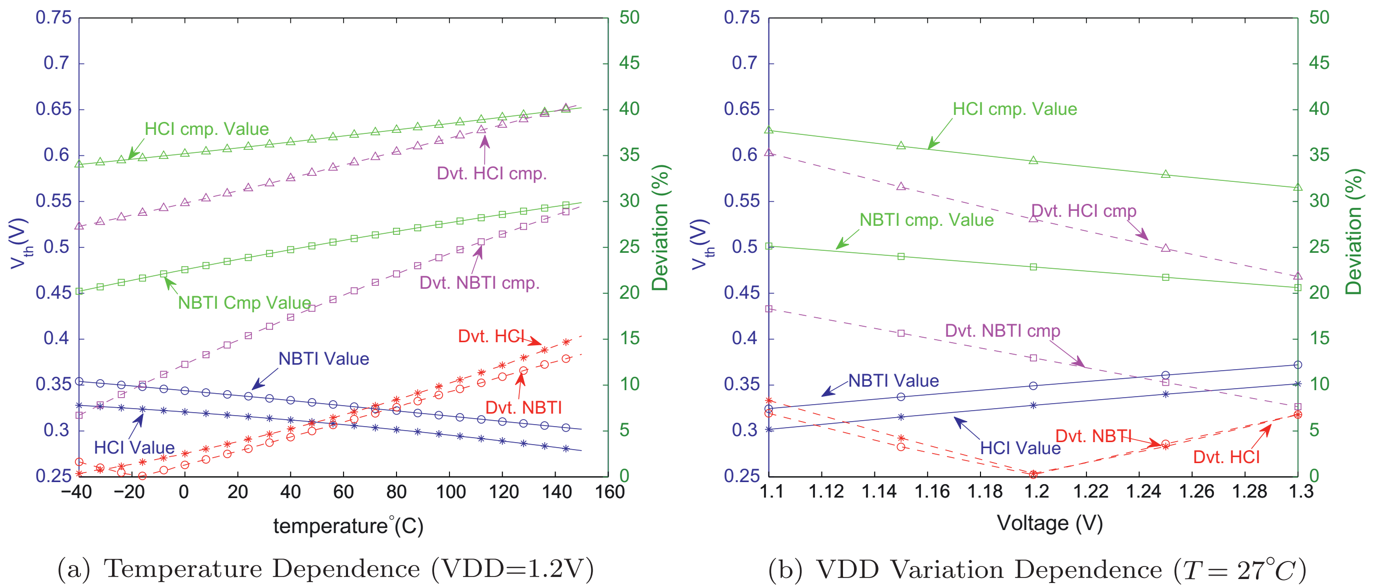

Fig. 4. Temperature and VDD variation dependence and its comparison: the left axis is the V_{th} value from the sensors, and the right axis is the absolute deviation relative to normal condition (T = 27 °C and VDD = 1.2 V); and the data with "cmp" label are for sensors from work [7].

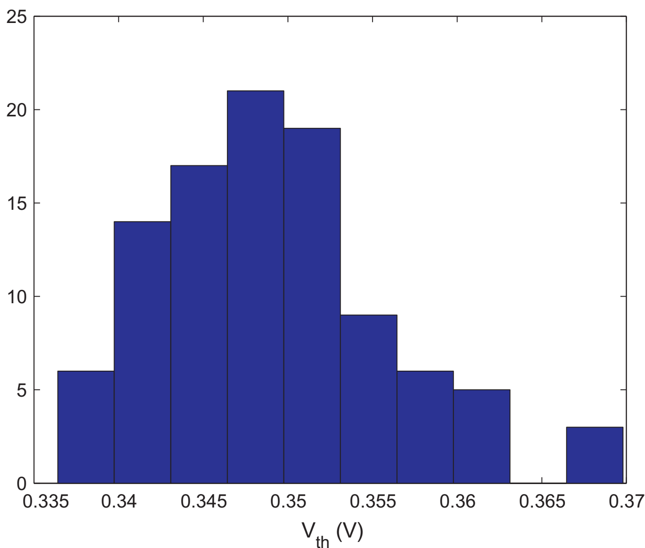

Fig. 5. Histogram plot of the output V_{th} of NBTI sensor using Monte-Carlo simulation.

by the sensor is less than 8%. Additionally, as one can deduce from the simulation results, the deviation of our designs have a good linearity in both temperature and voltage variations, which gives a simple way to calibrate the measurement online.

5. Related works and comparison

Recently, several works on aging/reliability monitoring or sensing have been reported. Srinivasan et al.'s [3] demonstrated how a DRM system can be used to boost performance in an acceptable reliability margin. Blome et al.'s [4] detailed it with specific task scheduling and DVFS technologies. Following the same design philosophy of DRM system in their works, our DRM system can be used to improve system's performance within certain reliability constraint by using DVFS and reliability-aware task scheduling technologies. With aging profiling data from on-chip aging sensors, more effective reliability management can be implemented, thus a better optimization can be achieved.

As a key part of the DRM system, the proposed aging sensors in this paper are able to collect aging/reliability information from circuits under NBTI and HCI stresses. The area overhead of our design is about 5.25 μm^2, and the power consumption is about 15.39 μW using TSMC 65 nm technology (for V_{th} Sensor only). When compared with aging sensors/monitors proposed in [12], our sensors are much more area and power efficient. Furthermore, as opposed to Karl's work [13] which requires a complicated empirical model to calibrate the ΔV_{th} to the output frequency, the relationship between V_{th} value and sensor's output of our design is simple and linear, which gives a very simple calibration scheme for our design. Most importantly, the work mentioned above is focusing on characterizing failure mechanisms, while our work is dedicated to DRM.

Agarwal et al.'s work [6,14] on a novel DRM system with aging sensors to detect delay violations is built on a binary detection of timing violation in the critical path, which limits its accuracy and adaptivity. Moreover process and dynamic variations are not considered in their design. Zhuo et al.'s work [5] considered the influence of process and temperature variation, but they use temperature and voltage sensors instead of aging sensor to make reliability assessment, which increase the overhead of area and power, and the design and calibration complexity. Different than their works, our sensors provides the DRM system with quantitive degradation measurement, which gives a deeper insight on the degradation progress and eventually leads to a better optimization for reliability.

Simulation indicate that our designs have low sensitivity 0.29 mV/°C to temperature and 0.24 mV/mV to voltage, respectively, when compared with 0.51 mV/°C for NBTI sensor and 0.325 mV/°C for HCI sensor from [7]. The temperature deviation relative to normal condition of our design is limited to 17% for extreme conditions and it is 5% at room temperature range. The voltage deviation is maximum 7% for extreme conditions and negligible at standard VDD.

To conclude, when compared with the state of the art, the proposed DRM framework and aging sensors straightly addresses the requirements of a DRM system at the expanse of relatively small

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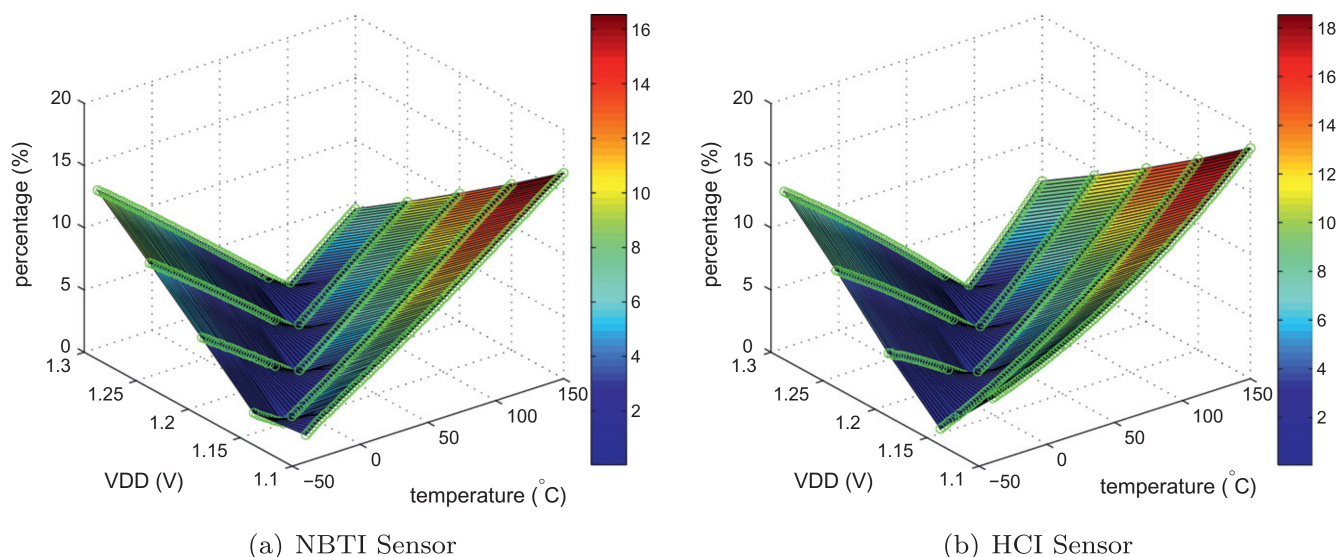

Fig. 6. V_{th} deviation relative to normal condition (T = 27 °C and VDD = 1.2 V) with temperature and voltage variations.

area overhead and low power consumption, while tolerance to process and dynamic variations is achieved.

6. Conclusion

In this paper, we propose a novel dynamic reliability management system with NBTI and HCI aging sensors. Our simulation indicate that the proposed sensors have good tolerance to dynamic variation with a sensitivity 0.29 mV/°C to temperature and 0.24 mV/mV to voltage, respectively, which outperforms the state of the art.

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