A Markovian, Variation-Aware Circuit-Level Aging Model

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***Abstract*—Accurate age modeling, and fast, yet robust reliability sign-off emerged as mandatory constraints in integrated circuits (ICs) design for advanced process technology nodes. This paper proposes a Markovian framework to asses and predict the IC lifetime by taking into account the joint effects of process, environmental, and temporal variations. By allowing the performance boundary to vary in time such that both remnant and non remnant variations are encompassed, and imposing a Markovian evolution, we propose a model that can be better fitted to various real conditions, thus enabling at design-time appropriate guardbands selection and effective aging mitigation/compensation techniques. The proposed framework has been validated for different stress conditions, under process variations and aging effects. Experimental results indicate an approximation error with mean value smaller than 10% and a standard deviation smaller than 15% for the considered circuit predicted end-of-life (EOL).**

***Index Terms*—Design-in reliability, FEOL reliability, Markovian, circuit aging.**

I. Introduction

Wear out mechanisms, further enhanced by the aggressive CMOS scaling adopted for performance improvement, have emerged as major reliability concerns of deep sub-micron devices. The time dependent drift of critical physical and electrical transistor parameters, due to manufacturing and environmental induced variations, as well as run-time aging effects, degrades the performance and eventually produces device failure. These considerations in addition with the high pressure in achieving short time-to-market figures imposed the reliability analysis to be addressed earlier in the product fabrication cycle, namely at the design time.

Most of past approaches that address the circuit-level reliability analysis focus mainly on either temporal or process variations, without considering the interactions between them. For instance, the threshold voltage V_{th}, aging-induced drift is a function of input aggression profile and environmental conditions but also depends on process parameters such as gate oxide thickness t_{ox} or initial threshold voltage V_{th0} [1]. Only recently, studies considering joint effects have been reported in the literature. In digital domain, aging-aware Statistical Timing Analysis (STA) schemes that rely on analytical expressions of circuit performance features (e.g., propagation delay, signal slope) as a function of process/wearout degradation parameters have been proposed. In [2], based on the device parameters statistical spread shifts, the circuit delay fall-out is obtained as an indicator of process variations and Negative Bias Temperature Instability (NBTI) aging effect. In [3] a Statistical Static Timing Analysis method (SSTA) is proposed in order to characterize the circuit delay distributions under process variations and NBTI effects. [4] introduces a statistical age prediction framework for a path under process variations and temporal stress. In [5] an analytical model suitable for circuit level that captures both short term NBTI and process variations effects is developed and used to quantify the impact on the circuit nominal degradation. In [6], the authors introduce the concept of virtual age that reflects the circuit cumulative aging evolution and propose a real time predicting framework for a circuit time-to-failure.

We note that previous approaches to aging models are deterministic. However, due to the very nature of the aging inducing phenomena we believe that a more appropriate, but also more complex approach should be a full probabilistic model: the age could be regarded not only as a function of the instantaneous value at time t of a degradation parameter X, for example, but also of its history (from $t = 0$ to the time moment t at which we want to compute the age):

$$A = A(t, x_1, x_2, \dots, x_n),$$

where $x_1, x_2, \dots, x_n$ are stochastic processes which enter in the expression of A by their particular realizations. As a consequence, A is also a stochastic process whose characteristics (e.g., probabilities, moments) have to be obtained from the properties of $x_1, x_2, \dots, x_n$. This is a very general formulation and for a workable model, obviously we have to impose particular restrictions.

The simplest and roughest simplification of this dependency is to express the age solely as a function of the parameter values at time moment t:

$$A = A(x_1(t), x_2(t), \dots, x_n(t)).$$

This brings us back to the point of view adopted in previous deterministic approaches, thus we do not follow this avenue.

Another simplification can be made based on the fact that we don't need all the values between 0 and t but only the values in a finite number of moments. In fact, we can further assume that only the value at time moment t, (denoted in the sequel by $x_i(t_k)$) and the one at the previous time sampling moment (denoted from now on by $x_i(t_{k-1})$) are required. $x_i(t_k)$ and $x_i(t_{k-1})$ are random variables not independent in

general, but correlated and passing from one to the other could be governed by probabilistic laws. The processes x_i could be Markovian processes and this character could be transferred to A. Moreover, the processes $x_1, x_2, \ldots, x_n$ could be correlated. In this case, if we describe (via a change of variables) the A function by the other processes $X_1, X_2, \ldots, X_n$ obtained from $x_1, x_2, \ldots, x_n$ by a linear transform of Karhunen-Loeve (KL) type [7], then our process A becomes well approximated by a small number of variables. In this manner, one can obtain a correct description of A by, e.g., a function of 4 variables $X_1(k)$, $X_2(k)$, $X_1(k-1)$, $X_2(k-1)$. In view of the above, the following remark is in order: a Markovian model fitted to the age problem must have the transition probabilities not only time dependent but also dependent of the new states. Our approach introduces a Markovian model fitted to the circuit-level aging problem. Furthermore, instead of considering the performance boundary fixed, we allow it to vary in time. In this way we obtain a more flexible model that takes into consideration that depending on stress duration, the effects on the circuit statistical parameters could be remnant or nonremnant. As a result, guardbands selection and appropriate aging mitigation/compensation techniques, better fitted to real working conditions are enabled.

In view of the previous discussion, this paper proposes a Markovian aging framework that is capable of assessing and predicting the performance degradation and lifetime of a circuit under process, environmental and aging variations. For deriving the relation between the circuit performance parameters and the drift parameters, we employ a previously proposed transistor-level aging framework [8] that accounts not only for the own transistor degradation caused by front end of line aging mechanisms but also for the influence of the aged neighboring transistors. The proposed aging assessment and prediction framework is validated by means of simulation considering both effects of process variations and lifetime dependent degradations. The simulation results quantitatively confirms that our framework can efficiently evaluate at design time the expected lifetime of a circuit under a certain stress profile.

The rest of the paper is organized as follows: Section II briefly describes the transistor-level age assessment framework. Section III extends the transistor-level aging framework to the circuit level. The circuit-level aging framework is introduced in Section IV. The simulation methodology and the obtained results are presented in Section V. The paper is concluded in Section VI with some final remarks and future work directions.

II. Transistor-Level Aging Framework

Figure 1 presents the circuit used for transistor age assessment, where P_{in} denotes the slope of the gate voltage V_{in}, P_{out} denotes the slope of the output voltage, and P_x is the slope of the surrounding current contribution I_x.

For proper transistor lifetime characterization, one should take into account not only the intrinsic self-degradation, but also the influence of the surrounding circuit topology on the transistor

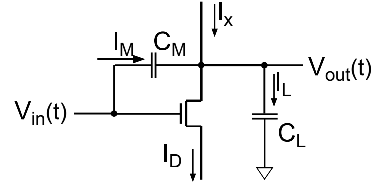

Fig. 1. Circuit schematic for transistor age assessment

in question (i.e., the influence of degraded transistors adjacent to the transistor under study). For instance, we propose to account for this influence of adjacent transistors, by means of:

- variation of gate voltage slope $\Delta dV_{in}/dt$ - the impact of aging of driver transistors,
- variation of I_x current slope $\Delta dI_x/dt$ - the impact of aging of transistors connected to the source terminal.

For the purpose of illustration, we consider as performance parameter the slope P_{out} of the output voltage. The modification of the voltage slope from device input to its output, namely: $P_\Delta = P_{in} - P_{out}$, measures the influence of the device in the degradation of the signal. We express P_Δ as being composed of two terms:

$$P_\Delta = P_{\Delta a} + P_{\Delta 0},$$

where $P_{\Delta 0}$ accounts for the inherent and initial degradation of the slope; and $P_{\Delta a}$ is the part of the degradation which increases with the device age. In principle, the term $P_{\Delta a}$ accounts for all factors which negatively impact the device performance, that is: (i) intrinsic factors - the drift of own degradation parameters $\mathbf{X}$ (e.g., V_{th}), and (ii) extrinsic factors - the variation of P_{in} and P_x slopes. More formally, $P_{\Delta a}$ can be expressed as a functional as follows:

$$P_{\Delta a} = f(\mathbf{X}(.),\, P_{in}(.),\, P_x(.)).$$

In view of the above, the age can be defined through the time integral $\int_0^t dP_{\Delta a} dt$, where $dP_{\Delta a} = dA$ are the time decrements of the slope. Once the aging increment is computed, one can proceed with the derivation of the aging rate and age expressions, i.e., the aging rate is derived by taking the ratio between the aging and time increments $\left(A_{rate} = \dfrac{dP_{\Delta a}}{dt}\right)$ and the age is given by integrating the aging increment over the interval $[0,\, t]$. In the analysis of a single transistor one can consider P_{in} = constant (i.e., the input signal is always not degraded) and in general we normalize the age such that $A = k \cdot (P_{in} - P_{out})$ arrives at the value 1 when P_{out} arrives at 0.9 of its initial value P_{out0}, for a given standard value of P_{in}. In consequence, for estimating the age of a transistor in real operating conditions we have to compute the value:

$$A = k \cdot \int_0^t (dP_{in} - dP_{out}) dt = k \cdot \int_0^t A_{rate} dt.$$

In the next section, making use of the transistor-level aging model, we propose a modality to find the location and number of monitored transistors required to determine the circuit performance degradation.

III. Circuit Performance Degradation

As embedded wear-out sensors are expensive in terms of silicon area and since a circuit may encompass thousands of paths and transistors, a reduction of the number of wear-out measurement sites is thus required for tractability purposes of circuit aging derivation.

As a reduction criterion, we employ the paths/transistors criticality in the given circuit, from a timing point of view. More precisely, we consider a reduced set of paths: the ones that could violate the timing constraints when their comprising transistors are subjected to wear-out induced degradation. Actually, only a small percentage of transistors from each such critical path is most likely to cause significant circuit performance degradation due to their aging. In the following we detail the procedure of deciding the reduced set of aging critical paths and transistors.

The aging of transistors is workload dependent; in consequence we consider several benchmarks (i.e., input aggression profiles for V_{in} and environmental conditions such as T and V_{DD}) corresponding to different degrees of computational complexity and dynamic operating conditions. In each case we determine the set of transistors that transition the most, as well as those which mostly operate without transitions (i.e., on or off). Without loss of method generality, we shall adopt the end-of-life (EOL) target of a transistor as 10% degraded output slope. With this convention in mind we eliminate from the set of transistors under analysis, all transistors with ages under half of previously defined EOL.

The paths comprising these transistors, constitute the potential reduced set of paths, that are to be subject to the aging-aware timing analysis. For illustration purposes, we propose to use as transistor-level aging monitor the propagation delay. Considering that P_{out} and P_{in} are computed at $V_{DD}/2$, we define the propagation delay of a transistor as:

$$D = \left(\frac{V_{in}}{P_{in}} - \frac{V_{out}}{P_{out}}\right) \cdot \frac{1}{2}.$$

Based on individual transistors delays, the path delay is then obtained by performing a timing analysis [9]. A further reduction of the set of paths mentioned above is possible by removing from this set, the paths with a delay that does not exceed the critical path delay.

Having decided on the reduced set of paths and transistors, we are now in position to introduce the proposed circuit-level statistical framework.

IV. Circuit Level Aging Model

In the proposed framework, we define the age of a circuit as a function of many parameters which can be divided into three main categories: (i) $\mathbf{d}$, design parameters (e.g., W), which are subject to optimizations; (ii) $\mathbf{s}$, statistical parameters (e.g., V_{th}) that fluctuate during to manufacturing process but also evolve in time depending on the dynamic operating conditions - their random behavior can only be described in probabilistic terms as random processes; and (iii) $\mathbf{r}$, range parameters (e.g., T, V_{DD}) whose variations are handled by specifying the range of values that can be attained.

In the following, the relation between the degradation parameters X_i and the performance parameter P_{out} will be given by a function f:

$$f : \mathbb{R}^n \to \mathbb{R};\ f(\mathbf{X}) = P_{out}.$$

During the lifetime of a device, its performance has to be better than an imposed value, which in our case means:

$$P_{out} > P_{out\,min}. \tag{1}$$

As P_{out} is time dependent (more precisely decreases with increasing time) through various parameters among which, some are random processes, the lifetime of the device can be expressed in probabilistic terms as:

$$R(t) = Prob\left\{P_{out}(t) > P_{out\,min}\right\}, \tag{2}$$

The device end of life is thus given by the value of t for which $P_{out}(t) = P_{out\,min}$.

Further, we adopt the usual method to achieve tractability of our problem, namely, in the case of more than one scalar statistical parameter, we apply on each of these parameters (with the restriction of having unimodal distributions) appropriate transforms to convert them into normal distributed random variables [10], while maintaining the correlation among each pair. In consequence, the statistical parameters become a normal distributed vector. In this way, we are able to compute the worst-case distance d_w, defined in [11] as the Mahalanobis distance between the mean point $\mathbf{s}_0$ and the worst case point $\mathbf{s}_w$ (i.e., the point belonging to the set of all parameters that violate a specification and is closest to the mean vector $\mathbf{s}_0$):

$$d_w^2 = (\mathbf{s}_w - \mathbf{s}_0)^T \cdot \mathbf{C}^{-1} \cdot (\mathbf{s}_w - \mathbf{s}_0), \tag{3}$$

where, as said, $\mathbf{s}$ denote the vector of statistical parameters after transforming them into Gaussian variables; $\mathbf{s_0}$ is its mean vector, and $\mathbf{C}$ is its covariance matrix, all at the same time moment. The worst case distance d_w, obtained with Equation (3) (based on the fact that the level contours are ellipsoids) is a measure of the circuit robustness. The worst case point $\mathbf{s}_w$ is found by solving:

$$\mathbf{s}_w = \text{argmin}\ (d_w^2 \mid P_{out} = P_{out\,min}).$$

As time t increases, the probabilistic properties of the statistical parameters vector, $\mathbf{s}(t)$, evolve, i.e., the mean $\mathbf{s}_0$ and the covariance matrix $\mathbf{C}$ are functions of time and the worst case distance becomes smaller. In spite of the fact that $\mathbf{s}_0$, the mean, is inside the admissible region, characterized by $P_{out} > P_{out\,min}$, the reliability with the new worst case distance attains its minimum acceptable value and the circuit reaches its end of life. This evolution is graphically caught in Figure 2.

Actually, the performance boundary defined as $P_{out}(t) = P_{out\,min}$ in the space of $\mathbf{s}$ coordinates, and being characterized by the performance function $P_{out}(\mathbf{d}, \mathbf{s}(t), \mathbf{r})$ which depends

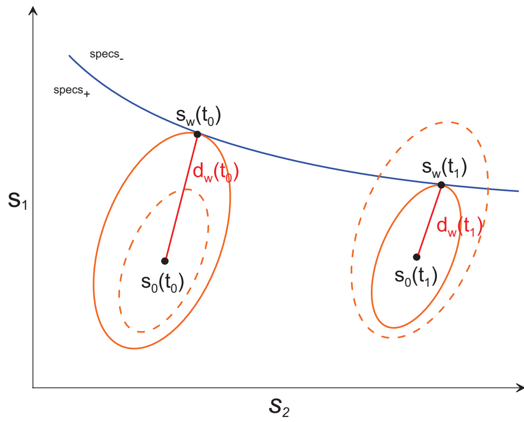

Fig. 2. Graphical representations of lifetime evolution for fixed performance boundary.

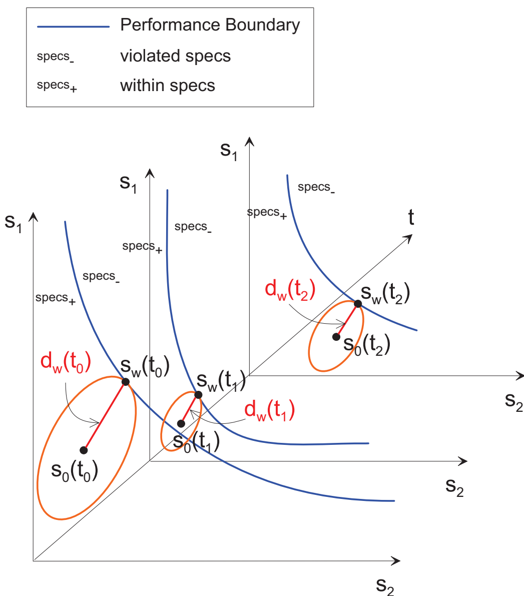

Fig. 3. Graphical representations of lifetime evolution for time varying performance boundary.

on t only via $\mathrm{s}(t)$, could be a too restrictive model for what one might encounter in real situations. For instance, if the range parameters vary in time too, this variation could have remnant - or only transient if the circuit was not exposed for a long time - influence on the physical modifications of the devices. This situation is easier described by allowing the performance boundary to vary in time, as graphically illustrated in Figure 3. Therefore, we propose to employ a space with one more coordinate - the time - and represent the evolution of the reliability ellipsoids as a tube and the evolution of the performance boundary as a surface exterior to the tube. In this way, both situations are encompassed, that is when the device degradations with T and V_{DD} variations for instance, are remnant, and when they are not remnant.

At this stage we have a model in which the performance scalar P_{out} depends on the vector of statistical parameters s, which has normal and correlated components. Therefore, an orthogonal transform (e.g., KL [7]) can be applied to decorrelate them; after this step the next simplification is to maintain only the two most important components and neglect all the others. It should be noted that these two most important components, retained, are now uncorrelated and as a consequence independent. The following step in developing a workable model is to accept a Markovian evolution and obtain the new values of the two components by applying the transition matrix to the old ones. In fact we deal with two uncorrelated Markov chains, with each component evolving separately. Both processes have a continuous space of states, $\mathbb{R}$, the set of real numbers. In consequence, the probability of a value is obtained by the Chapman-Kolmogorov equation as an integral over $\mathbb{R}$ from the conditional probabilities of that value, given each of the possible previous values:

$$p_{k+1}(y) = \int\limits_{x\in\mathbb{R}} p_k(x) \cdot p_k(y\,|x)\,\mathrm{d}x.$$

In the simplest case, i.e., a stationary Markov process, the model assumes a transition probability that is time independent, that is to say $p_k(y\,|x) = p(y|\,x)$. As previously stated, the evolution of s_1 is independent of s_2. In computing the evolution of the probability density function (pdf) of $s_1(t)$ and $s_2(t)$, we shall replace the continuous time t with a discrete set of integers k. The pdf of $s_1(k+1)$ can be obtained from the pdf of $s_1(k)$ (the same reasoning holds true for s_2) by an integral formula where the Markovian character has to be defined so as to fit the simulation results. This approach is more general than the one developed in [12] and thus can be fitted better to various real conditions.

The two independent Gaussian processes, s_1 and s_2, to which we impose a Markovian character, are therefore Wiener processes. The time evolution of their pdf-s for continuous time is described by [13]:

$$\begin{aligned} p(s_{i,0}, s_i; t)\,\mathrm{d}s_i &= Prob\,\{s_i < s_i(t) \le s_i + \mathrm{d}s_i \mid s_i(0) = s_{i,0}\} \\ &= \frac{1}{\sigma_i\sqrt{2\pi t}} \cdot \exp\left\{-\frac{(s_i - s_{i,0} - \mu_i t)^2}{2\sigma_i^2 t}\right\}\mathrm{d}s_i, \end{aligned}$$

where $i \in \{1,2\}$ and μ_i and σ_i denote the mean and the variance, respectively, of the two processes.
The boundary of the permissible domain in the $(s_1,\, s_2)$ plane is known and given by the functional relation between P_{out} and the two statistical parameters s_1 and s_2 (see Subsection II). As s_1 and s_2 are independent processes, their bi-dimensional pdf is the product of their one dimensional pdf-s. Along the time, the mean (the drift) and variance evolve as for the Wiener process and specifically, increase proportional with t. The circuit starts its life with given values $s_{1,0}$ and $s_{2,0}$ in the admissible domain; as t increases, the mean as well as the variance increase and the point $(s_1,\, s_2)$ eventually reaches the border. Actually we cannot wait until this event

happens: we have to fix the moment when the probability $Prob\{P_{out}(s_1, s_2) < P_{min}\}$ and this probability is given by the probability that (s_1, s_2) is out of the border.

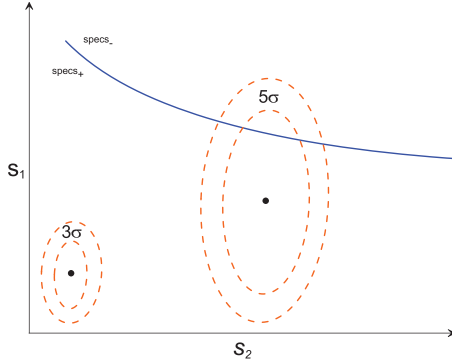

Fig. 4. 2D-pdf evolution.

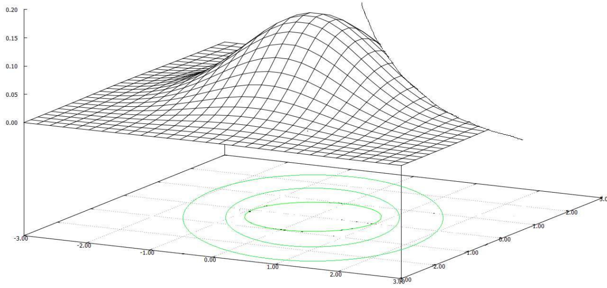

Fig. 5. 2D-pdf truncated by performance boundary.

In Figure 5 is presented a sketch of this situation in two successive moments with the 2-dim pdf of (s_1, s_2), while in Figure 4 is depicted the 2-dim pdf cut away by the performance specifications. Given the Gaussian character of our variables one can compute the probability of the domain D_{ext} (out of the performance border) for any time. For an estimation of the moment we are interested in, it is enough to have the values of:

$$Q(t) = Prob\{(s_1(t), s_2(t)) \in D_{ext}\}$$

in a finite number of moments and use a linear interpolation between them. In this way (the intersection of $Q(t)$ with the horizontal line $Q = Q_{max}$ admissible) we obtain the moment when the circuit reaches its EOL.

We stress out that using the hypotheses mentioned above we are able to bypass the difficulties of a direct Markovian model (in our model the Markovian character is included in the Wiener model for which there are classical results). The parameters of the Wiener processes have to be obtained from simulations.

When the $\mathbf{r}$ parameters are varying too, it is necessary to move the border accordingly at the same time as the pdf of (s_1, s_2) is evolving in the (s_1, s_2) space. There are two situations: either one knows their variation or only a pdf of this border (and so of the domain D_{ext}), is known. In the last case we have to compute $Q(t)$ for any position of the border - we shall index the possible positions at time t by a variable u - and to obtain the probability we look for as a weighted value of the probabilities for each D_{ext}:

$$Q(t) = \int Q(t, u) \cdot Prob\{D_{ext}(u)\}\, \mathrm{d}u.$$

It is very likely that we have only a few values of the $\mathbf{r}$ parameters, as for instance three values of V_{DD} with probabilities p_1, p_2, and p_3; for a time t. In such a case $Q(t)$ can be obtained as:

$$Q(t) = p_1 \cdot Q(t, D_{ext1}) + p_2 \cdot Q(t, D_{ext2}) + p_3 \cdot Q(t, D_{ext3}),$$

where $p_1 + p_2 + p_3 = 1$. We note inhere that this formulation does not contain the case when a variation of $\mathbf{r}$ parameters induces modifications on other parameters of the function P_{out}. In such a case, the Wiener process model parameters have to be continuously adapted during run-time.

In the following we propose a method alternative to the statistical framework for determining the circuit EOL, based on the end-of-life for the critical set transistors. Considering the application specific trade-off between prolonged usage of the circuit and dependency on known working regime, we propose to express: (i) the circuit EOL as the minimum path EOL and (ii) the path EOL as either the minimum EOL of analyzed critical transistors, or as a sum of individual transistors EOL values, weighted by workload dependent coefficients. The latter approach from (ii) is further detailed. Let us consider a critical path form aging point of view and denote by N the number of its encompassed critical transistors. The end-of-life of a path is determined as the weighted sum of its transistors EOL values $EOL_i,\ i = 1, \ldots, N$, as follows:

$$EOL_{path} = \sum_{i=1}^{N} w_i \cdot EOL_i = \sum_{i=1}^{N} EOL_i \cdot \sum_{j=1}^{4} Stress_j \cdot w_{ji}, \quad (4)$$

where:

- j denotes the state of the transistor i with the mapping: $1 \Leftrightarrow$ on, $2 \Leftrightarrow$ off, $3 \Leftrightarrow$ input transition $0 \rightarrow 1$, and $4 \Leftrightarrow$ input transition $1 \rightarrow 0$,
- the workload dependent weights $w_{ji} > 1$ are percentages from the clock period, T_{clk}, during which transistor i is on, off or transitioning, and
- the coefficients $Stress_j$ (i.e., $Stress_{on}$, $Stress_{off}$ and $Stress_{transition}$) are proportional with the power dissipation.

Finally, the following normalization is in order: $\sum w_i = 1$ in (4). In this way, the minimum EOL of the analyzed paths will directly measure the circuit end-of-life (EOL).

V. Performance Evaluation

The proposed Markovian variation-aware circuit-level aging model is verified on a $tsmc65lp$ technology, using as test

vehicle an 8-bit ripple carry adder, for which we determine the reduced set of critical paths and transistors according to the methodology described in Section III. The reliability analysis is carried by using Cadence RelXpert and Virtuoso Spectre simulators [14]. For the purpose of illustration, we employ Monte Carlo simulation loops, approach which is usually typical for analog circuits, where the analytical expressions of circuit performance features as functions of statistical parameters are not known. We choose as circuit performance feature the low to high (LH) propagation delay. As concerns the statistical parameters, we use the threshold voltage, V_{th}, the low-field mobility μ_0, the oxide thickness t_{ox}, and the oxide capacitance C_{ox}. After decorrelation, the components V_{th} and μ_0 are retained.

In Figure 6, is depicted the normalized circuit end-of-life, which is defined as the time when the propagation delay is degraded by $v\%$. For the purpose of illustration we define the EOL target for considered simulation framework as $v = 3\%$ degraded propagation delay. We consider several stress profiles (e.g., varying duty-cycle, temperature, input vectors), and obtain the corresponding performance boundary for defined EOL target in the $(\mathbf{V_{th}}, \mu_\mathbf{0})$ space, as result of reliability analysis (NBTI and HCI aging) and Monte Carlo simulation. For each profile and corresponding data set of statistical parameters, we determine $Q(t)$ in a finite number of moments, interpolate them and estimate the EOL time moment. This is compared against the accurate EOL value which is obtained by means of simulation, i.e., the time moment when $\mathbf{s} = \mathbf{s_w}$, for the obtained performance boundary. Figure 7 illustrates the EOL prediction error for varying temperature and duty cycles profiles. The prediction accuracy is quantitatively confirmed by the relatively small values of mean $(< 10\%)$ and standard deviation $(< 15\%)$ for the approximation error.

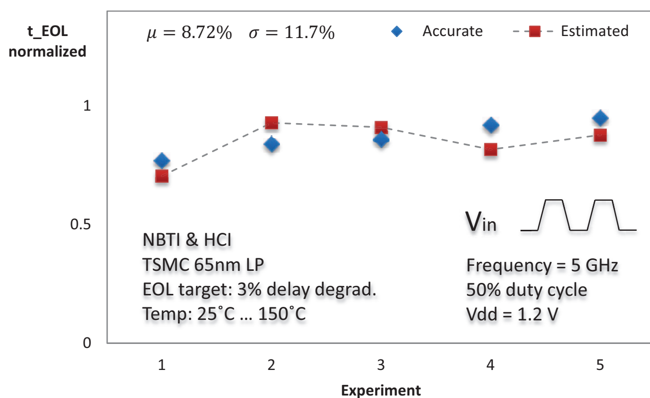

Fig. 6. Normalized accurate vs. predicted circuit EOL.

VI. Conclusions

In this paper we proposed a circuit level aging framework that adapts in time its performance boundary characterized by $P_{out}(t) = P_{out\,min}$. We noticed that, if the circuit has been stressed only for a short duration in time, the damage on the physical and electrical parameters might not be permanent.

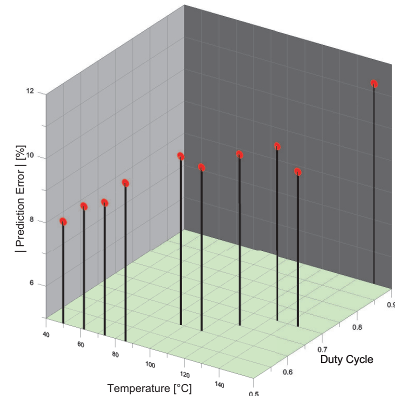

Fig. 7. Normalized EOL prediction error for varying temperature and duty cycle profiles.

This is opposed to the case when the circuit is exposed to stress conditions for a long period of time and as a consequence exhibits remnant parameters drifts. We proposed to account for these two cases by adapting the performance boundary according to the variation of statistical parameters. In this way we obtained an aging framework that is more flexible and thus better fitted to real conditions. Furthermore, since the age at time t is a functional, depending on the entire set of values taken by the degradation parameters starting from time 0 till time t, we imposed a Markovian character to our circuit level age prediction model by taking into account the history of the statistical parameters that fluctuate due to process variations and dynamic operating conditions. Experimental results indicated that the aging prediction is accurate, the approximation error having a mean value smaller than 10% and a standard deviation smaller than 15%. As a possible direction of research continuation, we mention the extension of the probabilistic model with the case when a variation of $\mathbf{r}$ parameters induces modifications on other parameters of the function P_{out}.

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