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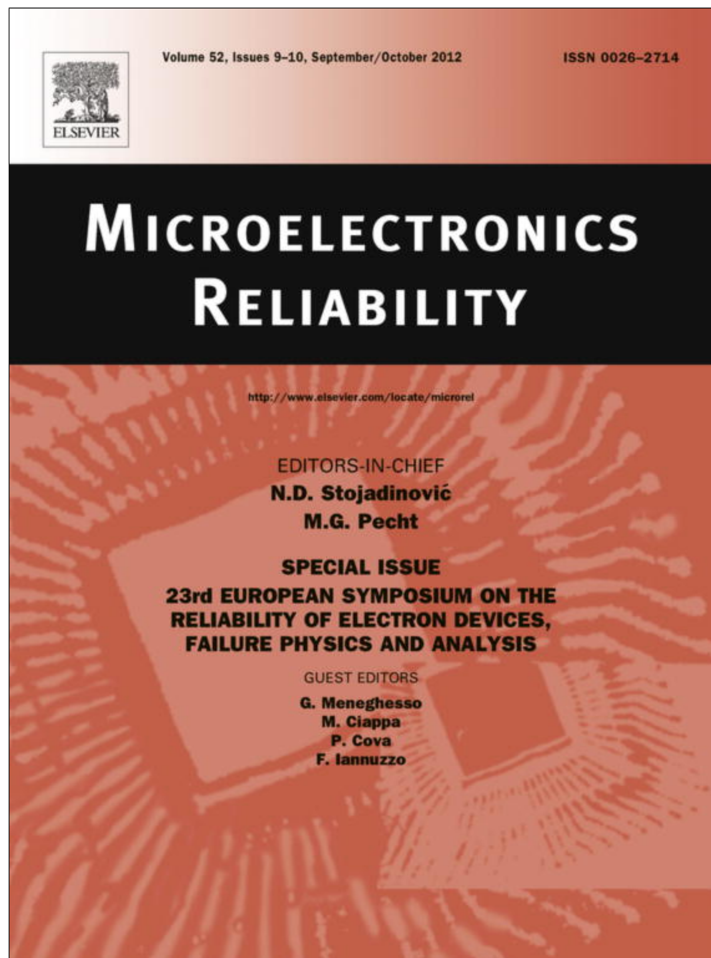

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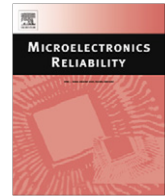

Context aware slope based transistor-level aging model

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ABSTRACT

Accurate age modeling, and fast, yet robust reliability sign-off emerged as mandatory constraints in IC design for advanced process technology nodes. This paper proposes a device-level aging assessment and prediction model using the signal slope as aging quantifier, that accounts not only for the intrinsic self-degradation but also for the influence of the surrounding circuit topology. Experimental results indicate the validity of slope as aging quantifier and that aging is underestimated when topology influence is disregarded.

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1. Introduction

Wear out mechanisms, further enhanced by the aggressive CMOS scaling adopted for performance improvement, have emerged as major reliability concerns of deep sub-micron devices. These aging phenomena lead to time dependent degradation of critical physical and electrical transistor parameters, which degrades the performance and eventually produces device failure. These considerations in addition with the high pressure in achieving short time-to-market figures imposed the reliability analysis to be addressed earlier in the product fabrication cycle, namely at the design time.

Existing approaches use delay as aging monitor [9–11] and model it as function of a parameter drift, obtained either analytically or by simulations. The delay models are commonly based on the Sakurai's α power law MOSFET model [1], to express the transistor current, which does not take into account the prevalent effects characteristic for present nanometer technologies. Moreover, most papers do not model the joint effect of multiple aging mechanisms [12–15], and very few consider the aged signal slope [2] as wearout monitor. In [3], the authors propose a delay model considering both Time Dependent Dielectric Breakdown (TDDB) and Negative Bias Temperature Instability (NBTI). In [4] an NBTI and Hot Carrier Injection (HCI) aware delay model that also provides the degradation of the output slope is introduced.

In this paper we propose a general framework for measuring the age of a device/circuit characterized by the fact that the parameter used as an aging measure is merely a functional of the aging parameters as functions of time. We propose to use as example of aging quantifier the signal slope at $V_{DD}/2$. We describe the slope based aging model analytically and validate it experimentally. The model takes into account the influences of the neighboring devices as well as own device degradation caused by Front-End-Of-Line (FEOL) aging mechanisms. Experimental results indicate that the aging prediction accuracy is improved when compared to the case when the external topology influence is disregarded.

The paper is organized as follows: In Section 2 we introduce the signal slope as aging monitor. Section 3 provides an explicit description of the transistor level aging model. The model accuracy is evaluated in Section 4. Finally, Section 5 provides a summary and comments on the main contributions and on the developments foreseen for the future.

2. Signal slope as aging monitor

The circuit employed for device age characterization is graphically depicted in Fig. 1, where V_{in} denotes the gate voltage, with slope P_{in}, V_{out} denotes the output voltage, with slope P_{out} and I_x is the surrounding environment current contribution, with slope P_x. Also, C_M and C_L are the input to output coupling capacitance and the output capacitive load, respectively. For proper transistor lifetime characterization, one should take into account not only the intrinsic self-degradation, but also the influence of topology on the transistor in question (i.e., the influence of degraded transistors adjacent to the transistor under study). We propose to account for this influence of adjacent transistors, by means of:

(i) variation of gate voltage slope $\Delta dV_{in}/dt$ – the impact of aging of driver transistors; and
(ii) variation of I_x current slope $\Delta dI_x/dt$ – the impact of aging of transistors connected to the source terminal.

The modification of the voltage slope from device input to its output, namely: $P_\Delta = P_{in} - P_{out}$, measures the influence of the device in the degradation of the signal. We express P_Δ as being composed of two terms: $P_\Delta = P_{\Delta a} + P_{\Delta 0}$, where $P_{\Delta 0}$ accounts for the inherent and initial degradation of the slope; and $P_{\Delta a}$ is the part

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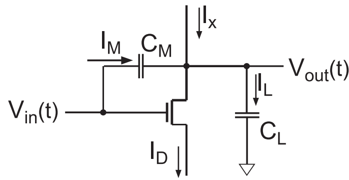

Fig. 1. Circuit schematic for transistor age assessment.

of the degradation which increases with the device age. In principle, the term $P_{\Delta a}$ accounts for all factors which impact negatively the device performance, that is:

(i) intrinsic factors – the drift of own degradation parameters **X** (e.g., V_{th}), and
(ii) extrinsic factors – the variation of P_{in} and P_x slopes.

More formally, $P_{\Delta a}$ can be expressed as a functional as follows:

$$P_{\Delta a} = f(\mathbf{X}(\cdot),\ P_{in}(\cdot),\ P_x(\cdot)).$$

In view of the above, the age can be defined through the time integral $\int_0^t dP_{\Delta a}dt$, where $dP_{\Delta a} = dA$ are the time decrements of the slope. Once the aging increment is computed, one can proceed with the derivation of the aging rate and age expressions, i.e., the aging rate is derived by taking the ratio between the aging and time increments ($A_{rate} = dP_{\Delta a}/dt$) and the age is given by integrating the aging increment over the interval $[0, t]$. In the analysis of a single transistor one can consider P_{in} = const (i.e. the input signal is always not degraded) and in general we normalize the age such that $A = k \cdot (P_{in} - P_{out})$ arrives at the value 1 when P_{out} arrives at 0.9 of its initial value P_{out0} for a given standard value of P_{in}. In consequence, for estimating the age of a transistor in real operating conditions we have to compute the value:

$$A = k \cdot \int_0^t (dP_{in} - dP_{out})dt = k \cdot \int_0^t A_{rate}dt.$$

3. Transistor aging model

The differential equation that describes the dynamic behavior of the circuit depicted in Fig. 1, is derived by applying Kirchoff current law at the output node as follows:

$$\begin{aligned} I_x &= I_D + I_L - I_M \\ I_x &= I_D + (C_L + C_M) \cdot V'_{out}(t) - C_M \cdot V'_{in}(t) \end{aligned} \tag{1}$$

We assume that the transient analysis is concerned with the behavior of the nMOS transistor, when the input voltage ramp V_{in} is rising, thus C_L is discharging.

From (1) one gets immediately:

$$I'_x(t) = I'_D(t) + (C_M + C_L) \cdot V''_{out}(t) - C_M \cdot V''_{in}(t). \tag{2}$$

Consequently, we deduce the analytical expressions of the terms involved in (2), as functions of $V_{out}(t)$ and its time derivatives. We adopt the ultra-compact I–V model from [5], which uses nine parameters to characterize the transistor behavior in superthreshold conduction. Our choice is motivated by the fact that the model is simple (linear model) and accurate (average absolute error <10% when compared to the state-of-the-art quadratic model derived by the same authors), while accounting for the prevalent physical effects encountered in current nanometer technologies. The current I_D is a function of t through V_{in} and V_{out}, so we can write:

$$I'_D(t) = \frac{\partial I_D}{\partial V_{in}(t)} \cdot V'_{in}(t) + \frac{\partial I_D}{\partial V_{out}(t)} \cdot V'_{out}(t). \tag{3}$$

Since for short-channel MOSFET devices, the carriers' velocity can saturate before the pinch-off condition is attained (L short enough so that $V_{DS\ \ sat} \ll V_{GS} - V_{TH}$), we consider the transistor operating in the saturation region at halfway of the output switching cycle ($V_{out} = V_{DD}/2$). Accordingly, we have the following expressions for the derivatives of the velocity-saturated drain current, with respect to the input and output voltages:

$$\frac{\partial I_D}{\partial V_{in}} = \beta_1 \cdot V_{out} + \beta_2; \quad \frac{\partial I_D}{\partial V_{out}} = \beta_3,$$

where the analytical expressions of β_1, β_2, and β_3 are derived in Appendix A. It follows that:

$$I'_D(t) = \beta_1 \cdot P_{in} \cdot V_{out} + \beta_3 \cdot V'_{out}(t).$$

Finally, (2) becomes:

$$\begin{aligned} &V''_{out}(t) \cdot (C_M + C_L) + V'_{out}(t) \cdot \beta_3 + V_{out}(t) \cdot P_{in} \cdot \beta_1 \\ &\quad = P_x - P_{in} \cdot \beta_2, \end{aligned} \tag{4}$$

which is a second order linear differential equation with variable coefficients. We simplify (4) by using constant values for the coefficients (the values they have when V_{out} reaches $V_{DD}/2$). This is motivated by the fact that the equation is valid for these values for the linear domain of the commutation, i.e., in the neighborhood of $V_{DD}/2$ even if not always for the entire range (from the beginning till the end of commutation process). Nevertheless, for some initial conditions like $V_{out}(0) = V_{DD}$ and $V'_{out}(0) = 0$, one can extend the approximate validity till the moment when $V_{out}(t) = V_{DD}/2$, with a small approximation error on the derivative P_{out}.

Substituting V_{out} with e^{mt} and solving (4) for m, yields two solutions:

$$m_{1,2} = \frac{-\beta_3 \pm \sqrt{\beta_3^2 - 4(C_M + C_L)[P_{in} \cdot (\beta_1 + \beta_2) - P_x]}}{2(C_M + C_L)}$$

The general solution of the differential Eq. (4) has the form:

$$V_{out}(t) = \mathscr{C}_1 \cdot e^{m_1 \cdot t} + \mathscr{C}_2 \cdot e^{m_2 \cdot t}, \tag{5}$$

where the constants $\mathscr{C}_1$ and $\mathscr{C}_2$ are obtained such that they satisfy the initial conditions corresponding to the transistor static operating regime, that is $V_{out}(0) = V_{DD}$ and $V'_{out}(0) = 0$. For usual values of the positive parameters β_1, β_2, and β_3, we may encounter the following two situations: (i) two real negative solutions, and (ii) two complex conjugated solutions (the third case with two real solutions of different signs was not encountered in practical simulations and thus it is not discussed in this paper). In the following we detail each of these two situations.

Let us consider first that (5) has two real, negative solutions (i.e., $m_1 = -m$ and $m_2 = -k \cdot m$, where $k > 1$).

By appropriate substitution of $m_{1,2}$ and $\mathscr{C}_{1,2}$ as functions of m and k, we can rewrite (5) as:

$$V_{out}(t) = V_{DD}\ \frac{k}{(k-1)} \cdot e^{-m \cdot t} - V_{DD}\ \frac{1}{(k-1)} \cdot e^{-km \cdot t}.$$

From here one can easily get the expressions for $V_{out}(1/m)$ and $V_{out}(2/m)$.

Table 1
The value of output voltage V_{out}, sampled at two different time instants ($1/m$ and $2/m$), for three different multiplicity factors k (3, 1.5, and 1.1).

k	$V_{out}(1/m)$	$V_{out}(2/m)$	$V_{out}(\tau)$
3	$1.054 \cdot \frac{V_{DD}}{2}$	$0.4036 \cdot \frac{V_{DD}}{2}$	$0.9769 \cdot \frac{V_{DD}}{2}$
1.5	$1.315 \cdot \frac{V_{DD}}{2}$	$0.6123 \cdot \frac{V_{DD}}{2}$	$0.9542 \cdot \frac{V_{DD}}{2}$
1.1	$1.435 \cdot \frac{V_{DD}}{2}$	$0.761 \cdot \frac{V_{DD}}{2}$	$0.9713 \cdot \frac{V_{DD}}{2}$

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As one can observe in Table 1, the output voltage $V_{DD}/2$ is obtained between two time instants $1/m$ and $2/m$, for all considered values of k. Since $m_2 < m_1$, the exponential $e^{m_2 t}$ decays more rapidly than the exponential $e^{m_1 t}$. In consequence, for large values of k ($k \geqslant 3$), V_{out} is dominated by the first exponential contribution, while for small values of k ($1 < k < 1.1$), V_{out} is obtained by taking the difference of the two exponentials, both with similarly high amplitude. These two cases are graphically illustrated in Fig. 2a and b.

Based on the above observations, we conclude that the value of t for which $V_{out} = V_{DD}/2$ can be determined in all cases (under the assumption of two real negative solutions $m_{1,2}$), and propose as a good enough approximation of this t, the value found by the linear interpolation of the V_{out} values at $1/m$ and $2/m$ time instants. Explicitly, the searched t can be obtained by:

$$\tau = t_{linterp} = \frac{1}{m} \cdot \left[1 + \frac{V_{out}(1/m) - V_{DD}/2}{V_{out}(1/m) - V_{out}(2/m)}\right].$$

To confirm the assertion that approximation for τ is consistent, in Table 1, column 4, we evaluate $V_{out}(\tau)$ for the three considered k values. Having τ, the slope V'_{out} at $V_{DD}/2$ becomes:

$$P_{out} = V'_{out}(\tau) = V_{DD} \cdot \frac{km}{k-1}[e^{-km\cdot\tau} - e^{-m\cdot\tau}].$$

As concerns the solution of (4) for the set of complex conjugate values of $m_1 = m_r + j \cdot m_i$ and $m_2 = m_r - j \cdot m_i$, we obtain the following expression:

$$V_{out} = V_{DD} \cdot e^{m_r \cdot t}\left[\cos(m_i \cdot t) - \frac{m_r}{m_i} \cdot \sin(m_i \cdot t)\right].$$

Once we get a formula for P_{out} in which are included aging effects like the evolution of $\mathbf{Y}$ (e.g., V_{th}, P_{in}, P_x) with age, we can use it to derive the evolution of P_{out}. The following remark is in order: as soon as all the dependencies are of the type we deduced above, we can measure the age by the slope or deduce it from the values of the degradation parameters $\mathbf{Y}$. A more correct point of view is to consider, as mentioned in Section 2, that the slope is not a function of the instantaneous values of its input variables in a functional formula. It is a function of the entire evolution of those quantities and only its increase, i.e., dP_{out} is depending on the instantaneous values of variables and so $dP_{out} = \sum \partial P_{out}/\partial Y_i$ and

$$P_{out} = \int_0^t \sum \left(\frac{\partial P_{out}}{\partial Y_i} \cdot \frac{\partial Y_i}{\partial t}\right) dt.$$

All said about P_{out} could be translated for other measures and one of interest is the delay of a pulse produced by the aging. There could be situations when the slope has very small variations while the delay can be more easily measured and thus can serve as a measure of aging too.

4. Performance evaluation

All simulations are performed in Cadence Virtuoso 6.1.5 [6], using a tsmc65lp technology. The reliability analysis is carried out using Cadence RelXpert and Virtuoso Spectre simulators. The following two modules are implemented in Verilog-A HDL: (i) the CMOS ultra-compact model from [5], with the required 9 parameters extracted for bsim4, [8] and (ii) the aging module that consists of the equations that approximate the output slope and the aging equations. For the purpose of illustration, we consider V_{th} as the degradation parameter X, whose drift is caused by NBTI and HCI aging mechanisms [7].

In order to validate our model and evaluate its aging assessment and prediction accuracy, we employ as test vehicle a CMOS 2-input NOR gate, as depicted in Fig. 3.

For model validation, we use as devices under test the PMOS transistor M_3 and the NMOS transistor M_1, both of them fresh (un-aged). The capacitance C_L is computed as the sum of drain junction capacitances and gate capacitances of fanout devices; the gate–drain capacitive coupling C_M is obtained as the sum of the gate-to-drain/source overlap capacitance and a fraction of the gate-to-channel capacitance. We apply various slew rates P_{in} and P_x and output loads such that both cases for the values of the 2 solutions of (4) are encountered. In Fig. 4, we compare for the PMOS transistor M_3 the estimated output slope at $V_{DD}/2$ using our model (red) with the one obtained from Cadence simulation (blue). By inspection of Fig. 4, we note that in spite of the rough approximation quality of (4) on the whole time domain, the slope is approximated fairly well at $V_{DD}/2$. This is quantitatively confirmed by the relatively small values of mean (<10%) and standard deviation (<5%) for the approximation error.

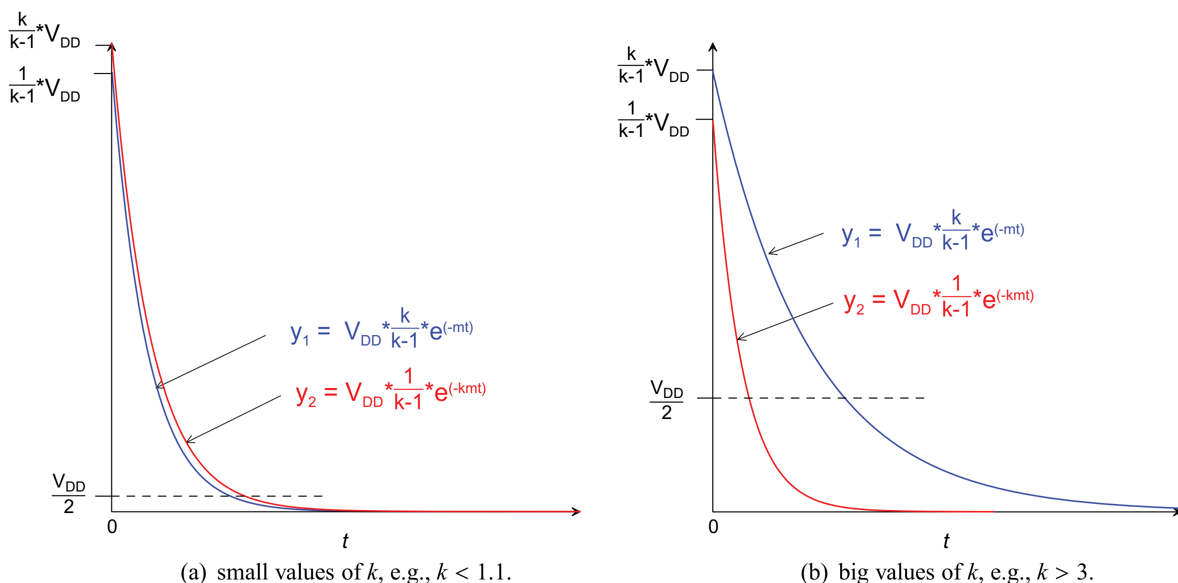

Fig. 2. Graphical interpretation of the approximation τ.

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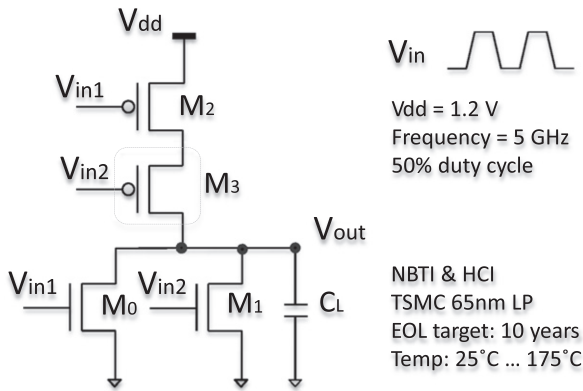

Fig. 3. Test circuit used for model validation and accuracy of aging assessment and prediction.

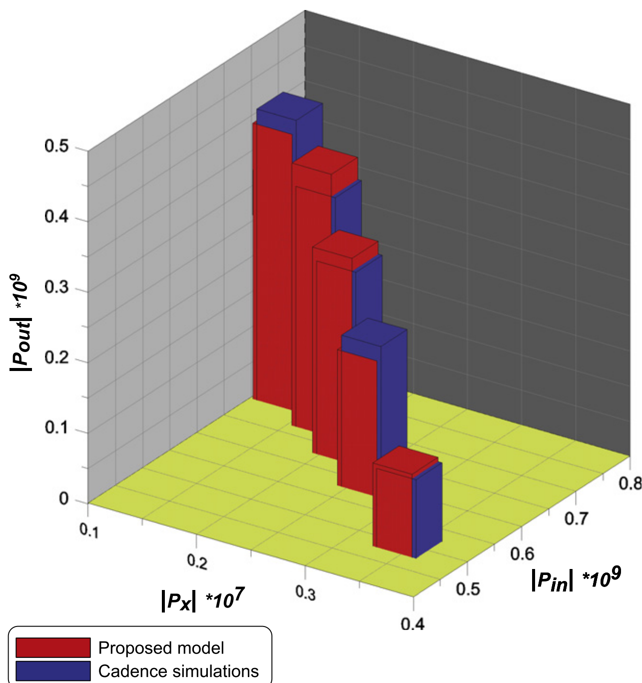

Fig. 4. Simulated vs. Estimated output voltage slope.

Commercial aging modeling and reliability analysis tools, e.g., Eldo from Mentor Graphics, RelXpert from Cadence, do not integrate the influence of neighbor degraded devices when computing the age of the current device, i.e., a transistor exhibits during its lifetime an aging rate that is the same in the case when its adjacent neighbor transistor is fresh, as well as in the case when the neighbor transistor is aged. The total electrical stress experienced by a device during its lifetime is determined by the integration of the device stress rate during a transient simulation, followed by the extrapolation of the result at a specified age, e.g., at the end of the device lifetime. The device degraded parameters drifts are then obtained as functions of the total stress. For deriving the stress rate are used accelerated lifetime models for the intrinsic FEOL mechanisms. By not taking into account the extrinsic contribution from the aged devices, may yield misleading results in terms of aging modeling and characterization.

In order to evaluate the accuracy of our slope-based aging model that accounts for both the intrinsic and extrinsic degradation, we compute M_3 transistor degradation in two cases: (i) with intrinsic and extrinsic influence factors (context-aware) and (ii) only with intrinsic influence factors. The corresponding simulation results are presented in Table 2, where $\Delta D = D_2 - D_1$, with D_1 [%] and D_2 [%] representing P_{out} degradation after 10 years for the context-aware case and for the intrinsic case, respectively. We apply several input aggression profiles typical for NBTI (static operation state) and HCI (dynamic switching periods), for a temperature range of 25–175 °C, with increments of 50 °C. We adopt the usually encountered end-of-life (EOL) target to estimate the NBTI and HCI sensitivity to the CMOS process, that is 10 years. Examining Table 2, we note that when the aging assessment is performed disregarding the influence of aging of the neighbor transistor M_2, the amount of degradation of transistor M_3 is underestimated by 4 – 7% (for the considered simulation setup) when compared to the case when both the intrinsic and the extrinsic degradation factors are taken into account.

Table 2
Aging assessment and prediction accuracy context-aware vs. intrinsic.

Aggression profiles	ΔD (%) @ M_3 after 10 years			
	25 °C	75 °C	125 °C	175 °C
$V_{in1} = 0$; $V_{in2} = V_{in}$	−4.78	−6.22	−6.63	−6.90
$V_{in1} = V_{in}$; $V_{in2} = 0$	−4.98	−5.91	−6.32	−6.67
$V_{in1} = V_{in}$; $V_{in2} = V_{in}$	−4.23	−5.56	−5.95	−6.37

5. Conclusions

The temporal degradation of transistor performance is a key limiting factor of a circuit lifetime. As a consequence, aging assessment and prediction becomes of foremost importance for reliable deep sub-micrometer CMOS devices. In this paper, we propose a transistor level aging model that takes into consideration not only the own device degradation caused by FEOL aging mechanisms such as NBTI, HCI, TDDB, but also the influence of the topology (i.e., the influence of aged neighbor transistors on the transistor whose age is being assessed). For this purpose, we define the transistor age as the time integral of the sum of output voltage slope variations caused by the aging induced drift of intrinsic/extrinsic parameters (e.g., V_{th}, P_{in}, P_x). The experimental results indicate that the slope of a transistor output voltage proves to be a reliable measure of aging that can characterize the global result of own degradation due to working regime and environmental conditions and of other devices ages which influence the correct functioning of the transistor under study. A final remark about the rational of this study is in order: there are efficient solutions to monitor the slope of the signal in a few points of a large circuit and so to monitor the circuit age; studies like ours prove that simpler models could help having a correct insight to the problem. As a possible direction of future research, we propose to extend this model towards the characterization of large circuits.

Appendix A. β Coefficients derivation

Given the expression of I_D, that is:

$$I_D = P(a \cdot V_{out} + b),$$

the following partial derivatives result:

$$\frac{\partial I_D}{\partial V_{in}} = V_{out} \cdot \underbrace{(a' \cdot P - w \cdot k_{RDS} \cdot a' \cdot a)}_{\beta_1} + \underbrace{(P \cdot b' - w \cdot k_{RDS} \cdot a' \cdot b)}_{\beta_2} = V_{out} \cdot \beta_1 + \beta_2$$

$$\frac{\partial I_D}{\partial V_{out}} = P \cdot a = \beta_3,$$

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where:

$$P = (w + k_{NWE} - w \cdot k_{RDS} \cdot a)$$

$$a = k_I \cdot k_{DIBL} \cdot \frac{(V_{in} - V_{th})^{\alpha-1}}{V_{th0}^{\alpha}} + k_I \cdot k_{CLM} \cdot \cdot \frac{(V_{in} - V_{th})^{\alpha}}{V_{th0}^{\alpha}}$$

$$a' = k_I \cdot k_{DIBL} \cdot (\alpha - 1) \cdot \frac{(V_{in} - V_{th})^{\alpha-2}}{V_{th0}^{\alpha}} + k_I \cdot k_{CLM} \cdot \cdot \alpha \cdot \frac{(V_{in} - V_{th})^{\alpha-1}}{V_{th0}^{\alpha}}$$

$$b = k_I \cdot \frac{(V_{in} - V_{th})^{\alpha}}{V_{th0}^{\alpha}} - k_I \cdot k_V \cdot k_{DIBL} \cdot \cdot \frac{(V_{in} - V_{th})^{3\alpha/2-1}}{V_{th0}^{3\alpha/2}} - k_I \cdot k_V \cdot k_{CLM} \cdot \frac{(V_{in} - V_{th})^{3\alpha/2}}{V_{th0}^{3\alpha/2}}$$

$$b' = k_I \cdot \alpha \cdot \frac{(V_{in} - V_{th})^{\alpha-1}}{V_{th0}^{\alpha}} - k_I \cdot k_V \cdot k_{DIBL} \cdot \cdot \left(\frac{3\alpha}{2} - 1\right) \cdot \frac{(V_{in} - V_{th})^{3\alpha/2-2}}{V_{th0}^{3\alpha/2}} - k_I \cdot k_V \cdot k_{CLM} \cdot \cdot \frac{3\alpha}{2} \cdot \frac{(V_{in} - V_{th})^{3\alpha/2-1}}{V_{th0}^{3\alpha/2}}$$

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