DfT Schemes for Resistive Open Defects in RRAMs

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***Abstract*—Resistive random access memory (RRAM) is one of the universal memory candidates for computer systems. Although RRAM promises many attractive advantages (e.g., huge data storage, smaller form-factor, lower power consumption, non-volatility, etc.), there are many open issues that still need to be solved, especially those related to its quality and reliability. For instance, open defects may cause RRAM cell to enter an undefined state (i.e., somewhere between logic 0 and 1), making it hard to detect during manufacturing test. As a consequence, this may lead to test escapes (quality issue) and field failures (reliability issue). This paper shows – based on defect and circuit simulation – how testing RRAM is different from testing conventional random access memories and how march test cannot guarantee higher defect coverage. The paper then motivates the need of development of special Design-for-Testability (DfT). A concept of a new DfT is then proposed. The concept is further exploited and mapped into two different DfT circuitries: (i) Short Write Time and (ii) Low Write Voltage. Both DfT schemes are implemented and simulated; the simulation results show that defects causing the RRAM cell to enter an undefined state are easily detected.**

***Keywords*—quality, reliability, memory defect, Design-for-Testability, memristor.**

I. Introduction

In recent years, several emerging memory technologies get substantial attention and are being actively investigated for future use. Promising candidates are *ferroelectric read access memory (FeRAM)*, *spin-torque transfer RAM (STTRAM)*, *phase-change RAM (PCRAM)* and *resistive RAM (RRAM)*. Table I summarizes several performance parameters of such memories and existing memory technologies [1], [2]. The table shows that all emerging memory technology candidates possess the non-volatility of flash. Moreover, they have the potential to achieve the density of DRAM and performance of SRAM. A memory with the attributes of flash, DRAM and SRAM is suitable for use as a single universal memory in computer systems [2]. From the density perspective, RRAM outperforms the other emerging memory technologies due to its simple two-terminal cell element (without access transistor). Among RRAM device technologies, memristor gains much attention from the industry because of its compatibility to CMOS fabrication technology [3]–[7].

Although RRAM promises many attractive advantages [1]–[6], there are many open issues that still need to be solved, especially those related to its quality and reliability. Research on this field is still in its infancy stage. To the best knowledge of the authors, there is very limited work on testability of

TABLE I
Memory technologies: Existing versus Emerging [1], [2]

	Existing memory technologies			
Performance parameters	SRAM	DRAM	NAND Flash	NOR Flash
Cell element[a]	6T	1T1C	1T	
Density (Gbit/cm^2)	0.17	6.67	2.47	1.23
Write time (ns)	<0.3	<0.5	10^6	10^5
Read time (ns)	<0.3	<1	<50	<10
Non-volatility	No		Yes	

	Emerging memory technologies			
Performance parameters	FeRAM	PCRAM	STTRAM	RRAM
Cell element[a]	1T1C	1T1R	1T1J	1M
Density (Gbit/cm^2)	0.14	1.48	0.13	250
Write time (ns)	10	<60	<20	<250
Read time (ns)	<45	<60	<10	<50
Non-volatility	Yes			

[a]T=transistor, C=capacitor, R=resistor, J=junction, M=memristor

RRAM. A SPICE simulation model for defect injection and circuit simulation was proposed in [9] for fault modeling; some simulation results were also reported. They reveal that depending on its value, a defect may cause conventional memory faults as those published in [11], [12], [13] or unique memory faults. The later consists of e.g., Undefined State Fault, where the state of the cell is undefined (i.e., the corresponding voltage of the cell is somewhere between *GND* and V_{dd}). The detection of these unique faults cannot be guaranteed with march-like test algorithms used for conventional memories; this is because read operations may produce random logic values. Therefore, special Design-for-Testability (DfT) schemes need to be developed.

This paper shows first – based on defect and circuit simulation – how testing RRAM is different from testing conventional random access memories and how march test cannot guarantee higher defect coverage. The paper then motivates the need of special DfT to detect unique faults in RRAMs. A concept of a new DfT is then proposed. The concept is further exploited and mapped into two different DfT circuitries: (i) *Short Write Time (SWT)* and (ii) *Low Write Voltage (LWV)*. Simulation results show that both DfT schemes can detect open defects causing the RRAM cell to enter an undefined state.

The rest of the paper is organized as follows. Section II briefly overviews RRAM structure and operations, as well as a short analysis of open defects within RRAM cell array. Section III describes the concept of the DfT scheme. Section IV discusses SWT scheme including the simulation results and circuitry. Section V presents LWV scheme. Section VI concludes the paper.

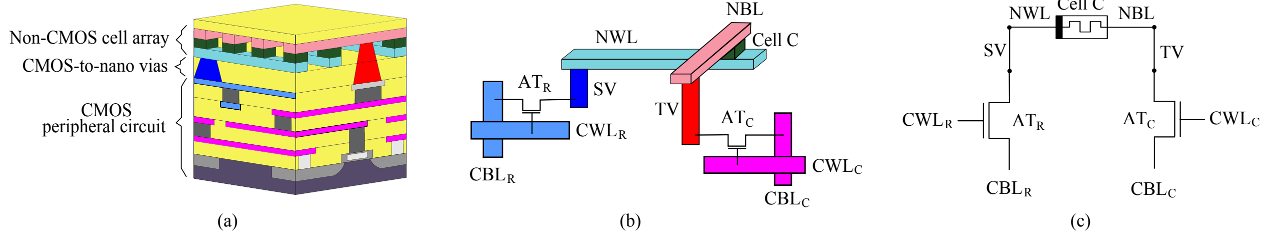

Fig. 1. (a) 3D RRAM structure (b) a single memory cell connection (c) electrical equivalent circuit

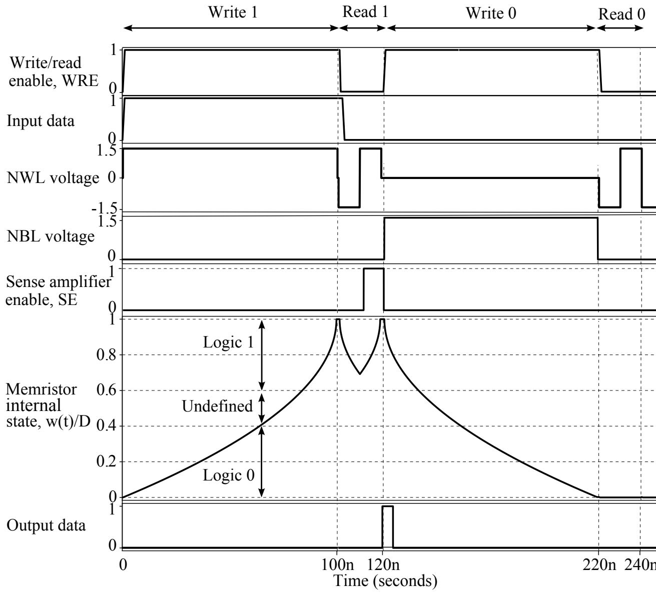

Fig. 2. Timing of control signals for RRAM operations

II. Background

This section reviews the RRAM structure, as well as its write and read operations. Thereafter, a short open defect analysis in RRAM cell array will be discussed in order to show some unique faults.

A. RRAM structure

Fig. 1(a) shows the generic structure of a three-dimensional (3D) RRAM [5]. The memory consists of three main parts: (i) non-CMOS cell array, (ii) CMOS-to-nano vias (CNVs), and (iii) CMOS peripheral circuits. The top layer is the cell array formed by two sets of parallel nanowires crossing perpendicularly with memristor sandwiched at each crosspoint; the middle layer is the CNVs made of metal (e.g., copper, tungsten); the bottom layer consists of the peripheral circuits (e.g., decoder, sense amplifier, etc.) structured from CMOS.

Fig. 1(b) illustrates the connection of a single RRAM cell *C*, which is divided into two groups: (i) the row group and (ii) the column group. The row group consists of the components connected to the lower-side terminal of cell *C*; these include nanowire word line *NWL*, short CNV *SV*, access transistor AT_R, CMOS word line CWL_R and CMOS bit line CBL_R. Conversely, the column group comprises the components connected to the upper-side terminal of cell *C*; these include nanowire bit line *NBL*, tall CNV *TV*, access transistor AT_C, CMOS word line CWL_C and CMOS bit line CBL_C. The electrical equivalent circuit of this single RRAM cell connection is shown in Fig. 1(c).

B. RRAM operations

The top five graphs of Fig. 2 depict the timing of control signals for write 1, read 1, write 0 and read 0 RRAM operations [7], [10], while the bottom two graphs show the RRAM cell internal state $\frac{w(t)}{D}$ and the output logic data value, respectively. $\frac{w(t)}{D}$ is the metric used to define the logic value hold by a RRAM cell (memristor) [4]. The logic state definition proposed in [10] is used in this paper. Logic 1 is defined for $0.6 \leq \frac{w(t)}{D} \leq 1$; whereas logic 0 is defined for $0 \leq \frac{w(t)}{D} \leq 0.4$. A safety margin $0.4 < \frac{w(t)}{D} < 0.6$ is set as undefined logic state. The RRAM operations are defined as follows (see Fig. 2):

- For write 1 operation, the *Write/read enable WRE* signal is set high for the duration of $100ns$ to initiate a write operation; at the same time, *Input data* of logic 1 sets *nanowire word line NWL* voltage to $1.5V$ and *nanowire bit line NBL* voltage to $0V$. During this period, $\frac{w(t)}{D}$ increases non-linearly (analog curve) from 0 to 1.
- For read 1 operation, the *WRE* signal is set low for the duration of $20ns$; at the same time, a voltage of $-1.5V$ is applied to *NWL* for the first $10ns$ followed by a voltage of $1.5V$ for the second $10ns$. During this period, $\frac{w(t)}{D}$ reduces from 1 to 0.64 before increases back to 1. During second read period, the *Sense amplifier enable SE* signal is activated to sense the read current. The read current is then converted to voltage, amplified and sent to output data buffer at t=$120ns$.
- For write 0 operation, *NWL* voltage is set to $0V$ and *NBL* voltage is set to $1.5V$; this causes $\frac{w(t)}{D}$ to reduce from 1 to 0 in symmetric pattern to that of write 1 operation.
- For read 0 operation, $\frac{w(t)}{D}$ remains at 0. The current is sensed, converted to voltage, amplified and sent to output data buffer at t=$240ns$.

C. Resistive open defects in memory cell array

In [9], a case study of resistive open defects within a single cell has been carried out. Open defects with different

TABLE II
OBSERVED FUNCTIONAL FAULT MODELS DUE TO OPEN DEFECTS IN MEMORY CELL ARRAY

Open defect value (Ω)	**Faulty behaviors**	**Fault models**
R_{op}>56k	The cell fails to undergo a down-transition (up-transition) when write 0 (write 1) is performed	TF_0 (TF_1)
R_{op}>10M	The cell is always stuck at logic 0 (logic 1)	SAF_0 (SAF_1)
R_{op}>21k	The cell returns an incorrect read logic value 0 while it keeps its correct logic 1	IRF_1
19k≤R_{op}≤56k	The cell is set to an undefined state by a write 0 (1) operation	USF_0 (USF_1)

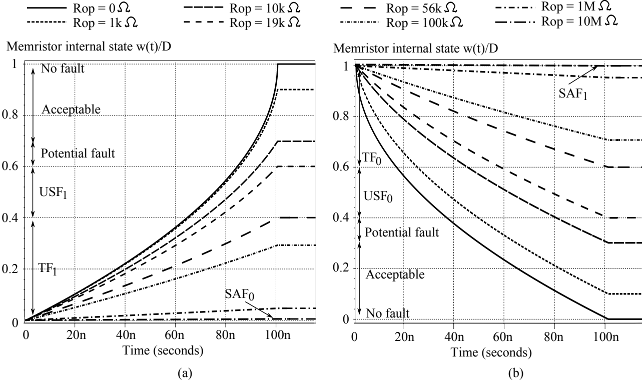

Fig. 3. Simulation results of resistive open defects within RRAM cell for (a) $0w1$ operation (b) $1w0$ operation

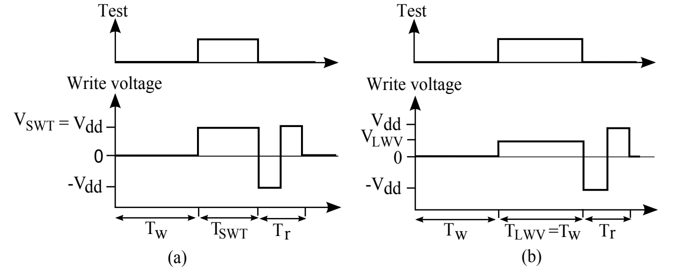

Fig. 4. Control signals for (a) SWT (c) LWV

resistance values R_{op} were injected and the memory operations $0w1$, $1w0$, $0r0$ and $1r1$ were performed; $0w1(1w0)$ denotes a write 1(0) applied to a cell which content is 0 (1), while $r1(r0)$ denotes a read operation with the expected value $1(0)$. For instance, the simulation results of $0w1$ and $1w0$ operations applied with a memory cell with an open defect in it are given in Fig. 3 (a) and (b), respectively. The figures show that the maximum (minimum) $\frac{w(t)}{D}$ value at the end of $0w1(1w0)$ operation decreases (increases) as R_{op} increases. When 19kΩ≤R_{op}≤56kΩ, the cell enters an undefined state since 0.6<$\frac{w}{D}$<0.4. When R_{op}>56kΩ, $\frac{w}{D}$≤0.4 ($\frac{w}{D}$≥0.6) meaning that the write operation fails to set the defective cell to logic 1(0).

Table II summarizes the observed faulty behaviors of the defective RRAM cell including their corresponding open resistance values and fault models. The analysis reveals that not only the traditional memory faults occur, but also new unique ones:

- Traditional fault models: these consists of e.g., *Transition Faults* (*TF_0* and *TF_1*), *Stuck at Faults* (*SAF_0 and SAF_1*) and *Incorrect Read Faults* (*IRF_1*) [11], [12], [13]. These faults *can* be detected by march tests.
- Unique fault models: these consist of e.g., *Undefined State Faults* (*USF_0* and *USF_1*). These faults *cannot* be detected by march test because the faults cause a random logic value to be read from the defective RRAM cells [9]. Therefore, a special Design-for-testability (DfT) scheme is required; this will be given next.

III. PROPOSED DFT CONCEPT

As already mentioned, open defects may cause the memory cell to enter an undefined state. Using sequence of write and read operation of march tests cannot guarantee the detection of such faults. The detection of these faults requires stressing the cell in such a way that:

- If the cell is faulty (i.e., undefined state), then stressing has to shift the state of the cell from the undefined to a wrong state. By performing a read operation after stressing the cell, the fault will be detected.
- If the cell is healthy, then it has to remains in its correct state. Otherwise, the stress may lead to overkill and yield loss.

RRAM operations rely mainly on the *duration of access time* and the *value of supply voltage* applied on *NWL* and *NBL* [4], [8], [10]. One can exploit these two properties to develop two DfT schemes; they are:

- Duration of access time: Every appropriate (normal) write operation requires a specific write access time; this is $100ns$ in Fig. 2. If now the access time is reduced, the cell will not have enough time to change its state from logic 1 (i.e., $\frac{w(t)}{D}$=1) to logic 0 (i.e., $\frac{w(t)}{D}$=0) or vice-versa; see Fig. 2. However, if the cell was already in undefined state (i.e., 0.4<$\frac{w(t)}{D}$<0.6), then applying a write operation with a reduced write time will push the cell to shift from undefined to defined state. This scheme is referred to as *Short Write Time (SWT)*; it is illustrated in Fig. 4(a). During a normal mode a write operation (say $w1$) is applied with the nominal access time T_w. Thereafter, the test mode is enabled and a write operation (say $w0$), referred to as *weak write*, with a shorter access time T_{SWT} is applied. The test mode is then set-off and a normal read operation is applied (say $r1$). If the cell suffers from open defect, then the first write $w1$ will put the cell in an undefined state and the weak write $\widehat{w}0$ will shift the state of the cell to 0. The operation $r1$ operation will return a wrong value 0 instead of 1 and the fault will

be detected. If the cell is healthy, then the weak write will not be able to change the state of the cell and the read operation will return a correct value.

- Supply voltage value: Every appropriate (normal) write operation requires a specific write voltage; this is $1.5V$ in Fig. 2. If now the voltage supply is reduced, the induced electric field will not enough to change the cell's state from logic 1 (i.e., $\frac{w(t)}{D} = 1$) to logic 0 (i.e., $\frac{w(t)}{D}$=0) or vice-versa; see Fig. 2. However, if the cell was already in undefined state (i.e., 0.4<$\frac{w(t)}{D}$<0.6), then applying a write operation with a reduced write voltage will push the cell to shift from undefined to defined state. This scheme is referred to as *Low Write Voltage (LWV)*; it is illustrated in Fig. 4(b). During a normal mode a write operation (say $w1$) is applied with the nominal supply voltage V_{dd}. Thereafter, the test mode is enabled and a write operation (say $w0$), referred to as *weak write*, with a reduced supply voltage V_{LWV} is applied. The test mode is then set-off and a normal read operation is applied (say $r1$). If the cell suffers from open defect, then the first write $w1$ will put the cell in an undefined state and the weak write $\widehat{w}0$ will shift the state of the cell to 0. The operation $r1$ operation will return a wrong value 0 instead of 1 and the fault will be detected. If the cell is healthy, then the weak write will not be able to change the state of the cell and the read operation will return a correct value.

In order to detect open defects within RRAM cells, one can apply an appropriate test algorithm while incorporating one of the above DfT schemes, as it is done in [14] for SRAMs. The following test algorithm can be applied.

1) Initialize memory cells to 0.
2) Write 1 to memory cells.
3) Activate DfT (SWT or LWV) and apply weak write 0; only defective cells will flip to 0.
4) Deactivate the DfT and read 1 from the cells. If the read value is 0, then faults are detected.
5) Initialize the cells to 1.
6) Write 0 to the cells.
7) Activate the DfT and apply weak write 1; only defective cells will flip to 1.
8) Deactivate the DfT and read 0 from the cell. If the read value is 1, then faults are detected.

A detailed description of these two DfT schemes mentioned above will be given in the next two sections.

IV. Short Write Time based DFT

As already mentioned, this scheme is based on reducing the write access time T_{SWT} while keeping the nominal supply voltage V_{dd}. Identifying the duration SWT of weak write is crucial; it has to detect faulty cells but at the same time prevent overkill. We propose the following methodology consisting of three steps.

First, set the targeted $\frac{w(t)}{D}$ boundaries of the undefined state that the DFT has to shift to a defined state. As shown in Fig. 5(a) and (b), the upper and lower boundaries are set to B_1=0.6 and B_0=0.4, respectively; this is in line with the definition of undefined state.

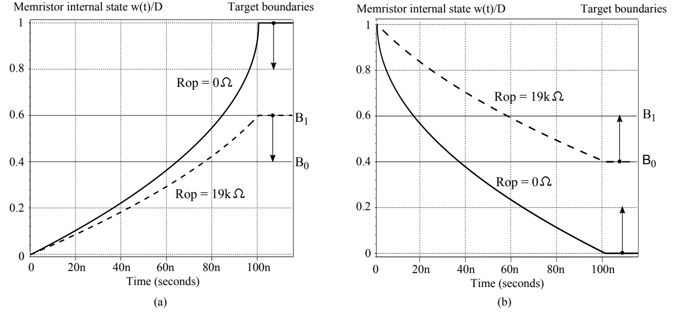

Fig. 5. Target and weak overwrite boundaries for (a) weak 0 (b) weak 1

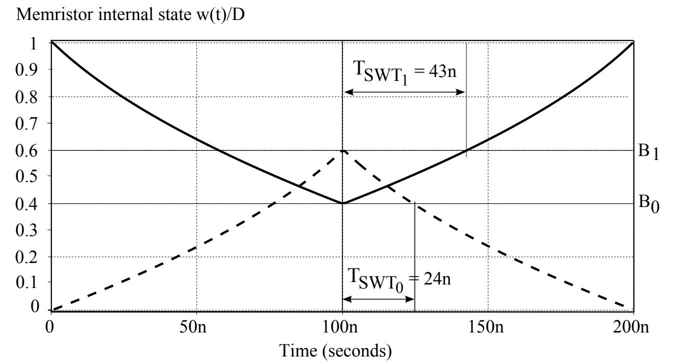

Fig. 6. Simulation result to determine T_{SWT_0} T_{SWT_1}

Second, search for the open defect R_{op} value that causes $\frac{w(t)}{D}$ to enter the targeted boundaries. A defect injection and simulation carried in [9] indicates that the open defect is $19k\Omega$ for both boundaries; see Fig. 3.

Third, search the required time for DfT scheme by performing memory operations $0w1w0$ and $1w0w1$ to the RRAM cell injected with $R_{op}19k\Omega$. Fig. 6 shows the resulting $\frac{w(t)}{D}$ curve for both operations. Analyzing the figure reveals that T_{SWT_0} at which $\frac{w(t)}{D}$ shifts from B_1 to B_0 (dashed line) is $24ns$. Likewise, the figure also shows that T_{SWT_1} at which $\frac{w(t)}{D}$ shifts from B_0 to B_1 (solid line) is $43ns$ for $1w0w1$ operations. Note that T_{SWT_0} requires shorter duration than T_{SWT_1} because the RRAM cell $\frac{w(t)}{D}$ changes quickly at larger values but slower at smaller values; i.e., larger $\frac{w(t)}{D}$ allows faster ionic drift thus higher current [4].

A. Simulation results

To evaluate the correctness of the proposed schemes, a simulation using the obtained write times T_{SWT} has been carried out. Two open resistance values are considered: (i) R_{op}=0Ω and (ii) R_{op}=19kΩ. For each injected open resistance, the test algorithm mentioned in Section III is performed.

Fig. 7 shows the result for SWT scheme that performs $0w1\widehat{w}0r1$ operations to a cell initialized with 0 and injected with the considered R_{op} values. The weak write $\widehat{w}0$ operation uses V_{SWT}=V_{dd}=$1.5V$ activated for T_{SWT_0}=$24ns$. This weak write operation causes the cell injected with R_{op}=19kΩ

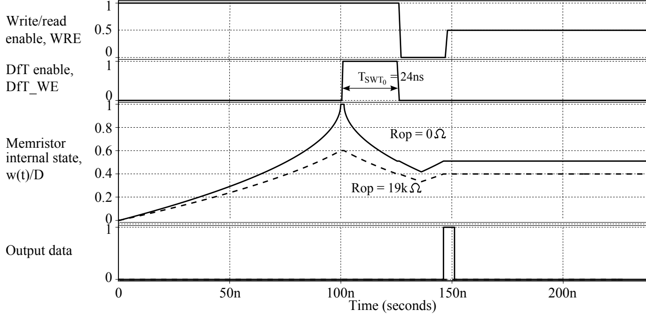

Fig. 7. Simulation results of SWT scheme for $0w1\widehat{w}0r1$ operation

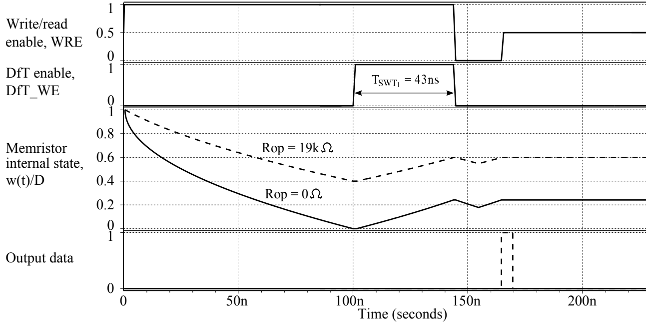

Fig. 8. Simulation results of SWT scheme for $1w0\widehat{w}1r0$ operation

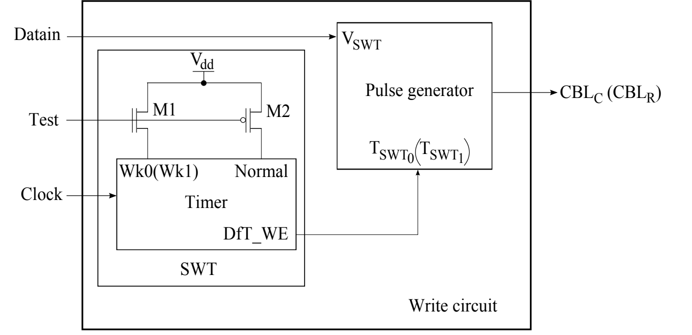

Fig. 9. Schematic of SWT circuitry

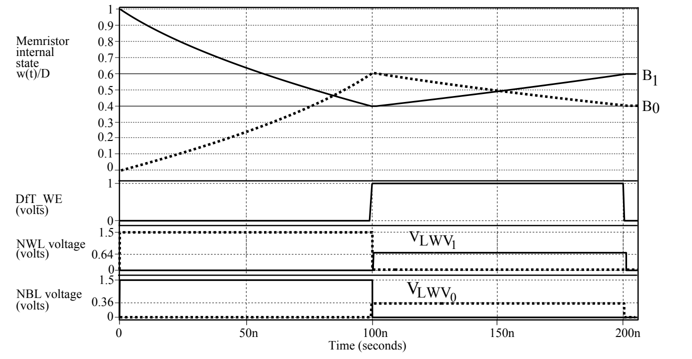

Fig. 10. Simulation result to determine V_{LWV_0} and V_{LWV_1}

to flip from the undefined logic state to logic 0. The subsequent read operation detects this defective cell, while the fault-free cell passes the test.

Fig. 8 shows the result for SWT scheme that performs $1w0\widehat{w}1r0$ operations to a cell initialized with 1 and injected with the considered R_{op} values. The weak write $\widehat{w}1$ operation uses V_{SWT}=V_{dd}=$1.5V$ activated for T_{SWT_1}=$43ns$. The simulation results show that the defective cell is detected while fault-free cell passes the test.

B. Circuitry

The SWT circuitry comprises a *Timer* that controls the duration of the write enable *DfT_WE* signal for two different write operations: weak write 0 (weak write 1) and normal write time, as shown in Fig. 9. An NMOS transistor $M1$ and PMOS transistor $M2$ are used to activate the appropriate operations. When the *Test* signal is high, $M1$ is switched on activating weak write 0 (1) operation; this in turn sets *Timer* to supply *DfT_WE*=V_{dd} for T_{SWT_0}=$24ns$ (T_{SWT_1}=$43ns$). The *DfT_WE* signal then activates *Pulse generator* to supply V_{dd} to RRAM CBL_C (CBL_R) (see Fig. 1) for the specified time period. On the contrary, when the *Test* signal is low, transistor $M2$ is switched on activating the normal write operation; this in turn sets *Timer* to supply *DfT_WE*=V_{dd} for T_{SWT}=$100ns$. Subsequently, *Pulse generator* is activated to supply V_{dd} for T_{SWT}=$100ns$.

V. Low Write Voltage based DFT

This scheme is based on reducing the supply voltage V_{LWV} while keeping the nominal write access time T_w. The same methodology for SWT is used; but the third step searches an appropriate voltage that sufficiently shifts the considered $\frac{w(t)}{D}$ boundaries instead of searching the shorter time. Each time an open defect is injected, a different V_{LWV} value is supplied to the RRAM cell under test and the memory operations $0w1w0$ and $1w0w1$ are performed. Note that the second write operation (e.g., $w0$ in $0w1w0$) uses a lower voltage than V_{dd}=1.5V supplied for T_{LWV}=$100ns$. The resulting RRAM cell internal state $\frac{w(t)}{D}$ curve is analyzed at the end of the second write operation. If the $\frac{w(t)}{D}$ if shifted to the desired boundary (B_1 or B_0), then the required write voltage has been determined; otherwise, a different write voltage is supplied. As shown in Fig. 10, to shift $\frac{w(t)}{D}$ from B_1 to B_0 after T_{LWV}=T_w=100ns, the required write voltage V_{LWV_0}=0.36V (dashed line at NBL voltage). Likewise, to shift $\frac{w(t)}{D}$ from B_0 to B_1 after T_{LWV}=100ns, V_{LWV_1}=0.64V (solid line at NWL voltage).

A. Simulation results

The same simulation setup for SWT scheme is used to simulate the LWV scheme. Fig. 11 shows the simulation results for the LWV scheme that performs $0w1\widehat{w}0r1$ operation using V_{LWV_0}=$0.36V$ activated for T_{LWV}=$100ns$. The simulation results show that the defective cell is detected and the fault-free cell is passed. The same detection capability is achieved for LWV scheme that performs $1w0\widehat{w}1r0$ operation using V_{LWV1}=$0.64V$ activated for T_{LWV}=100ns; see Fig. 12.

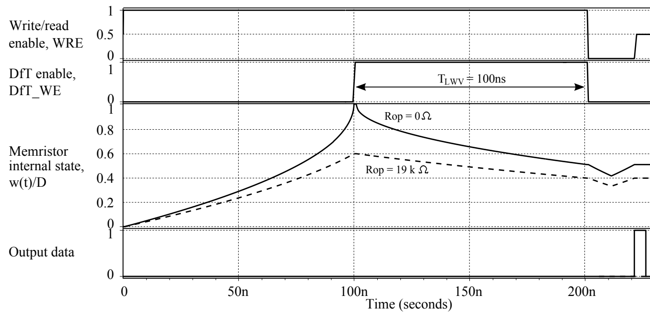

Fig. 11. Simulation results of LWV scheme for $0w1\widehat{w}0r1$ operation

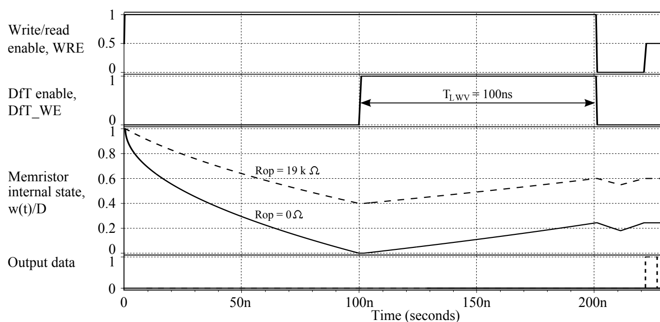

Fig. 12. Simulation results of LWV scheme for $1w0\widehat{w}1r0$ operation

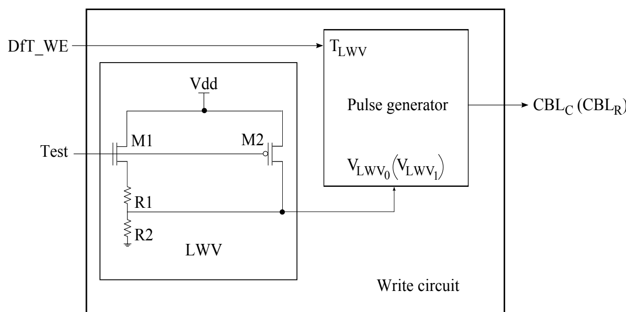

Fig. 13. Schematic of LWV circuitry

B. Circuitry

The LWV circuitry consists of components to drive two levels of voltage for two different write operations: weak write 0 (weak write 1) and normal write time, as shown in Fig. 13. The weak write operation is driven by a voltage divider circuit forming by two parallel resistors *R1* and *R2*; these resistors are connected to transistor *M1* and V_{dd}. The normal operation is driven by V_{dd} controlled by transistor *M2*. When the *Test* signal is high, transistor *M1* is switched on activating weak write 0(1) operation; this in turn supplies the *Pulse generator* with $V_{LWV}=\frac{V_{dd}\times R2}{R1+R2}$ where V_{dd} is 1.5V, $R1=1k\Omega$ and $R2=316\Omega$ (745Ω). The voltage is then supplied to the RRAM CBL_C (CBL_R); see Fig. 1. On the other hand, when the *Test* signal is low, *M2* is switched on activating normal write operation; during this period, $V_{dd}=1.5V$ is supplied to the *Pulse generator* input V_{LWV} and in turn the RRAM CBL_C (CBL_R).

VI. CONCLUSIONS

This paper presented two Design-for-Testability (DfT) schemes to detect resistive open defects in resistive random access memory (RRAM). The first DfT scheme, referred to as Short Write Time (SWT), supplies the nominal write voltage for a shorter period than the nominal write time. The second DfT scheme, referred to as Low Write Voltage (LWV), supplies a lower voltage than the nominal write voltage for the nominal time period. Simulation results show that both DfT schemes can detect the target open defects causing the RRAM cell to enter an undefined state. However, both DfT circuitries proposed in this paper only supply a fixed test stress (a shorter time or a lower voltage) once they are designed and fabricated. In production environment where process variations cannot be alleviated, open defects with various resistance values will occur. In this scenario, both DfT schemes might understress or overstress the RRAM under test leading to overkilling. Redesign can solve this problem, yet it is an iterative process resulting in extra cost and time-to-market delay. Therefore, it is vital to investigate programmable DfT schemes that can be adjusted to supply different test stress levels without requiring a redesign process; this is an ongoing study.

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