Exploring Test Opportunities for Memory and Interconnects in 3D ICs

Mottaqiallah Taouil Mihai Lefter Said Hamdioui
Delft University of Technology
Faculty of EE, Mathematics and CS
Mekelweg 4, 2628 CD Delft, The Netherlands
{M.Taouil, M.Lefter, S.Hamdioui}@tudelft.nl

***Abstract*— 3D-Stacked IC (3D-SIC) based on Through-Silicon-Vias (TSV) is an emerging technology that provides many benefits such as low power, high bandwidth 3D memories and heterogeneous integration. One of the attractive applications making used of such benefits is the stacking of memory dies on logic. System integrators for such application have to provide appropriate test strategy. However, they have to deal with block box IPs as IP providers usually refuse to share the IP content. Moreover, they dislike including JTAG in memory dies. Therefore, developing a low cost and high quality test approaches, while taking these constraints into consideration, is of great importance. This paper presents a framework of interconnect test approaches for memories stacked on logic, and look further than the only proposed JTAG solutions. The benefits and drawbacks of each possible solution is extensively discusses for stacked memories both with and without MBISTs, placed on the memory dies or on a separate logic die.**

Keywords: *iBIST, 3D Stacked IC, 3D Memory, Boundary Scan, Through-Silicon-Via*

I. INTRODUCTION

The popularity of 3D Stacked ICs (3D-SICs) is rising among industry and research institutes [1–4]. 3D-SICs are emerging as one of the main competitors to continue the trend of Moore's Law. Currently, a number of methods have been proposed to implement the interconnection of stacked dies. One of the most promising and perhaps the most reliable way to achieve this is with *Through Silicon Vias (TSVs)* [3]. TSVs are holes going through the chip silicon substrate filled with a conducting material. They enable short interconnections in 3D-SICs. Stacking dies using vertical interconnects have many benefits [4], including:

- Low latency interconnects between adjacent dies.
- Reduced power consumption.
- High bandwidth communication as TSVs cross dies along the surface of the chip
- Improved form factor and package volume density.
- Heterogeneous integration. Different dies in the stack could be manufactured by different wafer fabs, but also using different technologies. DRAM and logic integration in a single 3D-SIC becomes feasible.

Each manufactured 3D-SIC has to be tested to guarantee the required quality and defect-per-million (DPM) level. Several prior work addressed these issue and present test approaches for 3D-SICs [5–8]. For example, Lewis and Lee [9] considered pre-bond die testing in order to obtain a satisfactory compound yield. The authors proposed a scan island approach based on the IEEE 1149.1 [10] and IEEE 1500 [11]. Marinissen et al. [12] addressed many limitations of previous work by proposing a structured and scalable test access architecture using *TestTurns* and *TestElevators* to route test data through the stack, for pre-, mid- and post-bond tests. The architecture is further extended to support Multiple Tower (MT) stacking [13] and $2\frac{1}{2}$-D stacking [14,15]. Many of these features are ongoing activities in the IEEE P1838 [16,17] working group. JEDEC announced a new standard for Wide I/O mobile DRAM (JESD229 [18]). This standard supports interconnect testing through JTAG.

The state-of-the art in testing 3D stacked ICs assumes mainly the presence of scan chains and JTAG on each die, which are also used to perform interconnect test. However, stacked dies may not always contain JTAG interfaces. For instance, it is well know that memory providers are not in favor of integrating JTAG in their designs; they prefer rather to use a memory BIST (MBIST). Therefore, assuming that each stacked dies include JTAG is too optimistic. In this paper we will explore different ways of testing interconnects of stacked memory on logic both in the presence and in the absence of a JTAG interface. We also discuss the implications of having MBIST location (either on the memory die or on a logic day) on the different interconnect test approaches.

The remainder of this paper is organized as follows. Section II presents the requirements related to testing the interconnects of stacked memories. Section III presents an overview of existing 2D test standard that could be extended to 3D; it also briefly presents (on-going) 3D test standards. Section IV classifies possible 3D stacked memories. Section V explores the different interconnect BIST (iBIST) schemes for these memory classes, each scheme with its pros and cons. Finally, Section VI concludes this paper.

II. INTERCONNECT TEST REQUIREMENTS

Test standards need to satisfy certain requirements. For an interconnect BIST (iBIST), requirements can be classified and belong to the memory interface, test quality, compatibility with previous standards and to test modularity. Each of them is briefly described next.

A. Support for Different Memory Interfaces

A memory interface consists of a set of uni- or bidirectional wires possibly off-chip that describe the interaction with the memory. In 3D-SICs off-chip connections are mapped in the vertical dimension on TSVs. Typical interface signals include control, address and data signals as depicted in Figure 1. A memory consists of at least 1 access port, but in general could contain multiple read and write ports. The memory dies can operate either synchronously or

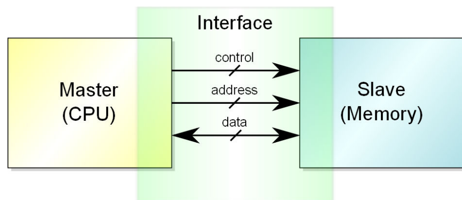

Fig. 1. Memory interface.

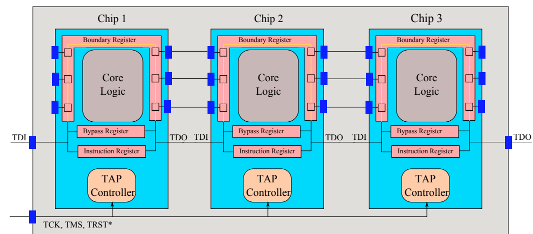

Fig. 2. IEEE std. 1149.1 wrapper.

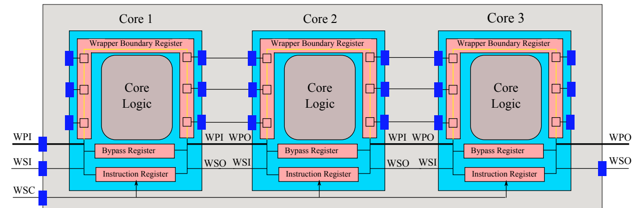

Fig. 3. IEEE std. 1500 wrapper.

asynchronously and are implemented using any technology such as SRAM, DRAM, Flash etc.

As we are dealing with stacked memory on logic, the interface as shown in Figure 1 has to be realized using TSVs. Therefore, failures in the interface or interconnects can be assumed to be independent of the memory technology under consideration. Hence, the iBIST solution has to deal with the interface irrespective of the memory type (e.g. SRAM, DRAM, Flash)

B. Test Quality

Design for testability and diagnosis is an important step in the design phase. Each wire/TSV that connects the master (e.g., CPU) with the slave (stacked memory) should be tested. Although TSVs are relative huge wires as compared to on-chip wires, many defects can occur; examples are as unfilled TSVs, partial filled TSVs, opens, roughness/spikes in TSV sidewall layers, manufacturing flaws in sidewall isolation oxide layer, leakage, etc. Any test solution should target as much as possible of such defects. Test patterns for some of such defects are well known [19]. However, as TSV are new components in the stack, new fault models might become relevant since a fully understanding of all TSV failure mechanisms is still needed; TSV keep-out-zone [20] and coupling [21] are examples of that.

C. Compatibility

Any suitable iBIST will add additional DfT hardware on the dies. However, the solution has to be compatible with the existing standards such as JTAG. Ideally the solution should form an extension of an existing/ongoing standards (such as the IEEE P1838 [16]) or easy to be integrated in them.

D. Modularity

The iBIST is responsible for interconnect testing only; e.g., it can be reused for any other kind of memories stacked on logic. Therefore the solution has to be modular. The concept of modularity provides many advantages such as (a) it helps in saving the development time and cost, (b) testing interconnect separately from the other dies, (c) allows memory providers to protect their IPs and withheld the implementation details even if the solution is integrated within the memory die, etc.

III. 3D Test Architectures

This section consists of two parts; first, it describes some of the familiar 2D test standards and subsequently, the (on-going) 3D standards. Here, we primarily focus on the interconnect test part as it is the main purpose of this paper.

A. 2D standards

The existing 2D test standards can be classified into three categories:

- Boundary Scan (BS) based: in this category input and output pins are wrapped by boundary cells. Testing input and output pins goes through this hardware.
- Test Logic (TL) based: in this configuration pins are tested by specific dedicated logic that generates output sequences based on the inputs.
- Instrumentation based: in this configuration, test units are activated by means of test instruments.

Boundary Scan based

Several standards are based on the boundary cell concept. In this section, we consider the two most important ones, i.e., JTAG [10] and IEEE Std. 1500 [11].

JTAG (also known as IEEE Std. 1149.1) is primarily developed for interconnect tests (EXTEST) on a Printed Circuit Board (PCB), but it can also be used to test independent dies on the board (e.g. diagnosis mode). JTAG comes with a low cost wrapper around each pin of each chip and is controlled by the TAP controller as depicted in Figure 2. The figure shows an example in which three chips are placed on a PCB. The Test Data Input (TDI) and Test Data Output (TDO) of each chip are cascaded and form a sequential chain. The operation mode of each chip is controlled through the TAP controller.

As System on Chips (SOCs) get more sophisticated and more IP-cores are integrated, test time becomes more critical. This necessitates a standard (IEEE Std. 1500 [11]) that supports cost-efficient testing of core-based SoCs. A similar wrapper as for the IEEE std. 1149.1 is placed around the core, with mainly the following differences: (a) the newer standard supports a wider parallel test data interface denoted by WPI, and (b) the WIR register is controlled directly at the cost of some extra I/O pins.

Several other (ongoing) standards that are based on a wrapper cell similar as in JTAG can be found in literature such as IEEE P1149.7. We refer to all of these schemes as Boundary Scan based testing.

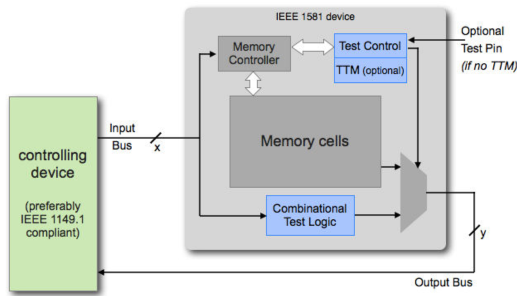

Fig. 4. IEEE std. 1581 [22].

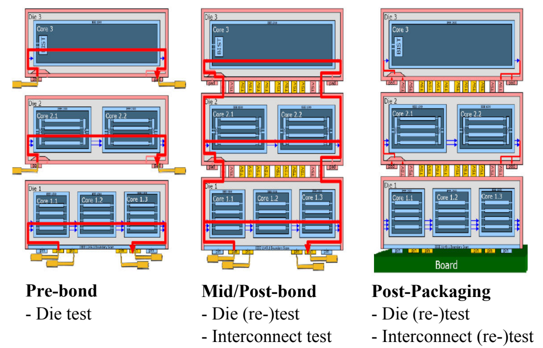

Fig. 5. IEEE P1838 [16].

Test Logic Based

A complete different way to test interconnects is by inserting dedicated logic for it. Figure 4 shows this concepts for a memory slave for the IEEE Std. 1538 [22]. In normal mode, the interconnects between the memory and host (e.g., a CPU) are in transparent mode and memory operations are not affected by the additional test hardware. However, the memory is bypassed in test mode and the inputs of the memory are directly forwarded to its outputs through combinational test logic. The combinational test logic usually consists of a couple of XOR gates. In the IEEE Std. 1538 the test mode is either activated by a dedicated pin or by the Transparent Test Mode (TTM) [22], where the TTM activates the test by special input sequences. For example, a specific clock frequency on the clock input pin of the memory, or a fixed input pattern that normally is considered to be an invalid can activate the test mode. The advantage of this scheme over BS based testing is a much more efficient test methodology for complex memories such as Flash EEPROM.

Instrumentation based

In instrumentation based testing, test resources on the chip are accessed using instruments, where each instrument could be any DfT unit such as a logic BIST, an MBIST, an analog BIST, etc. The instruments target only fractions of the chip. An ongoing standard is the IEEE P1687 [23]. By incorporating an instrument for TSVs, interconnects between dies can be tested. We do not consider this option in the remainder of this paper as it is currently not standardized.

B. 3D Standards in development

As 3D-SICs are quickly gaining more ground the need for a standardized test becomes more important. Several DFT solutions have been proposed [5–9], but with many limitations such as being not able to perform a test on a partial stacked die. Nevertheless, two promising standards are IEEE P1838 [16,17] and JEDEC 229 [18].

The IEEE P1838 is an on-going standard for 3D-SICs and focuses on dies as key components in the stack. The stack-level architecture routes both data and control signals up and down through the stack (TestTurns and TestElevators) to reach each particular die in the stack. The architecture supports both intra-die test (INTEST) and inter-die test (EXTEST) during all test phases as depicted in Figure 5. In the pre-bond phase, dedicated pads are used to test dies. In the mid-bond and post-bond phases, both dies in partial and a complete stack respectively can be tested (INTEST). EXTESTs can be performed for the interconnects during mid-bond and post-bond and are based on the JTAG [10] and IEEE1500 [11] standards. The final test (post-packaging) consists of the same tests options.

Recently, JEDEC announced a new standard for wide I/O mobile DRAM [18]. This standard is more than a test specification and targets the whole memory; the target is to improve memory bandwidth and to reduce latency, power, and form factor. The wide I/O specification defines the interface between logic and memory (LMI). With respect to testing, the following two functionalities are provided by the standard. The first added DfT hardware is JTAG used to test for contacts (TSVs and microbumps) and I/O testing. The second test feature is a post-assembly DRAM test to ensure the quality of memory dies. This makes it possible to test the DRAM independently from the logic chip. The DRAM layers are tested either through direct access pins or by electrical connection through General Purpose Input/Output (GPIO) drivers/receivers.

IV. 3D Stacked Memory Classification

In this section, we focus on the die test of the 3D memory. Section IV-A first presents the possible test moments. Thereafter, Section IV-B classifies 3D stacked memory.

A. Testing 3D ICs

This section presents first the differences between 2D and 3D test flows and shows that for 3D ICs many test moments are possible. These test moments are thereafter compiled into a framework of test flows.

A conventional 2D test flow for planar wafers is depicted in Figure 6(a) [24]. Here, usually two *test moments* are applicable; i.e., a wafer test prior to packaging and a final test after packaging. The wafer test can be cost-effective when the yield is low, since it prevents unnecessary assembly and packaging costs. The goal of the final test is to guarantee the final quality of the packaged chip. During the manufacturing of a 3D-SIC, additional test points can be defined for each partial created stack. At each test point a distinction can be made between die tests and interconnect tests. Die tests

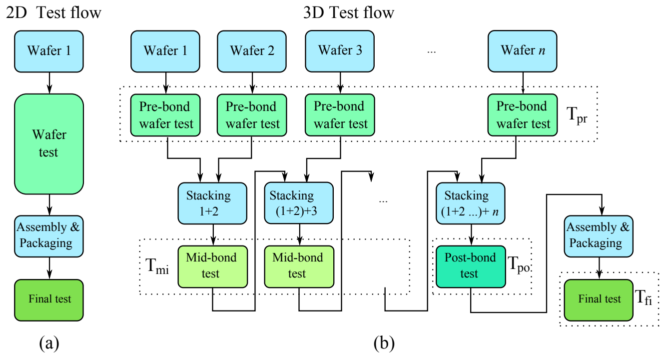

Fig. 6. 2D versus 3D D2W test flows.

ensure the functionality of individual dies, while interconnect tests ensure functional TSVs between dies. For 3D-SICs, four test moments can be distinguished in time as depicted in Figure 6(b), and explained next.

1) T_{pr}: n *pre-bond* wafer tests, since there are n layers to be stacked. T_{pr} tests prevent faulty dies entering the stack. Besides die test, preliminary TSV interconnect tests can be applied. For example, in [25] the authors use a capacitance test to detect some of the faulty TSVs. In [26], the authors propose active probing to detect faulty preliminary TSVs.
2) T_{mi}: n-2 *mid-bond* tests applicable for partial created stacks. In this case, either the dies, the interconnects, their combination or none of them can be tested. Good tested dies in the pre-bond test phase could get corrupted during the stacking process as a consequence of e.g., die thinning, and bonding [27].
3) T_{po}: one *post-bond* test. This test can be applied after the complete stack is formed. Analogous to wafer testing in the 2D test flow, T_{pr} can be applied to save unnecessary assembly and packaging costs. Both interconnects and dies can be tested.
4) T_{fi}: one *final* test can be applied after assembly and packaging to ensure the required quality of the complete 3D-SIC. Other specific packaging related tests could be applied at this test moment as well.

Note that in total there are $2 \cdot n$ different test moments.
Depending on whether one or more companies are involved in the manufacturing of 3D-SICS, different requirements can be set for the pre-bond wafer test quality [28]. If the (pre-bond) wafers are produced by one or more companies and the final 3D-SIC product is processed and manufactured by another company, a high pre-bond wafer test quality (e.g. a KGD) often is agreed upon. If a KGD contract is in place, high-quality pre-bond testing is required. If such a contract is not in place, the pre-bond test quality is subject to optimization. This means that there is not only the option to perform pre-bond testing or not, but also to perform pre-bond testing at a higher or lower test quality. Faulty undetected dies can be detected in a later stadium, e.g., in higher quality post-packaging tests. Similarly, a high quality pre-packaging test (Known-Good-Stacks test) can be applied.

A pre-bond memory die could be tested with a MBIST engine. That same engine could be reused for mid-, post-bond and final tests. For the iBIST, pre-bond testing is not considered as interconnects are only formed after stacking.

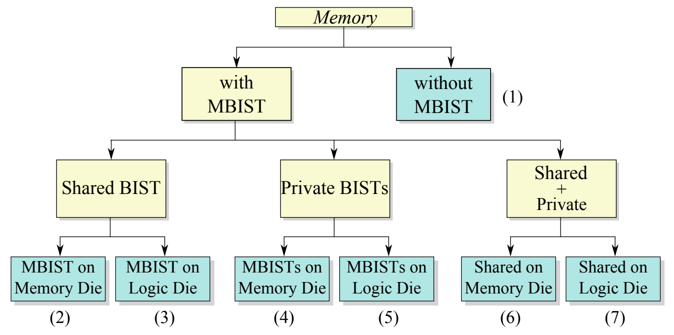

Fig. 7. 3D Stacked memory classification.

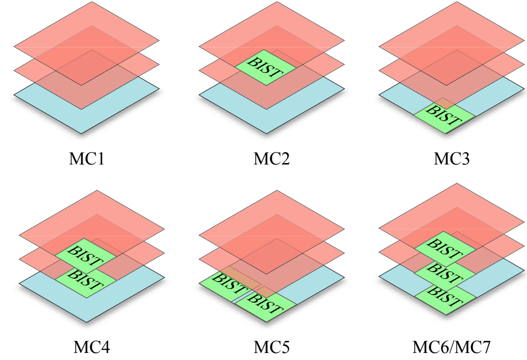

Fig. 8. Memory configurations.

B. 3D Stacked Memory Classification

Memories are typically tested by MBISTs which perform high quality at-speed tests. In 3D memories, one or several of MBISTs might exist in the stack simultaneously and there number is a trade-off between area, test time, yield, etc. For example, MBIST and/or Built-in-Self-Repair (BISR) circuits in the pre-bond phase allow dies to be tested and repaired prior to stacking, while a shared MBIST/BISR unit in the mid-bond or post-bond phase can also be used for vertical repair, i.e., inter-die redundancy. Each memory configuration affects the test and repair strategy. We define 7 cases of 3D stacked memories as depicted in Figure 7 based on the availability of MBIST engines, whether they are shared or private, and their location (on the memory or logic die) in the stack. They are further explained next and an example is given for each memory configuration (MC) in Figure 8. The examples consist of two top memory dies and a single bottom logic die. Note that each configuration could have 0, 1 or more BIST engines based on the configuration.

1) MC1 contains no MBISTs engines. Therefore, pre-bond testing (if performed) is done by probing the dies likely with lower quality and/or higher test cost as compared to using an MBIST). In the final phase, testing of memory can be performed through the logic layer, e.g., a CPU test [29]. This configuration is not interesting as it might be difficult to guarantee test quality and to perform diagnosis.
2) In MC2 a shared MBIST engine is placed on one of the memory dies. The MBIST can be used for

pre-bond testing and for post-bond testing when the whole memory is created. A clear visible drawback of this scheme is non-identical memory layers (with DfT and without DfT). The memory layer without an MBIST faces a similar pre-bond test problem as in MC1. An additional drawback are extra vertical TSV connections that are required to access and program the MBIST. Benefits of this system include area efficiency (a single BIST only), and close to at speed testing (latency to CPU is not taken into account). Moreover, an optimal test algorithm can be programmed as the memory manufacturer is responsible for the MBIST content. Theoretically speaking, if the repair rate is high enough the pre-bond tests can be skipped as the memory can be repaired in a later phase.

3) In MC3 the shared MBIST is placed on the logic die. Note that this logic die could be an interposer (used for the peripheral circuits) or be residing an actual design such as a CPU. This configuration has the benefit that at speed testing can be performed. However, as the memory dies could be manufactured in a different company then the CPU die, the system integrator is responsible for the memory test algorithms (which could be non-optimal due to confidentiality). Inter-die repair is a still possible, but the mutual sharing of resources on the memory dies becomes harder to implement. More interesting for this configuration is to use global spare resources on the logic die to replace faulty cells in the memory. Note that defects also occur due to stacking. Similarly as in MC1, pre-bond testing can only be done by probing. This configuration is efficient in terms of area (a single MBIST only) and cost less to access as compared to MC2.
4) MC4 is in essence an extension of MC2 in which each layer has its own private MBIST. If we compare this configuration with MC2, we see an extra cost in terms of area, but at each die can be tested at pre-bond using its private MBIST. Other benefits of this scheme are independent testing of layers in parallel (faster in test time) and inter-die repair can be realized similarly as in MC2.
5) MC5 can be seen as an extension of MC3, where each layer has its own MBIST on the logic die. Benefits of MC5 include test time reduction if both MBISTs run in parallel each optimized for its own memory layer and expense of extra area. The remainder benefits of this configuration are similar as MC3 such as global memory repair.
6) The theoretical difference between memory configurations MC6 and MC7 is the location of the shared MBIST in the stack (in the logic die for MC7 and in one of the memory dies in configuration MC6). We only consider the case where this shared MBIST is placed on the logic layer (i.e., MC 7). MC7 is basically now an extension of MC3 and MC4 and has therefore both benefits of these configurations (i.e., at speed testing in the pre-, mid- and post-bond and final tests all with repair capabilities). Drawback, however, is the additional area overhead. This memory configuration might exist for the case where the dies in the stack are composed of different technologies (e.g., FLASH, DRAM etc. all with their private MBISTs) and where a shared MBIST on the logic die is used for a global memory test.

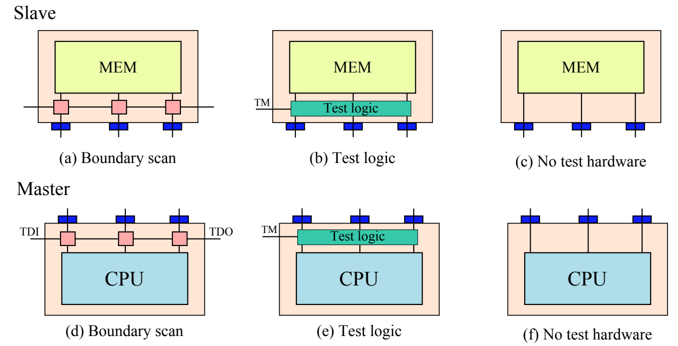

Fig. 9. iBIST schemes.

V. 3D iBIST Schemes

The second part that requires testing in 3D-SICs are the vertical interconnects. Figure 9 shows the hardware required for interconnect testing using the BS and *test logic*. The figure shows the required test infrastructure for both the master (logic) and slave (memory) dies such that interconnects become testable. On the slave side the test hardware for the interconnects consists either of (a) a boundary scan or (b) test logic or (c) no dedicated DFT. Similarly, cases (d), (e) and (f) show the same options for the master which in this case is considered to be a CPU. In total, nine combination can be formed. We discuss in short the applicability of each of these schemes which are depicted in Figure 9 from the master's perspective.

a) Master side - Boundary Scan: Figure 9(d) shows the case where the interconnects on the master die are tested with BS. In theory, the master could be connected with all the 3 test options for the slave. In case both the master and slave are connected using BS, it requires proper mode selection of the dies such that the return paths of the BS chain are matched [12]. In case, the interconnects on the memory side are connected to test logic, the BS has first to be put in the proper test mode. After that the test logic should be activated and subsequently the responses of the test logic based on the shifted patterns must be captured. The last case, where the memory has no test seems impractical for test purposes. Nevertheless, if this option is selected test patterns have to be applied in such away that the interconnects are tested through the memory. This might have a severe impact on test time for the interconnects.

b) Master side - Test logic: Figure 9(e) shows the case where the interconnects on the master die are connected using test logic. Note that the test logic on the Master side is different from the test logic on the slaves. On the master, the test logic is responsible for test pattern creation, while the test logic on the slave side only responds by sending patterns back based on its inputs. When the master contains dedicated test logic for the interconnects, it would be most

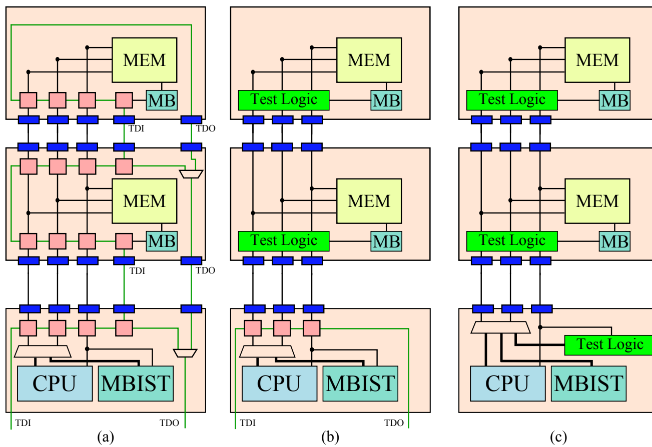

Fig. 10. Interconnect DFT for MC 7.

likely to have dedicated test logic on the slave side as well. These patterns can be stored on the master die (as only few patterns are required for interconnect tests [19]), or can be shifted in using normal scan chain if available.

c) Master side - No Test: In case there is no additional hardware support for interconnect testing (Figure 9(f)) on the master die it would be hard to communicate with any DfT on the Slave. Therefore, no direct test support for interconnects seems the only applicable case; nevertheless attempts could be made to force values on the TSVs indirectly by using internal scan chains if available. This approach without any DFT for the interconnects seems risky. In the final test, however, interconnects can still be tested indirectly for example through a CPU test, but requires more research.

From the schemes discussed above, we select the tree most promising iBIST configurations and combine their DfT with the MBISTS of configuration MC7 (most extensive configuration of Figure 8); the three iBIST schemes are depicted in Figure 10. Figure 10(a) shows this for the first case where both the master and two slaves contain a boundary scan. Note that the return path of the BS is multiplexed in order to differentiate between pre-bond and post-bond tests. Part (b) of the figure shows the second case where the slave contains test logic. As there are multiple slaves with test logic, each slave has to have its own activation circuit. This can be obtained for example by having different activation frequencies. Finally, part (c) depicts the hardware for the third case in which both the master and slave contain test logic for the interconnect test. Future research should determine which approach performs best in terms of test time and area overhead for given memory configurations.

VI. Conclusion and Future Work

In this paper, we described challenges and test opportunities for 3D stacked memories consisting of die tests and interconnect tests. First, we presented the possible test moments for a 3D-SIC. Thereafter, we explored for die tests the impact of the MBIST location and discussed how they affect quality and memory repair. For interconnect tests, several test approaches (or iBISTs) were explored. These explorations are required to develop low cost standardized test methodologies. In the future we will design and implement the iBIST schemes to obtain accurate trade-offs in term of hardware overhead and latency.

Acknowledgements

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