3D-COSTAR: A Cost Model for 3D Stacked ICs

Abstract— **Selecting appropriate and efficient test flow for a 3D Stacked IC (3D-SIC) is crucial for overall cost optimization. This paper presents 3D-COSTAR, a tool that considers costs involved in the whole 3D-SIC chain, including design, manufacturing, test, packaging and logistics (e.g. related to shipping wafers between a foundry and a test house); and provides the estimated overall cost and cost breakdown for a given input parameter set (e.g., test flows, die yield and stack yield). As a case study, the tool is used to compare the overall cost of producing a 3D-SIC by an Integrated Device Manufactures (IDM) and a fab-less company. For the fab-less company, we assume that each step in the 3D-SIC chain is outsourced to a different company. Therefore, additional logistics costs and high quality test contracts are in place; while an IDM does not have these constraints. Simulation results show that by choosing an appropriate test flow the overall 3D-SIC cost for the IDM can be reduced up to 20% for a 5-layered 3D-SIC.**
Keywords: *3D integration, cost modeling, test cost, test flows.*

I. Introduction

Tremendous effort has been put in place to bring *Through Silicon Via (TSV)* based 3D-SIC technology closer to market [1]. Realizing such ICs is attractive due to major benefits [2] such as (a) increased electrical performance, (b) reduced power consumption due to shortened interconnects, (c) heterogeneous integration supporting optimized logic, memory, RF, MEMs etc., and (d) reduced form factor, etc.

One of the major challenges that has to be addressed in order to make this technology commercially successful is overall cost optimization. As is the case for any IC, TSV-based 3D-SICs must be tested in order to guarantee the outgoing product quality and reliability. Hence, test cost is indispensable. Inherent to their manufacturing process, 3D-SICs provide several test moments such as before stacking, during manufacturing of partial stacked IC, after the complete manufactured stack, etc. This results into a huge space of test flows; each with its own cost. Determining the optimal and most efficient test flow requires the analysis of all test flows, as different design and/or manufacturing parameters may impact the cost differently. Therefore, an appropriate cost model is required. The cost model should be able to evaluate the cost of each test flow, while considering all relevant incurred costs in the production chain of 3D-SIC. For instance, a pre-bond test for TSVs requires additional test hardware on the die and therefore impacts the manufacturing cost.

Limited work has been published on this topic [3–8]. In [3], the author considered a manufacturing cost model for 3D monolithic memory integrated circuits; cost improvement of 3D with respect to 2D (for different 3D stack sizes) was modeled. In [4], the authors developed a 3D-cost model to determine the optimal stack size for a given 3D-SICs circuit, where they restricted the variable parameters to only die yield and area. In [5], the authors proposed a 3D cost model for Die-to-Wafer (D2W) and Wafer-to-Wafer (W2W) stacking. In [6], a detailed cost model of IMEC is presented; the paper primarily focuses on (a) the difference between cost integration for D2W and W2W stacking, (b) the impact of the number of TSVs and (c) the effectiveness of different 3D testing strategies in the pre-bond phase for D2W stacking. In [7], a 3D cost model is presented that focuses on modeling of metal layers and die area impact on 3D-cost integration for D2W and W2W integration. In [8], a 3D cost model is primarily developed to estimate the optimal tier count that leads to a minimal TSV count and subsequently partition the netlist into these tiers. However, none of the published work is able to model the impact of the test cost on the overall 3D-SIC cost since none of them considers the different test moments and test flows. In [9], a basic cost model for D2W stacking considering the impact of some test flows on the overall 3D-SIC cost was presented. However, this model suffers from many limitations addressed in [10] such as (a) a lack of support for variable fault coverage, (b) a restriction to a small set of test flows, (c) no consideration of logistics cost, (d) a focus on D2W stacking only, (e) no distinction between die and interconnect tests, (f) no support for parallel testing of dies, (g) no support for tower stacking, etc.

This paper presents 3D-COSTAR, a tool to evaluate test cost and overall 3D-SIC cost for any test flows without the above mentioned limitations. The tool is based on a cost model considering all costs involved in the 3D-SIC production chain including design, manufacturing, test, packaging and logistics; the logistics costs are mainly related to fab-less companies as they e.g. outsource testing and hence move the tiers from a foundry to a test house. As a case study, the tool is used to evaluate the cost price of a 3D-SIC using D2W stacking for an Integrated Device Manufacturer (IDM) and a fab-less company.

The rest of this paper is organized as follows. Section II and III present the architecture and flow of 3D-COSTAR respectively. Section IV covers a case study where the cost for an IDM and a fab-less company are compared. Finally, Section V concludes the paper.

II. 3D-COSTAR Requirements and Use cases

This section describes the architecture of 3D-COSTAR. First, the tool requirements are discussed and thereafter the tool use cases.

A. 3D-COSTAR Requirements

In order to determine the most cost-effective test flow, the test requirements should be specified. However, taking only the test cost into consideration is not sufficient to provide a fair comparison between the different test flows; a test flow does not only impact test cost, but also manufacturing cost and even design cost. For example, a pre-bond TSV test requires additional DFT hardware, while it prevents faulty dies to enter in the stack if detected. As a consequence, the die area increases (less dies per wafer).

Figure 1 shows the general architecture of 3D-COSTAR. The tool has five input classes which symbolize the costs involved in the whole 3D-SIC production flow; these include design cost, manufacturing cost, test cost, logistics cost and packaging cost.

a) Design: Design for Testability (DfT) starts at the design phase to accommodate for tests at later stages (pre-bond, mid-bond, post-bond and final tests). For example, pre-bond testing of TSVs using landing pads affects the chip layout and chip area, while can detect some faulty TSVs prior to stacking [12]. Similarly, mid-bond testing requires dedicated hardware to support testing during this phase. These types of trade-off are strongly test flow dependent and must be decided at design time as they impact the design and its associated cost.

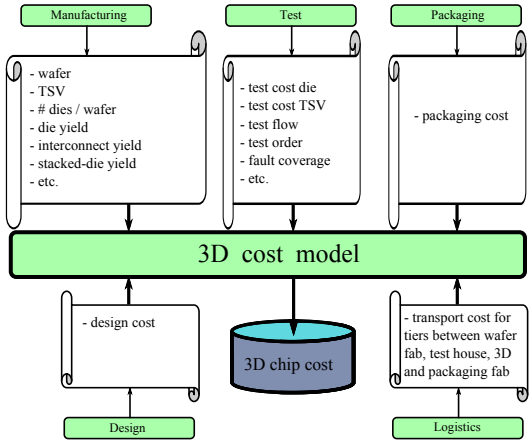

Fig. 1. 3D-COSTAR Organization.

b) Manufacturing: Manufacturing requirements are related to the fabrication, processing of wafers and the stacking of tiers. As the manufacturing is not perfect, TSV yield, die yield, and stacking yield are required to accurately determine the cost. The manufacturing class covers a wide range of parameters and consists mainly of two parts: (a) manufacturing cost related to 2D IC and (b) cost related to 3D stacking processing steps. The first part depends on the wafer cost, die yield, number of dies per wafer, cost of manufacturing steps, etc.; all of these results into a cost of a die per wafer. In case additional hardware is integrated for DfT, the number of dies per wafer reduces and therefore increases the chip cost. The second part depends on the cost of TSVs, wafer thinning, bonding (i.e., Die-to-Die (D2D), D2W and W2W), stacking process (i.e., Face-to-Face, Back-to-Face or Back-to-Back), interconnect yield, stacked-die yield, etc.; and it strongly depends on the applied test flow [9]. It is worth noting that the chosen bonding type and stacking process have a large impact on the cost and the yield of the 3D-SIC; for instance, in D2D and D2W stacking, Known Good Dies (KGD) can be stacked on each other to maximize the yield. This is not applicable in W2W stacking and therefore generally results in lower yield [16,17]. Moreover, as exact profiles of faults introduced during the 3D stacking are not know/published yet, the tool is built such that it supports any fault distribution during stacking.

c) Test: Figure 2(a) shows the conventional 2D test flow for planar wafers [11]; it consists of two test moments: a wafer test prior to packaging and a final test after packaging. The wafer test can be cost-effective when the yield is low as it prevents unnecessary assembly and packaging costs, while the final test is used to guarantee the final quality of the packaged chips. 3D-SICs, however, provide additional test moments; e.g., additional test moments can be defined for each partial stack. Moreover, at each moment a distinction can be made between different tests such as die tests and interconnect tests. In general, four test moments can be distinguished for 3D-SICs as depicted in Figure 2(b): (1) T_{pr}: n *pre-bond* wafer tests, (2) T_{mi}: n-2 *mid-bond* tests, (3) T_{po}: one *post-bond* test prior packaging and (4) one *final* test.

A *test flow* can be can be extracted from the above four defined test moments, which consist in total of $2n$ different moments. A test flow is as a collection of tests applied at these test moments. At each test moment, zero, one or more tests, possibly with different fault coverages, both for dies and/or interconnects, can be applied. Depending on the used test flow, the test cost might increase significantly. Therefore, skipping or reducing quality requirement at some test moments can restrain the test cost.

In addition, using advanced test equipment to reduce the test cost, parallel testing can be also used. Dies belonging to different layers can be tested in parallel if there is DFT support available for it.

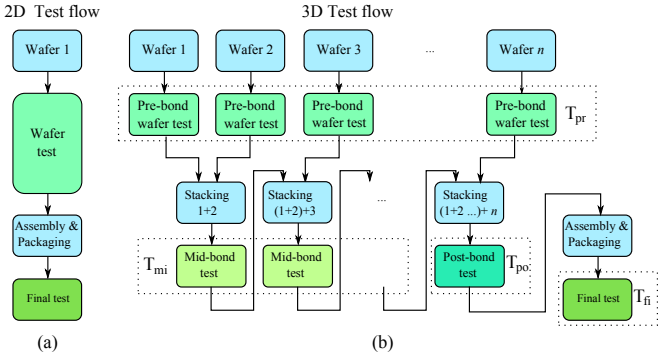

Fig. 2. 2D versus 3D D2W test flows.

3D-COSTAR does support the calculation of test cost for both parallel and serial testing of 3D-SICs.

The test cost can be company dependent as the quality of the applied tests could differ, e.g., for IDM and fab-less companies. For instance, depending on whether one or more companies are involved in the supply chain for the manufacturing of 3D-SICs, different test requirements can be set for the pre-bond wafer test [20]. If the wafers are produced by one or more companies and the final 3D-SIC product is processed and manufactured by another company, a high pre-bond wafer test quality (e.g. a KGD) often is agreed upon. If a KGD contract is in place, high-quality pre-bond testing is required. If such a contract is not in place (e.g., for an IDM), the pre-bond test quality is subject to optimization. Hence, at pre-bond test moment, we can not only perform or skip the pre-bond test, but we can also tune the quality of the applied test for cost optimization. Faulty undetected dies at this test moment can be detected in a later test moment, e.g., when applying a higher quality test in the final test moment. Similarly, a high quality mid- or post-bond test can be applied.

3D-COSTAR calculates test cost for any possible test combinations (test flow). Both the type of test and the used test flow impacts the overall 3D-SIC cost. Therefore, specifying an optimized test flow should be with full freedom, i.e., without any restrictions on the test moment, on the used test (die, interconnect or both), neither on the fault coverage, etc. The complexity of the test flow depends on the number of test moments, which increase linearly with the stack size. Hence, 3D-SICs could be probed several times. However, having several touch-downs on the bottom wafer for testing purposes can damage the bonding-bumps. Therefore, setting an upper limit of maximal allowed touch-downs for any test flow is very practical. 3D-COSTAR uses a variable parameter to set up this upper limit.

d) Packaging: After the 3D-SIC is manufactured and perhaps tested (a post-bond test), the 3D-SIC is assembled and packaged. The cost attributed to packaging depends on the used materials and technology [14]. We assume an independent cost for the packaging, i.e., it has no dependency with the other classes. Since all processing steps are defect-prone, a yield for the packaging has to be considered as well.

e) Logistics: The production of 3D-SICs requires design, manufacturing, test and packaging costs. However, to make a distinction possible between fab-less, fab-lite and IDM companies, an additional set of hidden costs, referred to as logistics, is needed. For instance, a fab-less company may perform stacking and testing in different houses/countries, while IDM may perform all the required processing steps in a single house/location. Therefore, logistics costs are a direct consequence of moving dies and wafers between different locations. Figure 3 shows an overview of logistics costs considered in our tool. It presents all possible logistics costs for the worst case scenario in which each activity in the 3D-SIC production chain can be outsourced; hence, the associated logistics

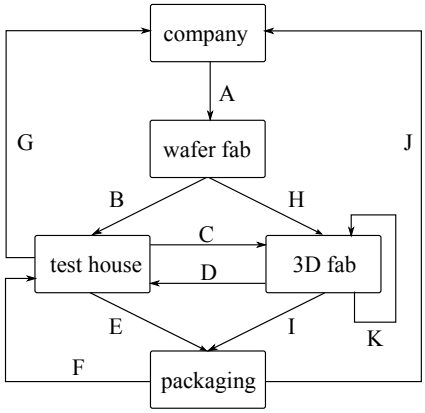

Fig. 3. Logistics cost for 3D-SIC.

costs have to be separated from each other. The figure assumes five companies/houses to be involved in the production chain: design company, wafer fab, 3D fab, test house and packaging house. A cost is associated to any moving activity of lots/wafers between any of these companies and is denoted by an arrow with a letter. There are in total 11 possible costs denoted by A till K. It is worth noting that test flows have a large impact on the logistics cost. Depending on the company type and test flow, some of the costs are not applicable. For example, in case pre-bond tests are skipped (arrow H), the cost associated with arrow B is inapplicable.

B. Use cases

Use cases define the functionality of the tool in terms of inputs and outputs. There are three main use cases.

1) *Overall cost calculation*. The primary goal of the tool is to calculate the overall cost of the production of 3D-SICs for different test flows, based on pre-defined input parameters in order to optimize the cost. The overall cost includes design, manufacturing, test, packaging and logistics cost.
2) *Cost breakdown*. The second use case is the analysis of the cost by breaking it down into design, manufacturing, test, packaging and logistics costs. This analysis reveals the share of each cost and provides insights about possible further cost optimization.
3) *Sensitivity analysis*. The third use case is sensitivity analysis of input parameters; it identifies those parameters that have largest impact on the overall cost. Thus, tuning these parameters first results in largest cost reduction.

III. Tool Flow

Figure 4(a) presents a high-level overview of the tool flow. The tool starts by reading all input parameters from the input files and subsequently creating the stack. Thereafter, the cost is calculated by taking involved costs into consideration and moving through the IC production chain of the IC (see Figure 4(b)). At each step, the tool updates the impacted cost if applicable. For instance, if a mid-bond test is performed, then the test cost has to be updated. Reading the input parameters, creation of the stack and the cost calculation are the core steps of the tool. They are explained next.

Read parameters

The first stage of the tool reads the input parameters of each class. The parameters are specified by keywords and read from a file. For example, keywords that must be specified that are related to manufacturing are *die cost*, *die yield* etc.

Stack creation

Figure 5 shows an example of how the creation of a stack take place and how is this information internally stored. Part (a) of the figure depicts a particular multiple tower stack IC. It consists of a

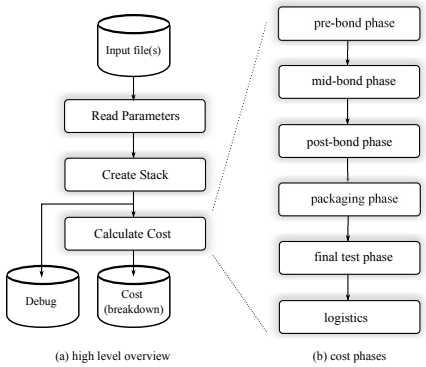

Fig. 4. Tool flow.

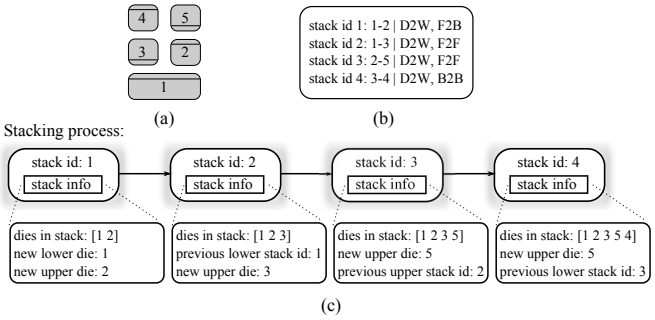

Fig. 5. Creating the stack.

bottom die/wafer labeled 1, a die labeled 2 stacked on die/wafer 1 using die-to-wafer (D2W) stacking process and face-to-back (F2B) stacking orientation, a die labeled 3 stacked on die/wafer 1 using D2W stacking process and face-to-face (F2F) stacking orientation, a die labeled 4 stacked on die 3 using D2W stacking process and back-to-back (B2B) stacking orientation, and a die labeled 5 stacked on die 2 using D2W stacking process and F2F stacking orientation. Part (b) of the figure, shows how this stack is read by 3D-COSTAR. This particular stack consists of 5 stacking operations; each operation requires a specific stacking process and orientation. Figure 5(c) shows how the information is used to create and store the stack internally in the tool. The stack is stored as an array of stacking operations. For example, after the first stacking operation (stack id: 1), the created stack consists of die 1 as a bottom/lower die and die 2 as an upper die. A debug file is created with the stack to verify the inputs.

Cost calculation

Given the input parameters, the different involved costs are calculated step by step by moving through the different phases shown in Figure 4. All costs are impacted by one of more of such phases. For example, pre-bond and mid-bond phases contribute to the manufacturing cost and requires DFT hardware (hence impacting the design cost as well), while these two phases together with post-bond phase and final phase contribute to test cost. The logistics cost strongly depends on the required number of movements of lots/wafers; e.g., between wafer fab, 3D stacking fab, test house, etc. The packaging cost is calculated based on the required packages for all the considered good stacked ICs (outgoing yield of the stack) after the post-bond test. The overall cost of 3D-SIC is calculated by summing up all the cost of design, manufacturing, test, packaging and logistics.

Not all dies enter the stack. For instance, dies that are tested faulty in the pre-bond phase. To obtain the cost, the ratio of dies that enter the stack have to be calculated properly. We use Equation 1 to define the relation between test escapes TE, ingoing yield Y_{in}

and outgoing yield Y_{out}; TE is the ratio of faulty dies that pass the test. The ingoing yield is the actual yield, the outgoing yield is the fraction of dies that is considered good after testing. Equation 2 [15] shows the relation between the test escapes, ingoing yield and the fault coverage (FC). By combining equations 1 and 2 we obtain Equation 3, the outgoing yield as a function of the ingoing yield and fault coverage.

$$TE = \frac{Y_{out} - Y_{in}}{Y_{out}} \quad (1)$$

$$TE(Y_{in}, FC) = 1 - Y_{in}^{1-FC} \quad (2)$$

$$Y_{out} = \frac{Y_{in}}{1 - TE} = \frac{Y_{in}}{Y_{in}^{1-FC}} = Y_{in}^{FC} \quad (3)$$

We assume that all these equations are valid for all yield operations involved in the manufacturing of the 3D-SIC; i.e, for the manufacturing of dies, TSVs and interconnects. For instance, imagine that dies of type d_2 need to be stacked on the top of dies of type d_1 (see Figure 5); each die has its own yield and FC. If d_1 is total number of bottom dies, then the total number of dies of type d_2 (say d_2) needed for the stacking will be:

$$d_2 = \frac{d_1 \cdot Y_{out,1}}{Y_{out,2}} \quad (4)$$

Each time a new die enters an already existing partial stack, its quantity is determined by combined outgoing yield of the dies. These steps are repeated until the whole stack is completed.

IV. Case Study

3D-COSTAR is an extensive tool that can be used to evaluate many aspects related to 3D-SIC test and cost evaluation. Examples are (a) compare cost analysis for D2W vs W2W stacking, (b) investigate the benefits of parallel testing (c) analyze manufacturing and test cost for tower stacking, (d) evaluate different test flows for variable fault coverage, (e) sensitivity analysis etc. In this section, however, the tool will be used to evaluate the impact of the overall 3D-SIC cost for two different companies, while producing the same 3D-SIC chip; an IDM company (say Company A) which has all its activities in-house (i.e., design, manufacturing, testing and packaging), and a fab-less company (say company B) which outsources all of its activities (expect the design). Section IV-A describes the default values used for cost evaluation for both companies. Section IV-B lists the performed experiments. Section IV-C presents and discusses the simulation results. Note that because of space limitations we focus only on the overall cost rather then on the cost break down or sensitivity analysis.

A. Experiment/parameter Setup

In order to make a fair comparison, it is assumed that the two companies under consideration (IDM and fab-less) target the production of the same 3D-SIC.

Design cost: For this case-study, we assume that the design cost for both companies are the same; therefore, such cost has no impact on the overall picture and cost comparison.

Manufacturing cost: Manufacturing cost consists of cost related to wafer/die, cost related to TSVs and cost related to stacking process.

Wafer/die cost depends on several parameters, e.g., stack size, die yield, number of dies per wafer, stacking yield, interconnect yield, etc. We consider a stack size n=5 where dies are stacked in a D2W fashion, in which the dies are identical in terms of yield and cost. The yield of the dies is based on the reference process in [16], where a standard 300 mm diameter wafer is used with an edge clearance of 3 mm. This work assumes a defect density of d_0 = 0.5 defects/cm^2 and a defect clustering parameter $\alpha = 0.5$. With a die area $A = 50\ mm^2$, the number of Gross Dies per Wafer (GDW) are estimated to be 1278 [21]. With the negative binomial formula for yield, a die yield of $Y_D = (1 + \frac{A \cdot d_0}{\alpha})^{-\alpha}$ = 81.65% is expected [15]. To estimate the cost to manufacture and process a wafer we use the cost models of [22] and [23]; the total price of a 300 mm wafer is estimated at approximately \$2779. The model in [22] considers a variety of costs, including installation, maintenance, lithography and material.

TABLE I

Fault coverage versus test cost.

fault coverage (%)	ratio test cost (%)	test cost (\$cent)
100	100	23
95	28	6.44
85	13	2.99
75	3	0.69
0	0	0.00

For the cost of manufacturing TSVs, we base our numbers on the work of EMC-3D consortium [24]; the cost of fabricating 5 μm TSVs on a single wafer is \$190 and is additive to wafer cost. We assume the cost of manufacturing TSVs to be 60% of the 3D stacking process cost [6]. Further, we assume the TSVs to have a yield of 98% per die.

The 3D stacking process cost (including bonding, thinning etc..) is assumed to be \$126 (40% of total 3D cost) [6]. In addition, the stacking yield is assumed to be composed of two parameters: the interconnect (TSV) yield Y_{INT} and the stacked-die yield Y_{SD}. In our simulations, the interconnect yield Y_{INT} is considered to be 99%. For the good dies that enter the stack, a small probability exists that they get corrupted during stacking; this is modeled by the stacked-die yield Y_{SD} and is assumed to be 97%. In [16], a stack yield of approximately 96% is used.

It is worth noting that for our case-study, we assumed that during the stacking only the *top* two dies and the interconnect between them could be corrupted; they are assumed to be defect-prone to stacking/bonding steps like heating, thinning, pressure.

Test cost: To estimate the test cost per die, the model in [15] is used; the model includes depreciation, maintenance and operating cost and assumes five ATE machines operating simultaneously. The derived test cost equals 3.82 \$cent/second per die. Assuming a test time of 6 seconds per die, the test cost will be \$0.23 per die. We attribute this test cost to a 100% fault coverage. Table I shows the relation between the fault coverage and die test cost [15] for the remaining considered fault coverage values. In [13], the authors estimate a test time of 80 μs to test 10000 TSVs using active probing. Hence, we ignore the test cost for pre-bond TSV test. We assume a pre-bond TSV fault coverage of 100%.

For the interconnects between the die, a test cost ratio of 1:100 with respect to the die cost is assumed (as in [16]). For the interconnects a fault coverage of 100% is assumed as well.

For the fab-less company B, the fault coverage for the dies are fixed to 100%, as we assume that KGD contracts exist between the involved fabs. For the IDM company A, the fault coverage can be flexible. Nevertheless, we assume the fault coverage in the post-bond and final-test to be 100% to prevent faulty ICs to be packaged and guarantee the final product quality.

Logistics cost: As discussed in Section II-A, there are many costs related to the transportation of tiers during the production of 3D-SICs. As company A has all resources in house, we assume the logistics cost to be null. For company B, these logistics are defined by arrows A, B, C, D, E, F and G; see Figure 3. We assume the price to move a single wafer between the involved fabs to be to 1% the manufacturing cost of a single wafer (i.e., for each of the involved arrows in the figure), regardless of the stack size.

Packaging cost: The packaging cost for 3D SICs used in our model is based on oral conversations with Boschman BV [25] and DIMES [26]. The costs are comprehensive and include machine,

TABLE II

FAULT COVERAGE FOR DIFFERENT TEST FLOWS

	Test Flow number											
	1	2	3	4	5	6	7	8	9	10	11	12
pre-bond	100	100	100	95	95	95	85	85	85	75	75	75
mid-bond	100	85	0	100	85	0	100	85	0	100	85	0

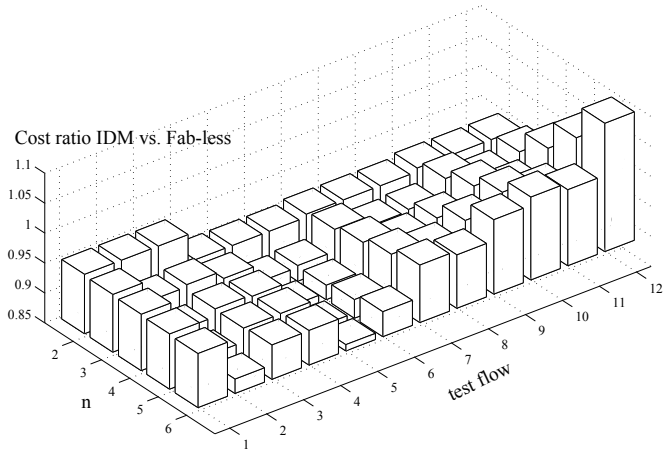

Fig. 6. Impact of variable stack size.

maintenance, labor and material cost. The packaging costs are assumed to be the same for both companies A and B. We assume a 100% packaging yield for both companies as this affects them in the same way.

B. Experiments performed

We compare the cost of producing a 3D-SIC by IDM company A and fab-less company B by performing the following three experiments:

1) **Impact of variable stack size**: The experiment considers a stack size $2 \leq n \leq 6$.
2) **Impact of variable die yield**: The experiment considers a die yield $0.6 \leq Y_d \leq 0.9$.
3) **Impact of variable stack yield**: The experiment considers an interconnect yield $0.91 \leq Y_{INT} \leq 0.99$, and a stacked-die yield $0.91 \leq Y_d \leq 0.99$.

Each experiment is performed for 12 test flows shown in Table II; each test flow consists of the following tests:

1) Pre-bond tests: For the IDM company A, we assumed tests with variable fault coverage for pre-bond testing; see Table II; for example, for test flow 4 we assumed FC=95%. However, for fab-less company B the fault coverage for pre-bond tests is fixed to 100%, as we assume that KGD contracts exist.
2) Mid-bond tests: For the IDM company A, we assumed tests with variable FC for mid-bond testing; see Table II; for example, for test flows 3, 6 and 9 have no mid-bond test at all while test flows 2, 5, 8, 11 have FC=85%. Also here, for fab-less company B the fault coverage for mid-bond tests is fixed to 100%.
3) Post-bond and final tests: The FC for these tests is assumed to be 100% for both companies to prevent faulty ICs to be packaged and guarantee the final product quality.

It is worth noting that company A can use any of the 12 test flows while company B can only use test flow 1. However, even if both companies use test flow 1, there is still a difference in the overall cost e.g., due to the logistics cost for company B.

C. Simulation Results

Below the results of the three performed experiments are given.

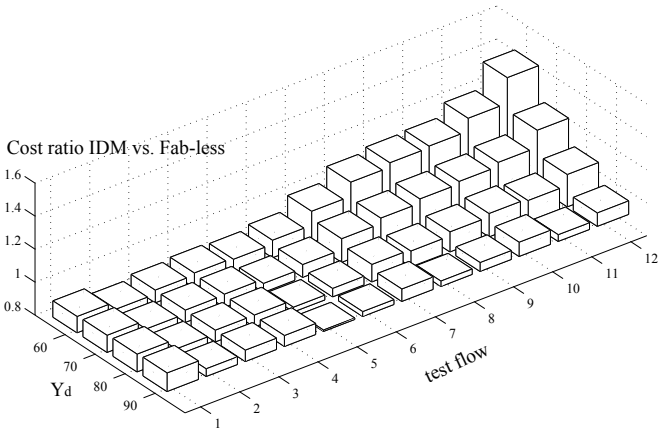

Fig. 7. Impact of variable die yield.

Impact of variable stack size: Figure 6 depicts the relative cost of producing a 3D-SIC by the IDM company A as compared with that of the fab-less company B for the 12 test flows for stack sizes $2 \leq n \leq 6$; the cost is normalized to the overall 3D cost of the fab-less company B. Note that the 12 test flows apply only to the IDM company; for the fab-less company only one test flow is used (for each stack size) which is similar to test flow 1 but with additional logistics cost. Inspecting Figure 6 reveals the following conclusions.

- Depending on the stack size and the chosen test flow, the overall cost of 3D-SIC for IDM can be either higher or lower than that of the fab-less company.
- For a given stack size, the overall cost can be optimized by choosing appropriate test flow combined with appropriate pre-bond and mid-bond fault coverage. For example, for n=3, 4, 5 or 6, the cost is optimal when using test flow 5 with a pre-bond fault coverage of 95% and a mid-bond fault coverage of 85%. A cost reduction of 12% can be obtained for a stack size n=6.
- Having a pre-bond fault coverage of 100% does not always results in optimal overall cost. In our case, the optimal cost is realized for a pre-bond fault coverage of 95%.
- Having a mid-bond fault coverage of 100% or a fault coverage of 0% does not always results in optimal overall cost. In our case, the optimal cost is realized for a mid-bond fault coverage of 85%.

Impact of variable die yield: Figure 7 shows the normalized cost of a 3D-SIC produced by the IDM company A with respect to the fab-less company B for the 12 test flows for variable die yield $60\% \leq Y_d \leq 90\%$. Inspecting the figure 6 reveals the following conclusions.

- Depending on the die yield and the chosen test flow, the overall cost of 3D-SIC for IDM can be either higher or lower than that of the fab-less company.
- The optimal test flow is die yield dependent. For example, in case the die yield equals 70% or lower test flow 2 performs best. However, for higher die yields (80% and higher) test flow 5 peforms best.
- Choosing appropriate values for the pre-bond and mid-bond fault coverage that leads to optimal costs reduction is die yield dependent.

Impact of variable stack yield: Figures 8 and 9 depict the relative cost of a 3D-SIC produced by the IDM company A as compared to that of the fab-less company B for the 12 test flows for variable stacked die yield $91\% \leq Y_{SD} \leq 99\%$ and variable interconnect yield $91\% \leq Y_{INT} \leq 99\%$ respectively. Inspecting Figure 8 reveals the following conclusions.

- Depending on the stacked-die yield and the chosen test flow,

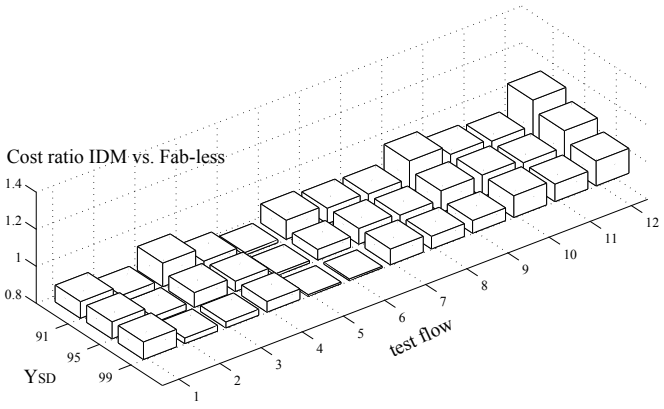

Fig. 8. Impact of variable stacked-die yield.

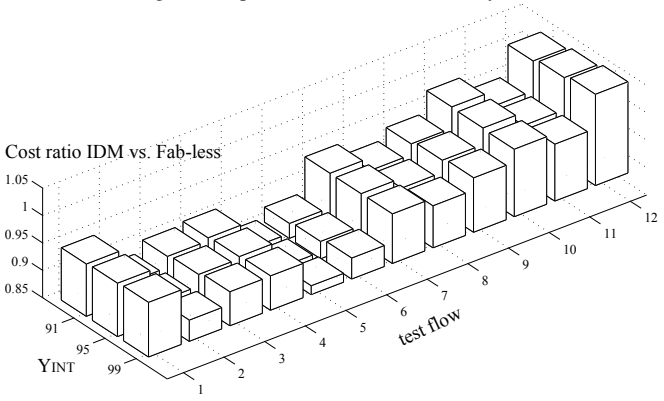

Fig. 9. Impact of variable interconnect yield.

the overall cost of 3D-SIC for IDM can be either higher or lower than that of the fab-less company.

- For this experiment, test flow 5 always results in overall optimal 3D-SIC cost. Note that the considered stacked-die yield is considered to be larger than 91%.

Figure 9 reveals the following conclusions.

- Depending on the stacked-die yield and the selected test flow, the overall cost of 3D-SIC for IDM can be either higher or lower than that of the fab-less company.
- The impact of the interconnect yield for considered values is very marginal; this is because the FC of the interconnects is set to 100%.
- Also for this experiment, test flow 5 always results in overall optimal 3D-SIC cost. Note that the considered interconnect yield is considered to be larger than 91%.

The results of these experiments clearly show that optimizing the overall/test cost is a complex task; it strongly depends on the test flow, FC of each test, different yield components, etc. Therefore using a tool, such as 3D-COSTAR, is extremely important to make appropriate trade-offs at an early stage in the design and optimize overall cost.

V. Conclusion

In this paper, 3D-COSTAR, a tool was introduced that can be used to evaluate different test flows for 3D-SICs; the tool consider all costs involved in the production (including design, manufacturing, testing, packaging and logistic) and produces the overall cost as well as the cost breakdown.

The case study presented in the paper showed the significant importance of using such a tool in order to make appropriate trade-offs for overall cost optimization. For example, the simulation results showed that when appropriate test strategies (test flow and fault coverage) are used for given design and manufacturing parameters, the overall cost can be reduced for IDMs with up to 20% as compared to fab-less companies. Therefore, tools like 3D-COSTAR are necessary for 3D-SIC cost optimization.

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