BTI Impact on Logical Gates in Nano-scale CMOS Technology

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Abstract—As semiconductor manufacturing has entered into the nanoscale era, Bias Temperature Instability (BTI) -Negative BTI (NBTI) in PMOS transistors and Positive BTI (PBTI) in NMOS transistors- has become one of the most serious aging mechanisms that reduces reliability of logic gates. This paper presents a simulation-based BTI analysis in both basic (such as NAND and NOR) and complex gates while considering the impact of input's duty cycle, the frequency at which they change, as well as the impact of the stressed transistor location. The simulation results show that the impact of BTI is strongly gate dependent and that in general the impact in complex gates is larger. When considering both NBTI and PBTI for basic gates, the results reveal that for a NOR gate the impact of NBTI is 2.19× higher than that of PBTI; while for a NAND gate, PBTI impact is 1.27× higher than that of NBTI. When considering different input duty cycles and their frequencies, the results show that the higher the duty cycle, the lower NBTI impact and the higher the PBTI impact regardless of the gate types and the frequency; a variation of ±30% duty cycle causes a variation of up to 49% variation in the impact of NBTI and a variation of 16% in the impact of PBTI. For complex gates, the results show similar trends, but with higher impact.

Index Terms—: NBTI, PBTI, Complex gates, duty cycle, frequency, stress location

I. INTRODUCTION

CMOS technology miniaturization has continued unabated for more than 30 years. The miniaturization resulted in higher IC performance and density; however, it has caused reliability issues in the scaled technologies [1]. Among the reliability issues, Bias Temperature Instability (BTI) has drawn attention that degrades the performance of the MOS transistors during "ON" states at elevated temperatures [2]. The impacts of BTI on MOS transistors include threshold voltage increment and current reduction leading to performance degradation [3,5,7].

BTI degradation originates from several electro-chemical sub-processes in the MOS transistors having high-κ [3], pure silicon dioxide (SiO_2), plasma nitrided or thermally nitrided dielectric layers [8]. These sub-processes take place during the transistor "ON" state and produce charges at the Si-SiO_2 interface [3,5]. These charges cause a transistor threshold voltage shift and consequently an additional gate delay. A unique property of BTI is annealing of the charges at the Si-SiO_2 interface during the transistor "OFF" state. The charge annealing reduces the threshold voltage shift and results in a lower additional delay. Therefore, depending on the ON/OFF ratio (which is referred to as *activity factor*) of the transistors, the gate will suffer from variable additional delays.

In recent years, there is an escalation of interest in BTI analysis at the gate level [10–15]. Paul et al. in [10] pioneered the work by performing NBTI analysis for the continuous inputs that resulted in the worst degradation and Haldun et al. in [11] carried out the analysis for a modified model. Kumar et al. in [12] and Khan et al. in [13] presented NBTI analysis for dynamic inputs. Luo et al. in [14] analyzed NBTI in the gates by considering stacking effect and Rakesh et al. in [15] introduced various process and design parameters in the analysis. All these analyses assume that all transistors in a gate have the same activity factor and contribute *uniformly* to gate delays. These approaches suffer from the very fundamental limitations as the authors have not yet investigated: (a) the organization of the transistors in a gate, (b) the interference among BTI in different transistors, (c) the workload dependency (based on activity factor e.g.) and (d) the location of the affected transistor in the gate. One recent exception for (a)-(c) is Kaczer et al. work in [21] but they only analyzed simple inverter and not extended the analysis to the other gates. Moreover, the published work focuses mainly on simple gates such as NAND, NOR, etc. However, the impact on the complex gates could be significantly different. Hence, it is vital to analyze BTI in gates that addresses all the above limitations.

This paper presents a simulation-based BTI analysis for basic and complex gates. Main contributions of the paper are:

- Incorporate both NBTI and PBTI in simulation for accurate BTI evaluation in the basic gates
- Investigate the impacts of BTI in basic gates while considering inputs with different duty cycles and frequencies. In addition, the contribution of BTI in each transistor within the gate to the overall impact is explored
- Analyze BTI in the complex gates and compare the results with those obtained for the basic gates

The rest of the paper is organized as follows: Section II presents BTI mechanisms along with a brief overview of a BTI model. Section III-A presents a model for BTI induced gate delay and a framework for BTI analysis. Section IV presents BTI analysis in the basic gates. Section V analyzes BTI in complex gates. Finally, Section VI concludes the paper.
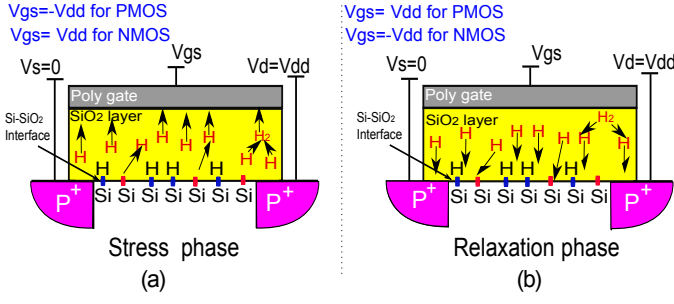
Fig. 1. Schematic view of (a) Stress phase: Si-H bond breaking, H and H_2 diffusions toward poly gate (b) Relaxation phase: H and H_2 diffusions toward the Si-SiO$_2$ interface and $\equiv$Si- bond recovery

II. BACKGROUND

This section explains BTI mechanism that takes place inside MOS transistors. Thereafter, it reviews a well known model that relates BTI mechanism to the threshold voltage increment.

A. BTI Mechanism

BTI causes threshold voltage (V_{th}) increments to the MOS transistors. V_{th} increment in a PMOS transistor that occurs under the *negative* gate stress is referred to as NBTI, and the one that occur in an NMOS transistor under *positive* gate stress is known as PBTI. Zafar et al. in [3] have carried out a comparative analysis of NBTI and PBTI impacts in MOS transistors; they concluded that either NBTI or PBTI can become more significant depending on the dielectric type.

For a MOS transistor, there are two BTI phases, i.e., the stress phase (see Fig. 1(a)) and the relaxation phase (see Fig. 1(b)). These two phases differ by the gate biasing (i.e., V_{dd} or -V_{dd}) of the MOS transistors.

Stress Phase

In the stress phase, the Silicon Hydrogen bonds ($\equiv$Si-H) breaking takes place at the Silicon-Silicon dioxide (Si-SiO$_2$) interface as shown in Fig. 1(a). The broken Silicon bonds ($\equiv$Si-) trap at the Si-SiO$_2$ interface thus known as interface traps and the released H atoms/molecules diffuse toward the poly gate. The *number of interface traps (N_{IT})* depends on $\equiv$Si-H bond breaking rate (k_f), H and H_2 diffusion rates (D_H and D_{H_2}), and $\equiv$Si- bond recovery rate (k_r). The overall process has been described by the reaction-diffusion (RD) model [5].

Relaxation Phase

In the relaxation phase, there is no $\equiv$Si-H breaking and H or H_2 diffusions towards the poly gate as shown in Fig. 1(b). However, H atoms/molecules diffuse back towards the Si-SiO$_2$ interface and anneal the $\equiv$Si- bonds. The annealing process reduces N_{IT} at the Si-SiO$_2$ interface and reduces the degradation caused during the stress phase.

B. BTI Model

In recent years, researchers are putting more efforts to analyze BTI mechanism that takes place inside the MOS transistors [3,5,6,21]. Kaczer et al. of [6,21] have recently developed a more complete model of the transistor level of NBTI. But this model is not yet available at the time of our work, and in [6,21] no higher level modeling has been proposed. Alam et al. in [5] have modeled the overall dynamics of NBTI as a Reaction Diffusion (RD) process. The model is usable at a higher level such as gate level. Because this work analyze BTI at the gate level, model of [5] will be used.

The model relates N_{IT} generated during the stress phase with the time (t) as follows:

$$N_{IT}(t) = \left(\frac{k_f.N_o}{k_r} \right)^{2/3} . \left(\frac{k_H}{k_{H_2}} \right)^{1/3} .(6.D_{H_2}.t)^{1/6}, \quad (1)$$

where N_o, k_H, and k_{H_2}, represent initial bond density, H to H_2 conversion rate, and H_2 to H conversion rate inside SiO$_2$ layer, respectively.

The number of interface traps that *do not* anneal during the relaxation phase is given by [12]:

$$N_{IT}(t_o + t_r) = \frac{N_{IT}(t_o)}{1 + \sqrt{\frac{\xi.t_r}{t_o + t_r}}} \quad (2)$$

where $N_{IT}(t_o)$ is the number of interface traps at the start of the relaxation phase, ξ is the diffusion coefficient during the relaxation with a value ξ=0.5 [12], t_o is the input period and t_r is the relaxation duration.

Interface traps at the Si-SiO$_2$ interface oppose the applied gate stress resulting in the threshold voltage increment (ΔV_{th}). The relation between N_{IT} and ΔV_{th} is given by:

$$\Delta V_{th} = (1 + m).\chi.q.N_{IT}/C_{ox}, \quad (3)$$

where m, q, and C_{ox} are the holes/mobility degradation that contribute to the V_{th} increment [7], electron charge, and oxide capacitance, respectively. Additionally, χ is a BTI coefficient with a value χ=1 for NBTI and χ=0.5 for PBTI [22].

III. GATE DELAY ANALYSIS

This section presents a gate delay model for BTI induced degradation and a framework for analyzing BTI in the gates.

A. Gate Delay Model

BTI induced ΔV_{th} of each MOS transistor has its contribution to the additional gate delay [13]. A generalized formula that relate BTI induced ΔV_{th} in a transistor to the additional delay is given by [10]:

$$\Delta D = \gamma.\frac{n.\Delta V_{th}}{(V_{gs} - V_{th})} \quad (4)$$

where n is the velocity saturation index and γ represents the stress duration with respect to the total input period (i.e., *activity factor*) of the transistor. The γ dependence of the contribution to the delay reveals that transistors in a gate having different stress and relaxation phases will suffer from

different degradations, resulting in variable contribution to the delay.

Sakuri et al. in [19] suggested that the gate output rise and fall transition times depend on the V_{th} of the PMOS and NMOS transistors, respectively. Since NBTI causes ΔV_{th} to PMOS transistor and PBTI causes ΔV_{th} to NMOS transistor; therefore, analysis in this paper considers the gate rise and falling transition times for estimating NBTI and PBTI impacts, respectively. This consideration isolates BTI impacts of NMOS and PMOS transistors in a gate.

B. BTI Analysis Framework

The analysis presented in this paper addresses both NBTI and PBTI impacts in the gates. For this analysis, a framework shown in Fig. 2 has been developed. The right side of the figure is used for degradation free simulation of the gates and the left side simulate BTI impact in the gates. For degradation free case, the gates are synthesized using 45nm PTM transistor models and simulated using HSPICE to get a reference for the performance metrics. Thereafter, Verilog-A modules are added to each transistor to get BTI augmented gates. Depending on biasing input of each transistor, the Verilog-A module produce ΔV_{th} that binds BTI impact to the additional gate delay (ΔD).
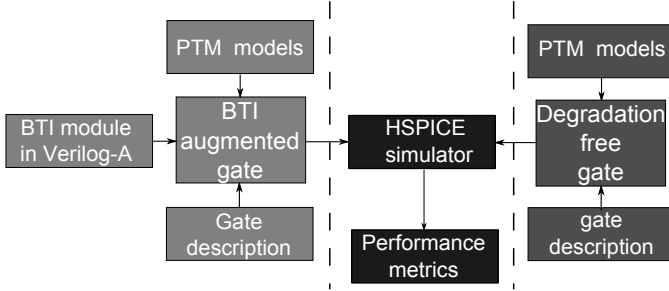
Fig. 2.   Schematics of the BTI analysis framework

The framework is used for analyzing BTI impacts in MOS transistors of an inverter. It is assumed that process variations and the other failure mechanisms, e.g. Hot Carrier Degradation and Electro-migrations produce complementary additive effects so in our analysis we do not incorporate them yet. Throughout the analysis, the input has γ=50% and BTI parameters used in Verilog-A module to get ΔV_{th} are, k_f= $8\times10^{-4}s^{-1}$, k_r=$3\times10^{-18}cm^3s^{-1}$, N_o= $5\times10^{16}cm^2$, and D_{H2}=$4\times10^{-21}cm^2s^{-1}$ [11]. Fig. 3(a) gives the ΔV_{th} increments of MOS transistors due to BTI; it shows that ΔV_{th} due to NBTI and PBTI approach 53.16mV and 28.08mV, respectively, after 10 years of operation. The curves follows the $t^{1/6}$ trend of Eq. 1 and have a good match with the silicon results presented in [3,4]. The ΔV_{th} is inserted into Eq. 4 to get ΔD. Fig. 3(b) shows ΔD, i.e., the percentage increment of the delay that approach 20.07% and 8.73% due to NBTI and PBTI, respectively. Therefore, it can be concluded that for a given input, (e.g., γ=50%) NBTI impact in PMOS transistors is more significant and approaches up to 2.30× the PBTI impact in NMOS transistors.
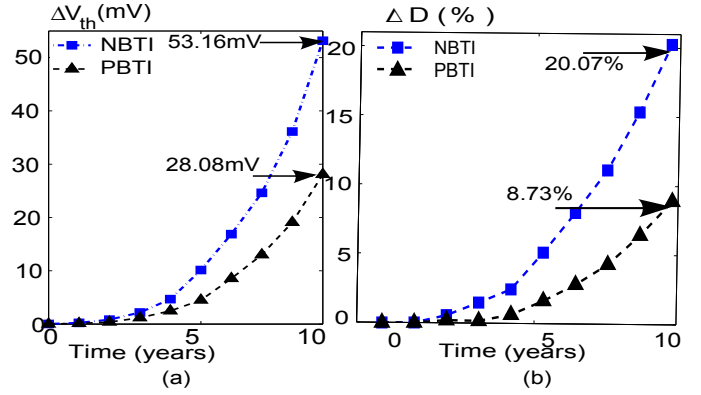
Fig. 3.   (a) BTI induced (ΔV_{th}) increment of PMOS and NMOS transistors as a function of time (b) Inverter delays ΔD increment due to NBTI and PBTI

IV. BTI IMPACTS IN BASIC GATES

This section analyzes BTI impacts in some basic gates, such as NAND and NOR gates. Initially, it analyzes BTI dependence on transistor organizations in the gates. Thereafter, it analyzes BTI dependence on some timing parameters such as; duty cycle, frequency and stress location.

A. Transistor organization Dependency

The analysis of BTI impact presented in this paper is inspired by the observation that all MOS transistors in a gate do not contribute *uniformly* to the delay increment. We argue that MOS transistors connected in series have positive interference in their BTI impacts and result in a larger delay increment. On the other hand, MOS transistors connected in parallel have mutually exclusive BTI impacts that result in smaller delay increment. To justify the argument, two basic gates -NAND and NOR- are analyzed for γ=50% at the inputs.

NAND gate

Let us consider a two inputs NAND gate shown in Fig. 4(a). The gate consists of two NMOS transistors (N_1 and
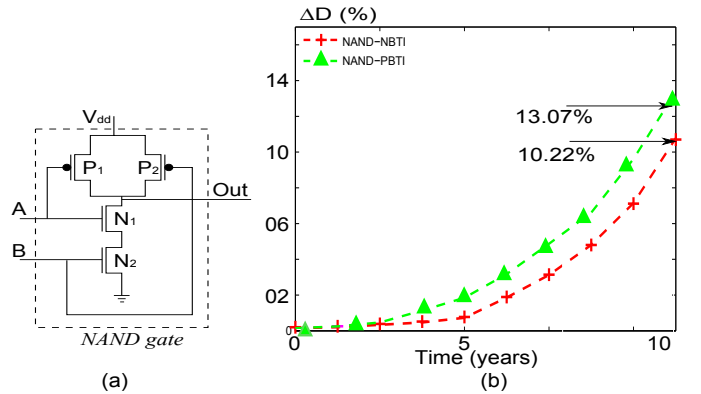
Fig. 4.   (a) Transistor organization in a NAND gate (b) Percent delays of NAND gate due to NBTI and PBTI
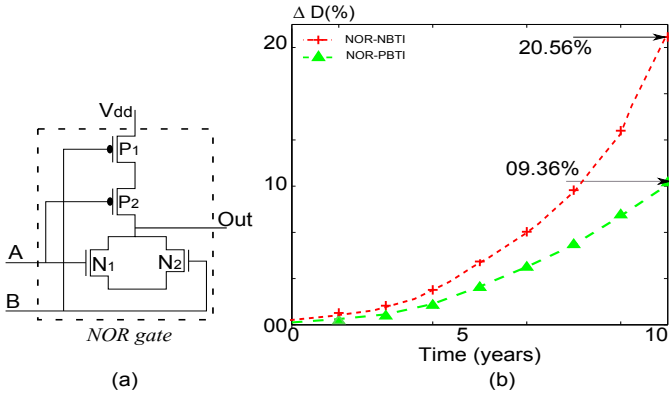
Fig. 5. (a) Transistor organization in a NOR gate (b) Percent delays of NOR gate due to NBTI and PBTI
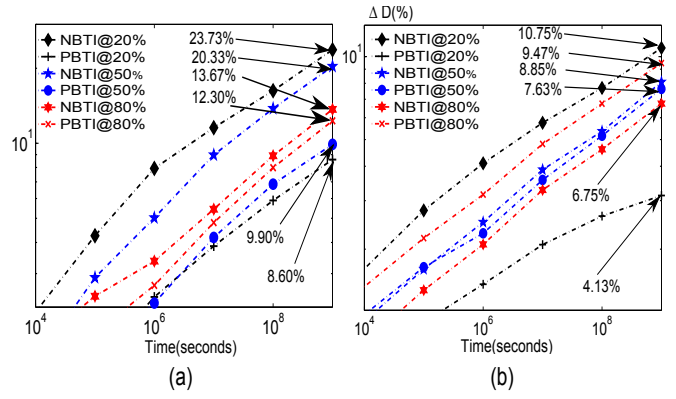

Fig. 6. (a) Percent delay increments of NOR due to NBTI and PBTI at 20%, 50% and 80% input duty cycles (b) Percent delay increments of NAND due to NBTI and PBTI at 20%, 50% and 80% input duty cycles

N_2) connected in series, as well as two PMOS transistors (P_1 and P_2) connected in parallel. The gate is analyzed using the framework mentioned in the previous section; the simulation results are shown in Fig. 4(b). Analysis of the results reveal that PBTI impact on the serially connected NMOS transistors agglomerates and causes about 13.07% additional delay. On the other hand, NBTI impact in the parallel connected PMOS transistors have mutually exclusive impacts and cause only up to 10.22% additional delay.

Therefore, it can be concluded that PBTI impact dominates in NAND gate and is up to 1.27× the NBTI impact.

NOR gate

To strengthen the claim of BTI dependence on transistor organization, a two inputs NOR gate shown in Fig. 5(a) is considered. The gate consists of two serially connected PMOS transistors (P_1 and P_2) as well as two parallel connected NMOS transistors (N_1 and N_2). The gate is analyzed using the framework and the results are shown in Fig. 5(b). It shows that NBTI impact in the serially connected PMOS transistors amasses to cause up to 20.56% additional delay, while PBTI impact in the parallel connected transistors can only cause 9.36% additional delay.

Therefore, it can be concluded that NBTI impact dominates in NOR gate and is up to 2.19× higher than the PBTI impact. We can conclude that opposite effects are present for NBTI/PBTI ratio depending on the transistor topology.

B. Timing Dependency

In addition to the dependency on transistor organization inside a gate, BTI has a strong dependence on the gate inputs. This section presents the impacts of three input parameters such as; duty cycle, stress location and frequency on BTI.

Duty cycle dependence

Duty cycle is defined as the percentage of a period that the inputs of a gate remains high. Note that *high* and *low* inputs cause stress and recovery phases to the NMOS transistors, respectively; it cause reverse phases to the PMOS transistors. Since stress and relaxation phases have symmetric processes

(i.e., ≡Si-H bond breaking and recovery), the dominance of one over the other is determined by stress and relaxation phase durations.

The two basic gates -NOR and NAND- are analyzed under three duty cycles -20%, 50%, and 80%- to evaluate the BTI impact. Fig. 6(a) shows the BTI induced delay increments in NOR gate under the three duty cycles. The figure shows that variation in the duty cycle has a significant impact on the BTI induced delays. For example, at 50% duty cycle in NOR gate, NBTI and PBTI cause 20.33% and 9.90% additional delays, respectively. However, at 20% duty cycle, the additional delay due to NBTI increases to 23.73%, which is 1.20× the 50% duty cycle case; while the delay due to PBTI becomes only 8.60%, which is 0.85× the 50% duty cycle case. However, it is observed that at 80% duty cycle, NBTI brings only 13.67% additional delay while PBTI causes 12.30% additinal delay. Similar, analyses are carried for a NAND gate and results are shown in Fig. 6(b).

It can be concluded, at lower duty cycles, NBTI is more significant than PBTI on the gates. However, higher duty cycles magnify PBTI and diminish NBTI impacts on the gates.

Frequency Dependence

Currently, there is no clear explanation of BTI dependence on frequency at the transistor level. Alam et al., in [5] have claimed frequency independence due to equivalent number of Si-H bond breaking and annealing during stress and relaxation phases, respectively. While Tibor et al., in [9] suggested weak frequency due to asymmetry between the bonds breaking and recovery during stress-recovery phases . Fig. 7(a), based on the model presented in Eq. 1 and Eq. 2, shows the BTI analysis of NAND gate at different frequencies (i.e., 333.33, 166.66 and 83.33 MHz) but identical duty cycles. The figure shows that the BTI -both NBTI and PBTI- induced delays are close the nominal values even with 4× variation in the frequency. Fig. 7(b) shows similar observation for a NOR gate. The figure shows that 4× variation in frequency brings negligible variation to the NBTI and PBTI impacts on NOR gate.
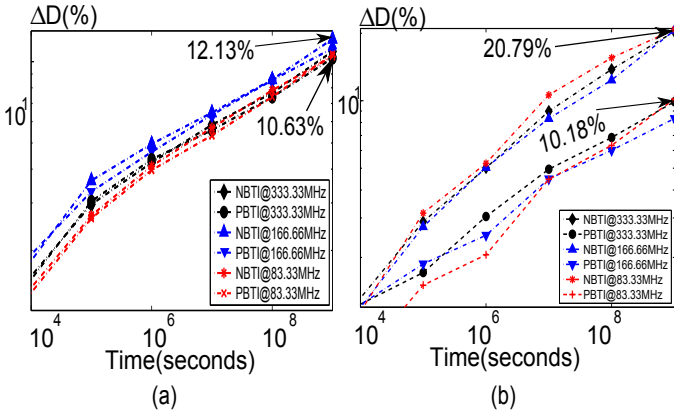
Fig. 7. (a) NBTI and PBTI induced delays in a NAND gate at different frequencies and identical duty cycles (b) NBTI and PBTI induced delays in a NOR gate at different frequencies and identical duty cycles

Therefore, it can be deduced that BTI is independent of the operating frequency. The analysis is consistent with the claim of frequency independence presented in [5].

Stress Location Dependence

Majority of the published literature estimated BTI impact with the assumption that a given ΔV_{th} in any transistor contribute *uniformly* to delay increment of the gate. However, in reality, the contribution to the delay increment depends on the location of the stressed transistor. We claim that for a given ΔV_{th} in a transistor closer to V_{dd}, the contribution to the delay increment is lower. Conversely, the same ΔV_{th} in a transistor closer the ground has higher contribution to the delay increment.

The stress location dependency is analyzed in the two basic gates. Fig. 8(a) shows the delay increment due to PBTI induced ΔV_{th} in N_1 and N_2 of Fig. 4(a). The figure shows that ΔV_{th} in N_1 causes 3.10% to the gate. However, the same ΔV_{th} in N_2 causes 5.62% delay increment. The higher contribution to the delay increment can be contributed to the lower driving potential at the source of N_2 due to drop in N_1. Similarly, Fig. 8(b) shows the difference in delay increment due to NBTI induced ΔV_{th} in P_1 and P_2 of Fig. 5(a); which

shows that NBTI in P_2 causes 17.14% delay increment, while NBTI in P_1 causes only 13.61% delay increment.

V. BTI IMPACTS IN COMPLEX GATES

This section analyzes BTI impacts in the complex gates. Initially, it explores BTI in some complex gates and then investigates its timing dependencies.

A. Transistor Organization Dependency

Complex gates realize complex logic functions using suitable MOS transistors configuration. Due to these transistors configurations, exact estimation of BTI impacts in complex gates is more challenging.

As an example case, the logic function $\overline{(A.(B+C)+D.E)}$ is implemented by the transistor configuration show in Fig. 9(a). The gate has at most three serially connected PMOS transistors (P_2, P_3, P_5) and two NMOS transistors (N_1, N_2 or N_4, N_5). The gate is analyzed using the framework of Section III-A and the results are shown in Fig. 9(b). The figure reveals that under the worst case -P_2, P_3, P_5- are under stress, NBTI impact -21.56% additional delay- is about $2.85\times$ the PBTI impact -7.59% additional delay-. The higher difference in the impacts can be attributed to the accumulative nature of the NBTI impact on the three serially connected PMOS transistors.
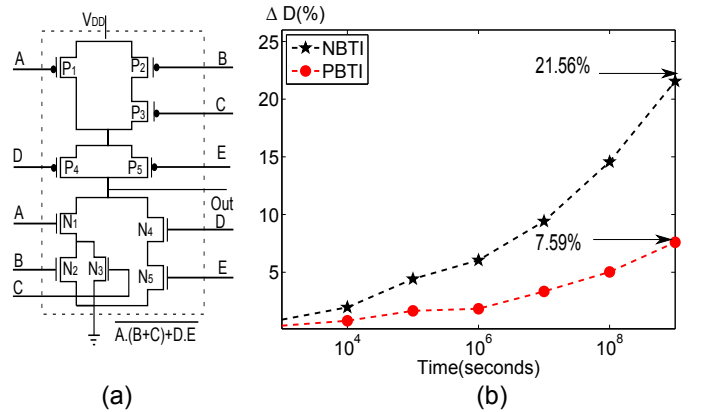
Fig. 9. (a) Transistor organization in a complex gate implementing $\overline{A.(B+C)+D.E}$ function (b) Percent delay (rising and falling output transition time increment) of the complex gate due to NBTI and PBTI

Moreover, to extend BTI analysis in other complex gates. Table 1 shows analysis of two well known complex gates i.e. And-Or-Invert (AOI) and Or-And-Invert (OAI). The table

TABLE I
NBTI AND PBTI IMPACTS IN DIFFERENT GATES

Gate	Max. PMOS in series	Min. NMOS in series	$\Delta D_{NBTI}(\%)$	$\Delta D_{PBTI}(\%)$
AOI	3	1	23.60	7.61
OAI	3	2	21.24	13.76

AOI=And Or Invert, OAI= Or And Invert

shows that depending on the number of serially or parallel connected PMOS/NMOS transistors, the impact of NBTI/PBTI becomes more significant. We can conclude that series and parallel connected transistors determine the dominant impact. Additionally, the sizes need to be differently selected to enable delay balancing, and that influence the NBTI/PBTI impacts.
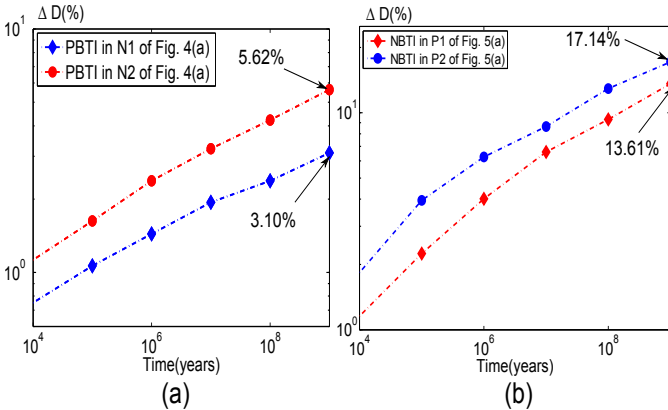

Fig. 8. (a) Percent delay increment of NAND gate due to PBTI induced ΔV_{th} in transistor N_1 and N_2 of Fig. 4a (b) Percent delay increment of NOR gate due to NBTI induced ΔV_{th} in transistor P_1 and P_2 of Fig. 5a
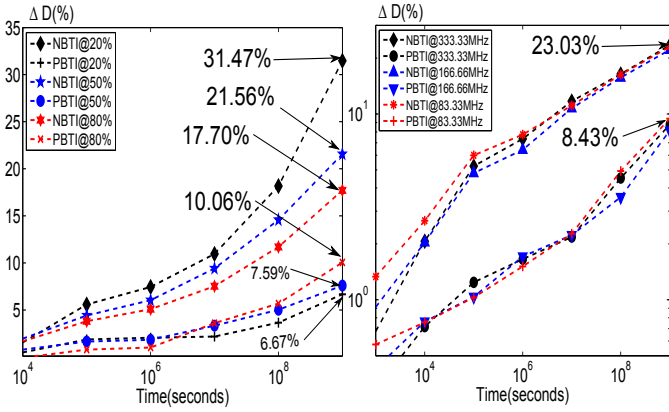
Fig. 10.   (a) Percent delay increments in the complex gate of Fig.9(a) at different duty cycles (b) Percent delay increments in the complex gate of Fig.9(a) at different frequencies

B. Timing dependency

Impacts of the three timing parameters are analyzed in the complex gate (see Fig. 9(a)). For duty cycle variation analysis, Fig 10(a) shows that NBTI induced delay increment reaches to 31.47% at 20% duty cycle. The increment is 45% higher than the 50% duty cycle case. Fig 10(b) shows BTI induced delay increment with the frequency variation and confirms our previous claim of the frequency independence.

The stress location dependency in pull-up network complex gate implementing $\overline{A.B + C.D + E}$, shown in Fig. 11(a) is analyzed. Initially, NBTI is inserted in P_1 and P_2 and all the other PMOS transistors are degradation free. Simulation results under this condition is shown in Fig. 11(a), which shows that NBTI causes 6.41% delay increment. However, when NBTI only effects P_5 and all the other transistors are degradation free, the delay incremet reaches 14.75%. The 2.28× higher impact can be attributed to lower source voltage of P_5 due voltage drop in the upper PMOS transistors.

VI. CONCLUSION

This paper presented a BTI analysis in both basic and complex gates. First, the transistor level analysis revealed that NBTI causes 2.30× more degradation to the PMOS transistors than PBTI causes to the NMOS transistors. Second,

considering transistor organization in gates showed that NBTI impact is more significant in NOR gates and PBTI brings more degradation to the NAND gates. Third, inputs timing dependencies of BTI showed; (a) input duty cycle has a significant impact on NBTI or PBTI dominance in a gate,(b) BTI is frequency independent, and (c) location of the stressed transistor causes a significant variation to the BTI impact on the gates.

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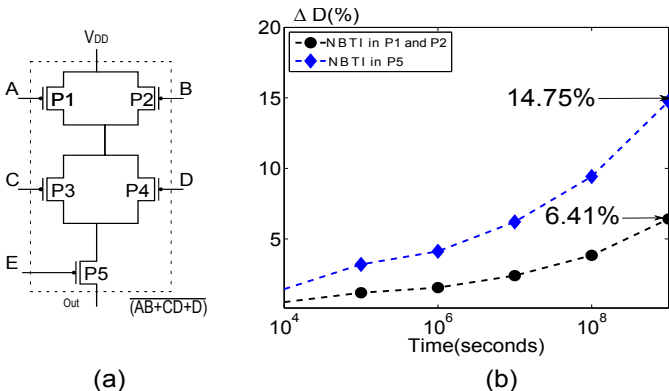
Fig. 11.   (a) Transistor organization in pull-up network of complex gate implementing $\overline{A.B + C.D + E}$ function (b) Percent increment in rising transition time due to NBTI