A Direct Measurement Scheme of Amalgamated Aging Effects with Novel On-Chip Sensor

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***Abstract*—Aggressive technology scaling has led to a significant reduction of device reliability. As a consequence Integrated Circuits (ICs) reliability became a major issue and Dynamic Reliability Management (DRM) schemes have been proposed to assure ICs' lifetime reliability. Though, up to date, various aging sensors have been proposed, few of them can provide real quantitative aging measurements. In view of this, we propose a direct measuring scheme by using the drain current as aging indicator. We designed a novel on-chip aging sensor able to detect the amalgamated aging effects of ICs caused by joint failure mechanisms. This is achieved by detecting the peak power supply current (I_{pp}) degradation from the device and/or circuit, which is a signature of the total drain current. Unlike the existing aging sensors which indirectly estimate the aging status of a device, the proposed sensor allows for direct aging assessment for single device and/or circuit blocks. Simulation results using the TSMC 65nm technology indicate that the proposed sensor can operate at 1GHz. Accelerated test simulation in Cadence for a set of $ISCAS85$ benchmark circuits indicates that the drain current exhibits a similar aging rate as the threshold voltage for the entire circuit lifetime, but with a better sensitivity towards the End-of-Life (EOL), which demonstrates the validity and practical relevance of the proposed aging monitoring framework.**

***Index Terms*—Dynamic Reliability Management, Aging, Process Variation.**

I. Introduction

As technology is continuously scaling down to achieve higher performance and integration density, transistor reliability is becoming a rising concern. Transistors suffer multiple degradations concurrently under normal operating conditions, e.g., Negative Bias Temperature Instability (NBTI), Hot Carrier Injection (HCI), and Time-Dependent Dielectric Breakdown (TDDB). Due to these failure mechanisms, the device performance degrades and failure might occur during device's expected operational lifetime [15], [9]. The slowly progressive performance degradation is known as "aging", which is reflected in the degradation of threshold voltage, channel carrier mobility, gate-oxide capacitance, etc.

Usually, Integrated Circuits (ICs) lifetime requirements are mostly made based on worst-case assumptions, which leads to highly conservative margins on technology parameters, resulting in the under utilization of the technology potential. To make better use of the technological improvement the pessimistic assumption should be relaxed and combined with a Dynamic Reliability Management (DRM) framework that relies on online sensors to measure the ICs aging status. In the recent past, a number of approaches for aging/reliability monitoring have been reported. In [13], Kim et al. introduced an on-chip aging monitor for high resolution degradation measurements by detecting beat-frequency from a pair of ring oscillators. Keane et al. further extended this idea to an "all-in-one" sensor for BTI, HCI, and TDDB in [11]. Though high precision can be achieved by their circuitry, a large area overhead is required ($0.035mm^2$ in 130nm technology). Karl et al. proposed compact in-situ sensors for monitoring NBTI and TDDB, respectively, in [12]. These sensors work in the sub-threshold region with leakage current to increase the sensitivity. Even though they require a small area overhead these sensors are sensitive to process, voltage, and temperature variations. Agarwal et al. proposed aging sensor designs integrated inside a flip-flop to detect delay violation(s) in [4], [3]. These designs are relatively small and can be potentially included in many chip flip-flops. However, this kind of sensor can only check delay violation in a static or quasi-static time window ("guardband"), and thus no quantitative aging information can be collected.

Nevertheless, all these sensors above have a common shortage that they cannot provide a direct measurement of the real aging status of the Circuit Under Observation (CUO). Previous work can be divided into two groups: (1) sensors that use performance comparison of fresh and stressed devices to get aging information; and (2) sensors that use timing violation checking in a predefined "guardband". For the former group, the aging information is extracted from an additional stressed device, which is carefully placed to make it exposed to the same stressing environment as the CUO. Though high correlation can be achieved by a smart enough placement algorithm, such an approach increases the complexity and effort at design-time and still ends up with an indirect aging measurement. The latter group of sensors can detect the real aging of the CUO, however, they cannot give a quantitative measurement on aging, as mentioned in the above paragraph.

To overcome the common shortage of the existing sensors, in this paper we propose a novel online aging sensor able to directly measure the real circuit degradation under NBTI and HCI. The proposed sensor measures the CUO I_{pp} value and converts it into a Pulse-Width Modulated (PWM) signal. The I_{pp} value accurately reflects the aging information as its value is affected by the degradation of multiple aging sensitive device parameters such as the threshold voltage (V_{th}) and the carrier mobility (μ).

The major contributions of our work include:

- We derive the relationship between peak power supply current I_{pp} degradation and multiple failure mechanisms and demonstrate that it can accurately capture the effect of multiple aging mechanisms;
- We propose a novel aging sensor, which is capable of directly measuring the real IC aging status caused by the amalgamated effects of NBTI and HCI failure mechanisms;
- With a V_{th} sensor, only one transistor can be observed when the entire circuit is monitored with one sensor. The proposed method allows us to observe the entire circuit instead of a transistor, which substantially reduces the area overhead, alleviates the problem of finding the optimum location for the sensors and to extrapolate the overall circuit-level aging from the transistor-level aging;
- We evaluate our proposal by means of simulations. We utilized a set of $ISCAS85$ benchmark circuits to validate our choice of using the drain current to monitor their aging status. Simulation results indicate similar aging trends for both the drain current I_D and the threshol voltage V_{th}, but with the I_D exhibiting better sensitivity as the circuits approach their EOL.

The rest of the paper is organized as follows: Section 2 presents the aging model describing the relationship between the peak current value and the IC aging conditions under multiple failure mechanisms. In section 3, the direct aging measurement framework is presented, followed by the description of the I_{pp}-based sensor architecture and the corresponding performance evaluation. Section 4 validates experimentally the aging estimation accuracy and the feasibility of our proposal - using the drain current for direct aging monitoring. Section 5 concludes the paper with a summary of this work.

II. Model Development

In prior work, the threshold voltage (V_{th}) is the most common physical parameter selected as indicator of transistor aging progress. However, aging sensors based on V_{th} can only be used to monitor the aging status at transistor level. Thus, for circuit level aging measurements many such sensors are required. Moreover, sensor positioning and the extrapolation method that can bring aging information from transistor to circuit level are far from being trivial issues. Furthermore, V_{th} is hard to be extracted directly without interrupting circuits' normal function. As a result, all V_{th} based aging sensors make use of sacrificed devices in order to replicate the stress to which the circuit under observation is subjected to, leading to an indirect measurement. In order to measure the real aging status inside a circuit, we propose to use the power supply current (I_p) as aging indicator.

A. Power Supply Current in CMOS Logic

Power supply current I_p is the total drain current passing through the supply voltage terminals. Without loss of generality, we start to determine the relationship between I_p degradation and failure mechanisms on an inverter circuit.

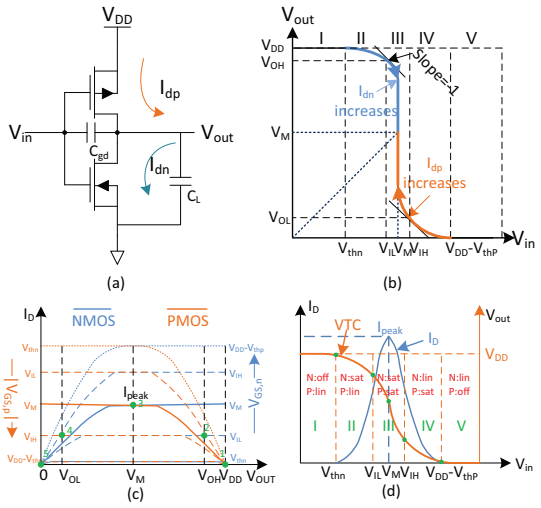

Fig. 1. Inverter peak current: (a) the circuit model; (b) VTC and the operating regions of PMOS, NMOS transistors; (c) intersections of the output characteristic curves of PMOS, NMOS transistors; (d) the peak power supply current and transistor operating regions.

The operating regions of each transistor during a low to high input transition (i.e., the input voltage switching from "0" to "1"), are graphically illustrated in Figure 1(d). During this progress, at some point ($V_{in} = V_{out} = V_M$), both transistors are saturated and the power supply current I_p reaches the maximum value I_{pp} because the V_{DS} values are equal for both transistors. Further increase of input voltage will make the NMOS enter the linear region and as a consequence the drain current I_D decrease until 0 (because the PMOS is switched-off by the gate overdrive voltage). The analysis is similar for the high to low input transition (when the input voltage changes from "1" to "0"). Summarizing, the current I_p reaches a peak I_{pp} during the input signal transition, when $V_{in} = V_{out}$.

The above analysis can be easily applied to more complex CMOS networks such as the general CMOS logic structure, depicted in Figure 2(a). The PMOS devices are equivalent to a pull-up network and the NMOS devices are equivalent to a pull-down network. Since the input vectors to the pull-up and the pull-down networks are complementary in CMOS logic, the working regions of pull-up and pull-downs networks shift oppositely during input signal transitions. Thus at some point, the I_p of the entire network will reach a peak I_{pp}. For the fresh (unaged) devices, this peak value is constant for a given input pattern, so the degradation of the peak current can be chosen as indicator for assessing the aging status inside any (large) CMOS logic network. Based on the above analysis and since the global I_{pp} is just a special case of I_D (i.e., when the total drain current from both the pull-up and the pull-down networks reaches its maximum), we can consider the peak power supply current as a signature of the drain current. Therefore, without loss of generality, in the next section we shall derive the aging model for I_{pp} using the drain current.

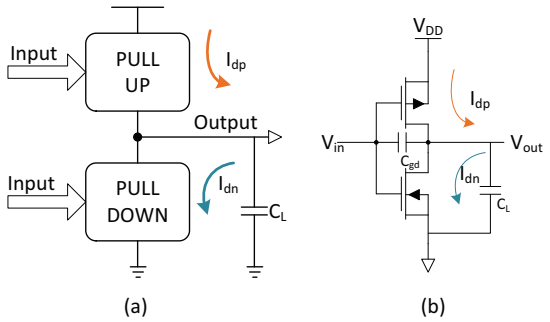

Fig. 2. Peak current of CMOS logic: (a) a general illustration of CMOS network; (b) Equivalent invert circuit for the pull-up network.

B. Aging Effects on Power Supply Current

Generally, the drain current in the saturation region can be expressed as:

$$I_{D_{sat}} = \mu C_{ox} \frac{W}{L} (V_{GS} - V_{th})^2. \tag{1}$$

A more general form of the drain current can be expressed as:

$$I_D = \mu C_{ox} \frac{W}{L} \left[(V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right]. \tag{2}$$

Equation (1) and (2) indicate the relationship between I_D and key device parameters, such as the mobility μ, the device threshold voltage V_{th}, and the oxide capacitance C_{ox}, which are degrading under joint NBTI and HCI induced stress. The peak power supply current is a special case of I_D, i.e., the I_D value which is equal in both the pull-up and the pull-down network. Therefore, as far as aging effects caused by amalgamated wearout mechanisms are concerned, I_{pp} follows the same rule as I_D does.

NBTI is an intrinsic front-end-of-line wearout mechanism which occurs in PMOS transistors mainly when the gate is subjected to a negative input voltage. The NBTI-induced I_D damage includes trap generation at the channel-dielectric interface and as well as inside the bulk of the dielectric. Consequently, the threshold voltage V_{th} shifts and channel mobility μ degrades due to the trap generation. The V_{th} degradation induced by NBTI can be expressed by:

$$\Delta V_{th} = \frac{q \Delta N}{C_{ox}}, \tag{3}$$

where q is the electron charge and ΔN is the total trap density generated by NBTI. The mobility degradation can be described by the following equation [6]:

$$\mu = \frac{\mu_0}{1 + \alpha \Delta N}, \tag{4}$$

where μ_0 is the original channel mobility, α is a process-dependent constant, and $\alpha \approx 2.4 \times 10^{-12} cm^2$[14]. For small ΔN, using $\Delta \mu = \mu_0 - \mu$, the channel mobility degradation can then be estimated by:

$$\frac{\Delta \mu}{\mu} = \frac{\Delta N}{1 + \alpha \Delta N} \approx \alpha \Delta N. \tag{5}$$

Assuming the threshold voltage shift and channel mobility degradation are independent progresses, then the change of I_D can be expressed as:

$$\Delta I_D = \frac{\partial I_D}{\partial V_{th}} \Delta V_{th} + \frac{\partial I_D}{\partial \mu} \Delta \mu. \tag{6}$$

Since the NBTI stress happens when PMOS is in saturation mode, applying the above equation to Eq.(1), yields:

$$\Delta I_D = \frac{I_{D0}}{(V_{GS} - Vth - V_{DS}/2)} \Delta V_{th} + \frac{I_{D0}}{\mu_0} \Delta \mu. \tag{7}$$

Generally, $V_{DS} \approx 0$ when the channel is conducting. Inserting Eq.(3) and Eq.(5) into above equation, we can estimate the degradation of I_D due to NBTI as follows:

$$\frac{\Delta I_D}{I_{D0}} = \frac{q \Delta N}{C_{ox}(V_{GS} - Vth)} + \alpha \Delta N, \tag{8}$$

which suggests that the fraction of I_D degradation is proportional to the severity of NBTI wearout.

Similarly, the HCI-induced degradation is also a combined effect of threshold voltage shift and channel mobility degradation, which implies that basically Equation (6) also holds true for HCI degradation. Hence, the amalgamated aging effects of NBTI and HCI can be written as:

$$\frac{\Delta I_D}{I_{D0}} = \left[\frac{q}{C_{ox}(V_{GS} - Vth)} + \alpha \right] \cdot \Delta N_{nbti+hci}, \tag{9}$$

where $N_{nbti+hci}$ is the total trap density generated by NBTI and HCI.

III. Direct Aging Measurement With A Novel Sensor

In this section, we describe the circuit architecture of the sensor that enables the proposed direct measurement of the NBTI and HCI induced aging effects. The block diagram of V_{th}-based and proposed I_{pp}-based aging measurement schemes are depicted in Figure 3. Different from existing V_{th}-based measuring scheme, our scheme measures the power supply current I_p directly from the CUO. The sensor consists of a Built-In Current Sensor (BICS), which mirrors the transient I_p current of the CUO, and sends it to a Current-mode Peak Detector (CPD). The CPD detects the peak value of the input current by using a current comparator, and holds the peak current for an adjustable time within a current memory, which allows the current-to-time converter (C2T) to translate the current value into a Pulse-Width Modulated (PWM) signal. With the PWM signal, the aging status of the CUO can be extracted by further processing with the model discussed in Section II. This aging information can be further utilized to implement a DRM system, which can provide the best system performance for certain given application and reliability requirements.

The key component of the proposed sensor is the CPD, which is described in detail in the following sub-section. In order to achieve a good accuracy, the C2T is carefully designed as well, and details are presented in Section III-B. For the current sensing we make use of the BICS approach proposed in [10].

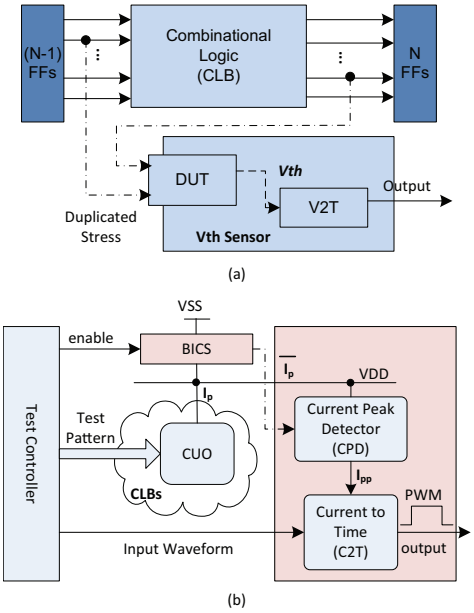

Fig. 3. Illustration of the two different measurement scheme for degradation detection: (a) V_{th} sensor scheme; (b) a direct measurement scheme with the proposed I_{pp} sensor (in the shadow box). The aging indicator I_{pp} of the proposed sensor is taken from the CUO directly. V_{th} sensor takes the aging indicator V_{th} from the DUT of the sensor.

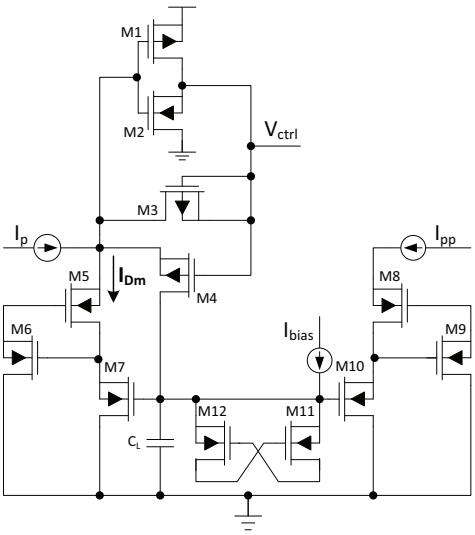

Fig. 4. Circuit schematic of the current-mode peak detector.

A. The Current Peak Detector (CPD)

Figure 4 depicts the proposed current peak detector, that is composed of: (i) a current memory cell with an adjustable memory holding time constant, to retain the peak current value, and (ii) a current comparator to determine if the present supply current value is bigger than the stored peak value, in which case the peak current value in the memory cell is updated. We denote by I_p, the input current of the CPD, by I_{pm} and I_{pp}, the input and output current of the current memory cell, and by V_{ctrl}, the output voltage of the current comparator. The current comparator [5], compares the values

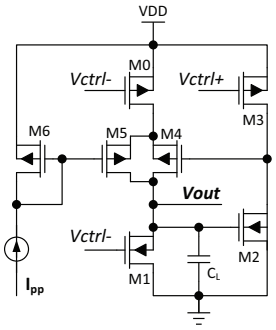

Fig. 5. Circuit schematic of the current-to-time converter.

of I_p and I_{pm} currents. When the comparator input current is positive, i.e., $I_p > I_{pm}$, the comparator input voltage increases to the upper rail voltage V_{DD}, forcing the output voltage V_{ctrl} to be low. The current memory cell consists of two regulated cascode stages [7], which enables a better output swing and an increased output impedance. To describe the CPD operation, we distinguish between two functional stages: (i) the mirroring stage, characterized by $I_p > I_{pm}$ (i.e., the CPD input current is bigger than the stored peak value), and (ii) the peak holding stage, characterized by $I_p < I_{pm}$ (i.e., the CPD input current is smaller than the stored peak value, hence the peak value remains unchanged). During the mirroring stage, the comparator output voltage V_{ctrl} is low, enabling the current memory cell via transistor M_4, to mirror I_p (i.e., $I_{pp} = I_{pm} = I_p$). During the peak holding stage, V_{ctrl} is high, transistor M_4 is off, and the current memory cell holds the peak value of the I_p current (i.e., $I_{pp} = I_{pm}$). The storing capability is achieved using the gate-to-source capacitances of M_7 and M_{10}, in parallel with the discharge path consisting of cross coupled transistors M_{11} and M_{12} and current source I_{bias}. In this way, the discharging time constant can be controlled by the current I_{bias}. The maximum peak current is limited by the sourcing ability of the comparator with feedback diode, while the minimum detected peak current is constrained by the comparator gain and the output impedance of the circuit under aging assessment.

B. The Current-to-Time Converter (C2T)

The C2T converter, based on a thyristor delay element [8], is depicted in Figure 5. It receives as triggering input the comparator output voltage V_{ctrl} and generates a time interval proportional to the value of the control current I_{pp}. Its operation can be described as follows: When a rising edge of V_{ctrl} is detected, the load capacitance charges from 0 to V_{DD}, slower until the voltage V_{out} reaches the threshold voltage of transistor M_2, and faster for the remaining time to V_{DD}, due to the feedback connection. The falling edge of V_{ctrl} triggers the discharging of the voltage across capacitor C_L through the drain-source capacitance of M_1 and the gate-source capacitance of M_2. The transient waveform of the voltage across the load capacitance C_L is presented in Figure 6. The C2T time delay is defined as the rising time of

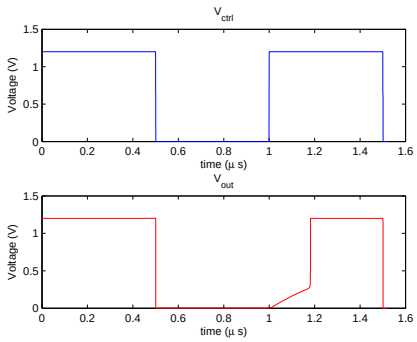

Fig. 6. The transient waveform of the voltage across capacitor C_L.

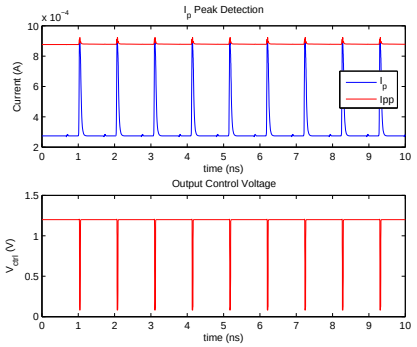

Fig. 7. Peak current detection at 1GHZ.

the converter voltage output and is given by the the relation:

$$T = C_L \cdot V_{th_{M2}}/I_{pp},$$

where $V_{th_{M2}}$ denotes the threshold voltage of transistor M_2.

C. Circuit Performance

The proposed aging sensor was implemented by using TSMC 65nm technology to analyze its performance. Figure 7 depicts the transient waveform of the I_p current and its afferent peaks, at a frequency of $1GHz$.

In order to assess the accuracy of the peak detector and current-to-time converter circuits, we use a two stage operational amplifier as test vehicle. The reliability analysis of NBTI and HCI aging is carried out using Cadence RelXpert and Virtuoso Spectre simulators [1]. Figure 8 presents current-to-time converting results and the error evaluation of the peak detector circuit. The left axis represents the variation of the time delay T as a function of the control current I_{peak} for a load capacitance $C_1 = 1pF$. The right axis represents the measured peak value of I_p compared with the ideal peak value. For the purpose of illustration, we use a control current in the range $100uA \sim 1mA$, which results in a delay range of $120ns \sim 40ns$. Simulation results reveal that a fairly good linearity and accuracy are achieved.

IV. Simulation and Results

In order to validate and evaluate the feasibility of our proposal, i.e., using the peak value of the I_p current as circuit

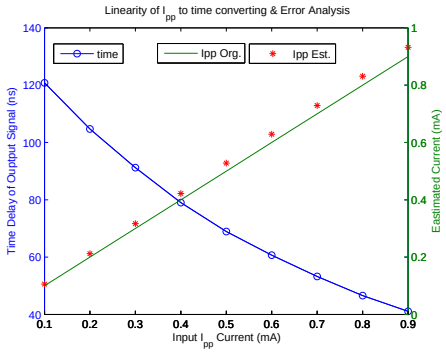

Fig. 8. Linearity of peak I_p to time converting (left axis) and error analysis of peak detection (right axis).

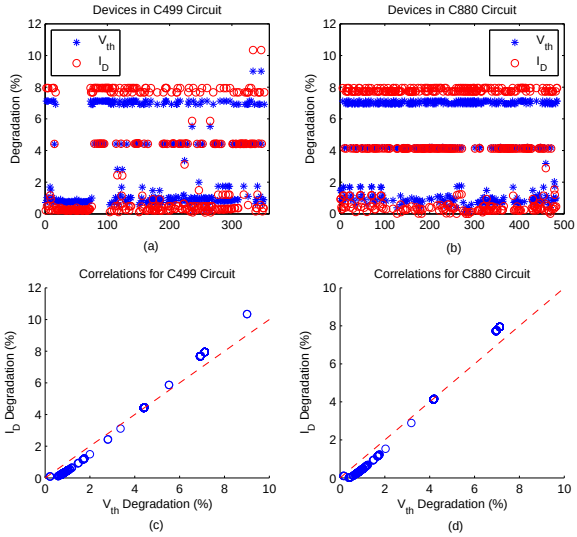

Fig. 9. The percentage degradations of V_{th} and I_D for all devices in the c499 and c880 circuits - (a) and (b); and the correlations between the percentage degradations of V_{th} and I_D - (c) and (d).

aging monitor, we conducted accelerated testing simulation on the following ISCAS85 benchmark circuits: c499, which is a 32-bit single error correcting circuit comprising 202 gates and c880, which is an 8-bit ALU, comprising 383 gates. The benchmark circuits are synthesized using the standard cells from the $45nm$ NangateOpenCellLibrary [2] technology library. The reliability analysis is carried by using Cadence RelXpert and Virtuoso Spectre simulators [1]. As concerns the simulation environment, we employed several input aggression profiles consisting of different input patterns for each benchmark circuit. As environment parameters, we used a temperature of $27°C$, and a power supply $V_{DD} = 1.0V$. We exposed the benchmark circuits to NBTI/PBTI and HCI wearout stress and adopted an EOL target of 10 years. For each benchmark circuit, we determined its critical path. Then we measured the percentage degradation of the V_{th} and the drain current I_D for every transistor on the critical path.

The percentage degradation of V_{th} and I_D for all devices in the c499 and c880 circuits are graphically illustrated in

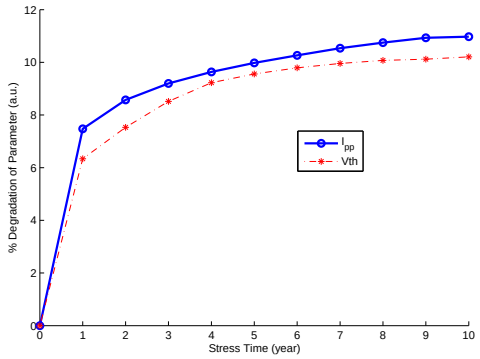

Fig. 10. The time evolution of the V_{th} and I_D degradation for 10-year simulation.

Figure 9 (a) and (b). In can be observed that for both considered circuits, for those devices which are less degraded (i.e., the percentage of degradation is small), the I_D degradation is smaller than the V_{th} degradation. As the degradation percentage becomes larger, the I_D degradation value increases faster than the V_{th} value and eventually, towards the conventional EOL (i.e., 10% degradation of circuit critical parameters), it becomes larger than the V_{th} value. The improved sensitivity can be attributed to the dependence of I_D on multiple aging critical parameters, such as the threshold voltage V_{th} and the mobility μ. This means that the I_D degradation could be a better indicator than the V_{th} degradation is, if we are concerned with the reliability status of the IC more near its final operating stage. Figure 9 (c) and (d) depict the correlations between the percentage degradations of V_{th} and I_D. As it can be seen from the figures, the percentage degradation of I_D and V_{th} are strongly correlated, which means that both of them indicate the same aging trend for all the devices.

V. Conclusions

In this paper, we proposed a direct aging measurement scheme with a novel aging sensor able to detect the amalgamated effects of NBTI and HCI. The sensor monitors the degradation of the peak power supply current in the Circuit Under Observation (CUO), enabling the measurement of the real aging status inside a circuit. The I_{pp}-based aging sensor, implemented in a commercial 65nm technology can operate at 1 GHz. The validity of using the I_D value to monitor the circuit aging, is analyzed and experimentally verified by means of simulation for a set of ISCAS85 benchmark circuits. Compared to conventional V_{th} aging monitor, I_D exhibits a better sensitivity as the circuit under aging assessment approaches its EOL, confirming the validity and practical relevance of the proposed aging monitoring framework. Figure 10 shows the evolution curve for the V_{th} and I_D degradation for 10-year simulation. The I_D curve has the same aging rate as the V_{th}, which confirms the validity of using I_D as aging quantifier during the entire circuit lifetime.

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