

# Controlled Degradation Stochastic Resonance in Adaptive Averaging Cell-Based Architectures

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**Abstract**—In this paper, we first analyze the degradation stochastic resonance (DSR) effect in the context of adaptive averaging (AD-AVG) architectures. The AD-AVG is the adaptive version of the well-known AVG architecture. It is an optimized fault-tolerant design for future technologies with very high rates of failures and defects. With system degradation the AD-AVG reliability is diminishing, as expected, but at a certain moment in time it increases due to the DSR occurrence, which is counterintuitive. We study this phenomenon under various redundancy levels and noise condition. If we take for example a 20-input AD-AVG with particular noise conditions, our simulations indicate an initial yield decrease from 1 to 0.89 with the system degradation, then a grow up to 0.94 at the DSR peak, and finally a decrease to zero when the system is reaching its end of life. Subsequently, we introduce a method to induce DSR in an AD-AVG structure, regardless of the degradation level, when this results in reliability improvement. To achieve this, we augment the AD-AVG with per input controllable noise injectors that can be utilized to induce virtual circuit degradation and create the required conditions for the DSR peak appearance. With this scheme the beneficial DSR effect is created even though the actual DSR system degradation (aging conditions) is not reached. This allows us to provide an optimum and nearly flat reliability level at any time before the DSR peak degradation level. Our experiments suggest that when we apply this method to the same 20-input AD-AVG, we obtain a guaranteed yield level of 0.94 from fresh devices to the DSR peak degradation level with a maximum yield of 0.97. In this way, a minimum yield level can be guaranteed, by determining at design time the required AD-AVG redundancy that provides it, for the entire life of the system.

**Index Terms**—Aging, averaging cell, fault-tolerance, hardware redundancy, nanoscale technology, reliability.

## I. INTRODUCTION

**N**OWADAYS, most of the new emerging device technologies are suffering from a reduced device quality. Thus, along with the benefits of smaller size, low-power

consumption, and high performance, future technologies are expected to have associated higher levels of process and environmental variations, low reliability as well as performance degradation due to the high stress of materials [1]–[4]. In view of the previous remarks, the development of more powerful fault-tolerant architectures emerges as a key research topic at the present. We note that while thus far fault-tolerant techniques with low levels of redundancy have been sufficient, this cannot hold true for new technology generations which are expected to exhibit much higher rates of failures and defects.

Currently, most of the fault-tolerant techniques rely on the use of majority gates [5], [6]. A potential alternative to majority gates is the averaging (AVG) cell [7]–[9], which exhibits higher reliability at lower cost by computing the average of the input replicas instead of relying on majority voting. Moreover, as suggested in previous paper [10], for high fault rates AVG requires a reasonable redundancy level, thus area overhead, when compared with modular redundancy (MR) or NAND multiplexing. Working with the averaging technique variations in opposite directions can be compensated and thus reduce the output probability of error. It has been demonstrated that this approach is maximally effective when the inputs are subject to independent variations with similar magnitude [9]. However, this condition is no longer valid for the current technologies as heterogeneity starts playing a relevant role. To optimize the AVG architecture in nonhomogeneous variation environments, we proposed the adaptive averaging (AD-AVG) architecture [11]. This enhanced AVG technique is capable of tolerating nonhomogeneous input variations and the effects of degradation by cleverly adapting the input weight values. The basic AD-AVG principle is to assign larger weights to the most reliable inputs, based on the measure of the associated variability, and smaller weights to the ones more prone to be unreliable. We have analyzed in detail the AD-AVG capabilities in [11], and we have recently discovered an interesting but counter-intuitive phenomenon occurring in AD-AVG structures, the so-called degradation stochastic resonance (DSR) [12], that deserves further study.

In this paper, we analyze in detail the DSR phenomenon and its consequences on the AD-AVG reliability enhancement capabilities. This counterintuitive effect takes places in the AD-AVG structure as a result of the combined effect of hardware degradation and the noise present in the Variability Monitor, i.e., the AD-AVG part in charge with the averaging weight calculation and reconfiguration. The DSR effect is related to the well-known suprathreshold stochastic resonance (SSR), which was first analyzed by Stocks in [13]. Some interesting applications of SSR phenomenon are sigma-delta modulators [14] and analog-to-digital converters [15]. In the case of AD-AVG, DSR

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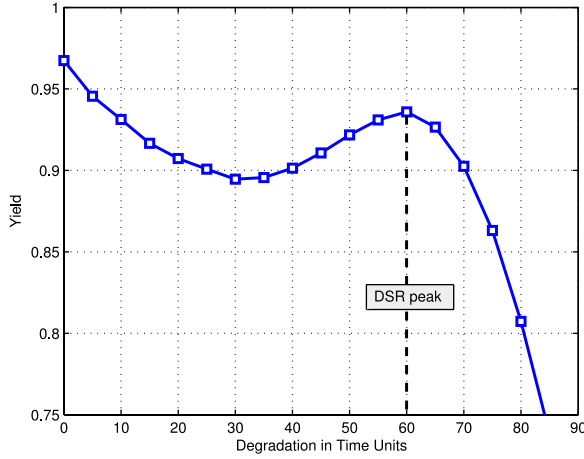


Fig. 1. Yield of 20-input AD-AVGs against degradation with noise in the Variability Monitor of magnitude  $\sigma_s = 0.06$  V.

occurrence provides an unexpected reliability enhancement after a certain degradation level is reached and under specific noise conditions. Our simulations indicate that a DSR-induced reliability peak is reached at a particular amount of degradation in time, which depends on the AD-AVG reliability level and input variability level. Thus, the DSR phenomenon implies that while the system degradation increases the AD-AVG reliability evolves as follows: after an initial decrease, it improves until a maximum value is reached at the DSR peak, after which it finally steadily decreases to zero.

For example, if we take a 20-input AD-AVG with a noise level in the Variability Monitor of 0.06 V, then the reliability evolves as follows (see Fig. 1): 1) The yield starts from a high value of 0.97 in fresh devices and gradually decreases to 0.89 when the degradation level is reaching 35 units. 2) As the degradation is increasing, due to the DSR effect, the yield starts increasing up to 0.94, at the DSR peak which corresponds to an accumulated degradation in time of 60 units. 3) After the DSR peak the circuit's accumulated degradation causes a drop in the yield characteristic. This particular AD-AVG example was chosen to clearly show the DSR effect. In general, DSR causes different yield evolutions depending on the circumstances of redundancy, noise, and degradation level. We also want to point out that even in current technology a 20x replication appears to be unacceptable, due to device scaling, which results among other positive aspects in a low reliability, such a solution might be unavoidable. Moreover, if we consider some emerging technologies such as solid-state nanopores high replications levels of up to 20 are not prohibitive any longer [16], [17].

As DSR results in yield improvement under certain aging conditions a legitimate question to ask is: *Can one take an advantage of DSR over the entire lifetime of the system?* In the second part of the paper, we address this question and propose a method to artificially create the conditions such that DSR induced yield peaks are obtained for a large part of the system life time, i.e., from fresh devices (in particular, from the moment when the yield falls under a minimum acceptable value) up

to the end of life (the degradation is that high that no yield improvement is possible any longer).

To this end, we first demonstrate that by artificially changing the variability level of the AD-AVG inputs we can control the DSR peak occurrence and position, thus for any degradation level we can find an input variability level that induces a DSR yield peak. Subsequently, we propose to augment the AD-AVG structure with per input controllable noise injectors and to extend the Variability Monitor such that it can compute, apart from the required input weight values, also the noise level that virtually increases the circuit amount of degradation. In this way, the AD-AVG is capable of creating the required conditions for the DSR peak occurrence, regardless of the actual system degradation level.

Our simulations indicate that the augmented AD-AVG scheme is capable, besides of eliminating the yield decrease range that normal AD-AVGs exhibit prior to the DSR peak, of providing higher yield levels. This extra benefit can be explained by the fact that even though we are placing our structure under the DSR peak conditions, the system presents a lower level of accumulated degradation than the one associated to the DSR peak, which results in an yield improvement.

If we apply the proposed DSR control by noise injection to the same example as before, i.e., a 20-input AD-AVG with a noise level in the Variability Monitor of 0.06 V, the reliability evolves as follows (see Fig. 8): 1) the yield starts from a high value of 0.97 in fresh devices and gradually decreases to 0.94 during the first 6 units of degradation in time. In this lifetime part no noise injection is needed; 2) from 6 degradation units further noise injection is applied and a nearly flat yield curve is obtained until the DSR peak degradation level (60 units) is reached. In this part of the yield characteristic, we get a minimum guaranteed yield level of 0.94 and a maximum of 0.97; and 3) after the DSR peak the circuit's accumulated degradation causes a drop in the yield characteristic until it eventually reaches zero.

This paper is organized as follows. In Section II, we present the AD-AVG architecture and the models we use to simulate it. In Section III, we introduce the DSR effect with a particular example of a two-input AD-AVG in which we can analytically demonstrate it, then we extend the DSR intuition to general AD-AVG architectures, and provide simulations to observe it in different conditions of noise and degradation. In Section IV, we propose a method to control the DSR effect and exploit its benefits in the AD-AVG design. We explain in detail the principle of the DSR control based on the input noise injectors and then sketch a potential implementation. Section V presents our conclusions and future work directions.

## II. AD-AVG CELL

The AD-AVG architecture, a fault-tolerant structure based on hardware redundancy is graphically depicted in Fig. 2. It is an extension of the AVG cell. Both structures are designed to compute the most probable value of a binary variable from a set of  $R$  error-prone physical replicas. In the case of AVG it is assumed an homogenous aggression scenario for all the replicas and consequently AVG makes use of the same weight

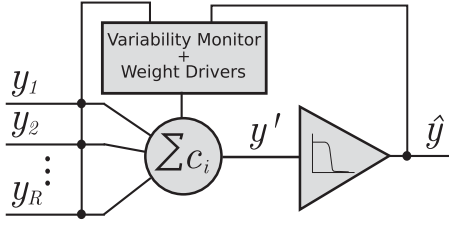


Fig. 2. AD-AVG architecture.

for all the inputs. In contrast, the AD-AVG cell architecture does not assume homogeneity and thus evaluates the variability at each input, by employing a Variability Monitor block, and calculates the set of different weights to optimize reliability. In [11], it has been demonstrated that the AD-AVG cell can efficiently tolerate high amounts of heterogeneous variability and accumulated degradation in the physical replicas.

The AD-AVG operation is based on a weighted average computation of  $R$  input replicas  $y_i$  of a binary variable  $y$ .

$$y_i = y + \eta_i \quad i = 1, \dots, R \quad (1)$$

Each replica  $y_i$  is assumed to be affected by an independent variation  $\eta_i$  that alters the ideal value  $y$ . The  $y_i$  signals are represented in the system by continuous voltage levels, where 0 and  $V_{cc}$  electrical levels stand for ideal logical values “0” and “1,” respectively. Without the loss of generality, we use  $V_{cc} = 1V$ . The  $y'$  variable is a weighed average of the replica’s inputs and consequently the AD-AVG output  $\hat{y}$  is an estimation of  $y$  according to (2).

$$y' = \sum_{i=1}^R c_i y_i \quad \hat{y} = \begin{cases} V_{cc} & \text{if } y' > V_{cc}/2 \\ 0 & \text{if } y' < V_{cc}/2. \end{cases} \quad (2)$$

We model the variation magnitudes as Gaussian random variables with null mean and different standard deviation levels  $\sigma_i$ ,  $\eta_i \sim N(0, \sigma_i)$ . The averaging weights  $c_i$  are normalized to the unity, i.e.,  $\sum_{i=1}^R c_i = 1$ , and their optimal values, as far as reliability is concerned, are

$$c_i^{\text{opt}} = \frac{\sigma_{y'}^2}{\sigma_i^2} \quad i = 1, \dots, R \quad (3)$$

where  $\sigma_{y'}^2$  corresponds to the minimum achievable weighted average variance. The analytical proof of the aforementioned equation can be found in [11]. The input variances  $\sigma_i^2$  are estimated by means of the Variability Monitor block that is subject to noise

$$\widehat{\sigma_i^2} = \sigma_i^2 + \xi_i \quad (4)$$

We model the noise level in the Variability Monitor as a Gaussian random variable with null mean and standard deviation  $\sigma_s$ ,  $\xi_i \sim N(0, \sigma_s)$ . The Variability Monitor is based on the computation of the disagreements between the AD-AVG output  $\hat{y}$  and the signal provided by each replica  $y_i$ . This mechanism was introduced by Mathur and Avizienis in [18]. The averaging weights are reconfigured by the weight drivers according to the input variance estimators and the optimal averaging weights’

formula, see (5). A detailed presentation and discussion about this calculation can also be found in [11].

$$c_i = \frac{1/\widehat{\sigma_i^2}}{\sum_{j=1}^R 1/\widehat{\sigma_j^2}}. \quad (5)$$

In this study, we assume as a matter of reference for the AD-AVG yield the percentage of circuits that satisfies the reliability requirement  $P_e < 10^{-4}$  (equivalently  $\sigma_{y'} < \sigma_{\max} = 0.1344 V$ ). As it is exposed in detail in our previous work [11], we use a degradation model to simulate the system behavior over time. In the analysis, we use a degradation normalized temporal unit called “degradation in time.” With this unit, instead of relating particular amounts of degradation to time, we make our model more general and technology independent. We basically focus our degradation metric on measurable circuit magnitudes that vary with degradation and associate degradation in time units to these increments. This technique was utilized in other studies, e.g., [19]. In these cases time is not directly related to degradation but measurable percentages of parameters shift due to degradation. Our degradation model can be stated as follows: we generate the initial values of the input replicas variance following a Gamma probability distribution function  $\sigma_i^2 \sim \Gamma(x; k, \phi)$  with scale parameter  $\phi = 2$  and mean value  $E\{\sigma_i^2\} = 0.07 V^2$  (this value reproduces technologies with poor reliability); the influence of increasing amounts of degradation is modeled by adding random Gamma-distributed increments to the initial input variances. We define the unit of degradation in time, so that it corresponds to a mean increase in the replicas’ variance  $\sigma_i^2$  of magnitude  $0.02 V^2$ . We use this normalized time-scale because we want to have a technology independent degradation model. In practice the relationship between degradation and time depends on the particular utilized technology, the stress experienced by the system, and other environmental conditions, thus our model can be translated in time if this information is available.

### III. DEGRADATION STOCHASTIC RESONANCE

In this section, we analyze the DSR effect in the AD-AVG architecture. To do so, we first focus on a particular case of DSR with a two-input AD-AVG structure ( $R=2$ ). This example will reveal us the circumstances of noise under which the DSR effect occurs. After this example we also perform a sensitivity analysis of the AD-AVG yield to the degradation of one particular input. This result will permit us to generalize the DSR effect to AD-AVG structures with an arbitrary number of inputs. Finally, we will show simulation results for the AD-AVG structure with different redundancy factors  $R$  and noise levels in the Variability Monitor ( $\sigma_s$ ) in order to conclude a clear overview of the DSR impact in AD-AVG structures.

#### A. DSR in two-Input AD-AVG

Focusing on a simple AD-AVG case with two-inputs, we are able to perform an exact analytical study of the DSR effect. We analyze the case of a two-input AD-AVG when one of the inputs has very small, even null variability level ( $\sigma_1 \approx 0 V$ ) and the

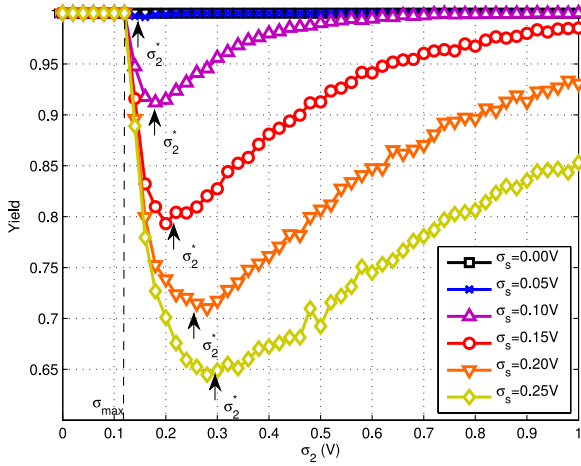


Fig. 3. Monte-Carlo simulation result of a two-input AD-AVG yield against  $\sigma_2$  with null variability in the input 1 ( $\sigma_1 = 0$  V). We consider different levels of noise in the Variability Monitor ( $\sigma_s$ ) and a maximum admissible output variability of  $\sigma_{\max} = 0.1344$  V.

variability of the other one ( $\sigma_2$ ) increases over time as a consequence of degradation. In order to perform the calculations, we model the statistics of the input variability levels with parameters  $\sigma_1$  ( $\approx 0$  V),  $\sigma_2$ , the noise in the Variability Monitor  $\sigma_s$ , and the reliability specification of maximum admissible output variability  $\sigma_{\max}$  (above this level we assume cell failure). First, we perform a Monte-Carlo simulation; Fig. 3 depicts the resulting yield against the variability in the input 2 ( $\sigma_2$ ). We observe that the yield is always 1 when  $\sigma_2 < \sigma_{\max}$ . This is because, in these conditions, any possible combination of weights gives place to an output with a variability level lower than the maximum tolerated. However, as soon as  $\sigma_2$  becomes greater than  $\sigma_{\max}$  the yield begins to decrease at different rates depending on the level of noise in the Variability Monitor. Obviously, the greater the noise the greater the yield loss. This detrimental effect of degradation, or increase in the variability, happens only during a certain range of input variability. After a critical variability level in the input 2 ( $\sigma_2^*$ ), the effect of further degradation changes and becomes beneficial; this is the starting point for the DSR effect in this particular case (see Fig. 3). We can understand this phenomenon by realizing that as the input variability  $\sigma_2$  grows the AD-AVG is capable of calculating more precisely the optimal value of the averaging weights. The ratio between the variability  $\sigma_2$  and the noise in the Variability Monitor  $\sigma_s$  increases, and therefore the measure of input variability necessary to calculate the averaging weights becomes more reliable. In fact, the AD-AVG gives more weight to the input 1, which has null variability, and the yield grows up to 1 again.

For this particular case, it is possible to prove the effect analytically. Given the conditions described for this example, we can calculate the probability density function of the averaging weights  $f_{c_1}(c_1)$ ,  $f_{c_2}(c_2)$ , and the yield of the AD-AVG structure  $Y$ . Taking the derivative of the yield with respect to the variability level  $\sigma_2$ , we obtain a closed analytic expression that reveals the impact of degradation in the reliability of the structure, as

TABLE I  
CRITICAL VARIABILITY LEVELS ( $\sigma_2^*$ ) OF DSR EFFECT IN A PARTICULAR CASE OF TWO-INPUT AD-AVG WITH NULL VARIABILITY IN THE FIRST INPUT

$\sigma_s$ (V)	$\sigma_2^*$ (V)
0.00	0.1344
0.05	0.1474
0.10	0.1777
0.15	0.2149
0.20	0.2550
0.25	0.2965

given next

$$\frac{dY}{d\sigma_2} = \frac{1}{\sqrt{2\pi}\sigma_s} \sqrt{\frac{\sigma_{\max}}{\sigma_2}} e^{-\frac{\sigma_{\max}\sigma_2}{2\sigma_s^2}} \operatorname{erf}\left(\frac{\sqrt{\sigma_2(\sigma_2 - \sigma_{\max})}}{\sqrt{2}\sigma_s}\right) - \frac{\sigma_{\max}}{\pi\sigma_2\sqrt{\sigma_2(\sigma_2 - \sigma_{\max})}} e^{-\frac{\sigma_2^2}{2\sigma_s^2}}. \quad (6)$$

Matching to zero (6), we obtain the condition in terms of accumulated degradation ( $\sigma_2$ ) that the AD-AVG system must satisfy in order to start experiencing the DSR effect, see (7). In this example, we define this characteristic point of change from detrimental to beneficial degradation as the critical variability level  $\sigma_2^*$ .

$$\frac{1}{\sqrt{\pi}a} \times e^{-a^2} = \operatorname{erf}(a) \quad (7)$$

where

$$a^2 = \frac{\sigma_2^*(\sigma_2^* - \sigma_{\max})}{2\sigma_s^2}. \quad (8)$$

Solving this equation, we get the expression of  $\sigma_2^*$ :

$$\sigma_2^* = \frac{\sigma_{\max}}{2} + \sqrt{\left(\frac{\sigma_{\max}}{2}\right)^2 + 0.769\sigma_s^2}. \quad (9)$$

Substituting this formula with the simulation parameters of Fig. 3, we can verify the analytical model, see Table I, when compared with simulation results. Using this relation, it is possible to find the critical variability level  $\sigma_2^*$  of the AD-AVG for any given noise level and reliability requirement.

### B. AD-AVG Yield Sensitivity Analysis

In order to extend the previous result to AD-AVG systems with arbitrary number of inputs, we perform a sensitivity analysis of the AD-AVG's yield to the variability level of one particular input (the  $i$ th one). With this experiment we demonstrate the occurrence of the DSR effect in a general AD-AVG case. To do this, we assume an  $R$ -input AD-AVG and analyze the sensitivity of the weighted average variance against the contribution of the  $i$ th input. We separate the general output variance expression as follows:

$$\sigma_{y'}^2 = c_i^2 \sigma_i^2 + \sum_{j=1, j \neq i}^R c_j^2 \sigma_j^2. \quad (10)$$

We generate random sets of  $R - 1$  variance values  $\sigma_j^2$ ,  $j = 1, \dots, R$ ,  $j \neq i$ , following the Gamma distribution function as in previous studies [11]. As for the  $i$ th variability ( $\sigma_i$ ), we swept



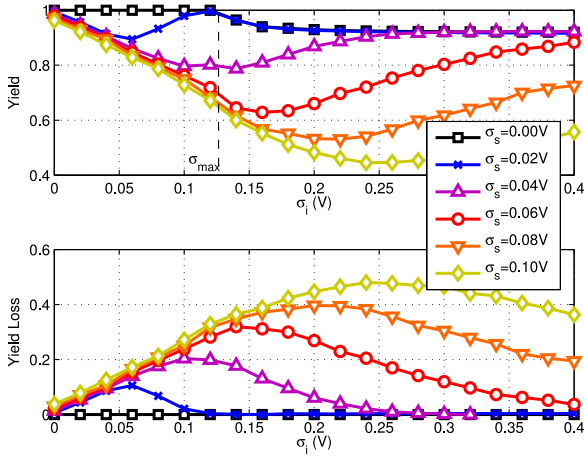


Fig. 4. Sensitivity analysis of AD-AVG's yield with multiple inputs to the variability of input  $i$ th for different levels of noise ( $\sigma_s$ ) in the Variability Monitor. The figure aforementioned shows the AD-AVG yield and the lower shows the yield loss which is defined as the yield with a null noise in the Variability Monitor ( $\sigma_s = 0$ ) less the yield.

its value from 0 to 0.4 V in the Monte-Carlo simulations. In these conditions, we estimate the AD-AVG's yield taking into account different levels of noise in the Variability Monitor ( $\sigma_s$ ). Fig. 4 depicts the simulation results against the influence of  $\sigma_i$ .

We note in this experiment that ideally (when the noise in the Variability Monitor is null) the AD-AVG yield is 1 as long as  $\sigma_i < \sigma_{\max}$ , and after this value the yield decreases gradually to 0.93. This happens because the AD-AVG structure with null noise perfectly optimizes the reliability. Therefore, while the  $i$ th variability is lower than the reliability requirement  $\sigma_{\max}$  the AD-AVG yield is 1, and after this value the yield decreases gradually to the maximum yield achievable with the remaining  $R - 1$  inputs. On the other hand, when the Variability Monitor is affected by noise, the optimal weight values are calculated imperfectly and the yield is not maximized. We observe in the figure that the impact of this imperfect weight configuration is not homogenous throughout all the values of  $i$ th input variability. The yield loss presents a resonance effect with the  $i$ th input variability for different levels of noise in the Variability Monitor ( $\sigma_s$ ). This result together with the previous example evidences the relevance of the DSR effect in the AD-AVG structure.

### C. DSR in AD-AVG

Once we have perceived the intuition of the DSR effect and demonstrated its applicability to general AD-AVG cases, we focus in this section on the analysis of typical AD-AVG. Following with the previous simulations, we analyze now AD-AVG structures against the degradation in time and observe the evolution of reliability. This time we need to use the degradation model described in Section II. We simulate different size AD-AVGs with different levels of noise in the Variability Monitor ( $\sigma_s$ ) and estimate the corresponding yield. Fig. 5 depicts the simulation results for redundancy factors  $R = 3, 10$ , and 20.

In the figure, we clearly observe how the yield characteristic of AD-AVG changes over time due to the DSR effect. We also note that the influence of this resonance phenomena is more

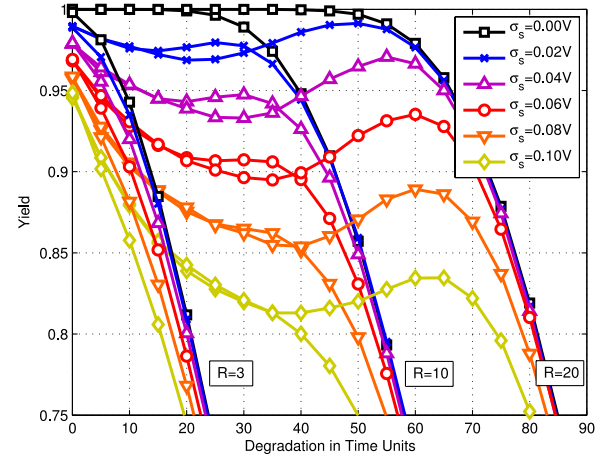


Fig. 5. Yield analysis of different size AD-AVGs against degradation for different levels of noise ( $\sigma_s$ ) in the Variability Monitor.

significant at higher levels of redundancy. In the examples of Fig. 5, the DSR effect is not perceived for the three-input AD-AVG, whereas it does for the 10 and 20 inputs AD-AVG. Another conclusion that we can extract from the figure is that DSR implies a diminution of the negative influence of noise in the Variability Monitor when the accumulated level of degradation is significantly higher than the noise level. In fact, both Figs. 4 and 5 show a negative impact of noise in the Variability Monitor that increases for low levels of degradation or input variability and then decreases after a critical amount of degradation in time. From this point, we identify the characteristic degradation in time units associated to the resonance peak as the DSR virtual age of the circuit. For example, the DSR age of 20-input AD-AVG with a noise in the Variability Monitor of  $\sigma_s = 0.06$  V is 60 units of degradation in time.

Thanks to this effect it is possible to obtain higher factors of AD-AVG yield after specific amounts of degradation. Regarding the experiment in Fig. 5 on the DSR effect, we can extract the following counterintuitive conclusions.

- 1) The DSR effect is more relevant in AD-AVGs with larger number of inputs.
- 2) Given an AD-AVG in a particular situation of degradation in time and noise level it is not necessarily the best option to use all the available replicas. There are situations in which less input replicas provide higher yield with the same degradation in time and noise in the Variability Monitor due to the DSR phenomenon.
- 3) We would increase the system yield if we could artificially increase the amount of degradation in time up to the resonance peak. This operation is feasible as long as the level of degradation in time is below the DSR peak degradation level. This will be contemplated in next section.

## IV. DSR-AWARE AD-AVG DESIGN

In the previous section, we demonstrated that after a certain degradation level the DSR phenomenon occurs, which results in a yield improvement. Based on this, we conclude that degradation can also have beneficial effects and one can embrace it

and try to take advantage of it whenever possible. However, the DSR enhancement becomes effective only after a certain system degradation is accumulated because one cannot take advantage of it in fresh devices. In order to extend the DSR benefit over the entire system lifetime, we propose in this section a DSR tailored AD-AVG structure. The main idea behind our proposal is to artificially create degradation symptoms in the AD-AVG such that it exhibits, regardless of the real degradation level, the DSR peak behavior/yield. To this end, we first analyze the relation between AD-AVG degradation, input variability, and the DSR occurrence, and demonstrate that by increasing the input variability we can induce DSR peak conditions at any degradation level. In other words by increasing the input variability a virtual degradation correspondent to the DSR peak can be induced in the AD-AVG system. Based on this, we further demonstrate that by run-time controlling the input variability we can place the system yield above the DSR peak level for a large range of degradation levels, i.e., most of the system lifetime span. Finally, we briefly discuss the practical implications of this method on the AD-AVG cell organization and sketch a potential implementation of DSR tailored AD-AVG cells.

#### A. DSR Occurrence Control

The main idea behind extending the DSR effect occurrence is to add virtual degradation to the system in order to create DSR peak degradation conditions regardless of its actual degradation level. Thus, to virtually make the system behave as it had the amount of degradation associated to the DSR peak. Degradation affects the hardware and causes a variability increase in the input signals. Therefore, one way to achieve this virtual degradation is to increase the input variability levels to make the system behave like it would have been in a higher degradation status. However, we have to take into account that only reversible approaches can avoid reducing the circuit lifespan. In fact, if we increase the circuit degradation using an irreversible procedure, we are maximizing the reliability at the present moment but we are compromising the future. As degradation always keeps increasing irreversibly the amount of virtual degradation, we need to get to the resonance peak decreases over time. In this line of reasoning, we propose the use of controllable noise injectors that can easily modify the magnitude of noise added to the inputs. A detailed explanation of the proposed controllable noise injectors is given in Section IV-B. In the augmented AD-AVG structure, the practical control of DSR effect takes place inside the Variability Monitor and Weight Drivers block, see Fig. 6. Based on the estimated input variability levels  $\hat{\sigma}_i^2$  it is possible to approximate the optimum noise level as shown next.

In order to test the efficiency of this idea, we analyze the impact of adding the Gaussian noise to the AD-AVG inputs on the overall system reliability. To perform this analysis, we take as a reference the curve in Fig. 5 corresponding to 20-input AD-AVG with a noise in the Variability Monitor of  $\sigma_s = 0.06$  V and compare it with the case when noise with different magnitudes is added to the AD-AVG inputs. We basically repeat the same Monte-Carlo simulations whose results are depicted in Fig. 5

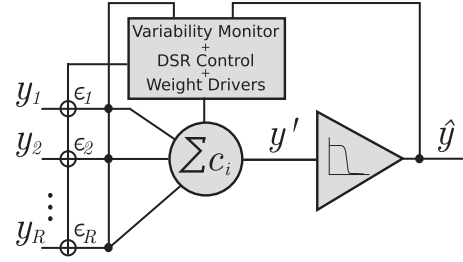


Fig. 6. Adaptive averaging cell architecture with independent noise generators added to the inputs.

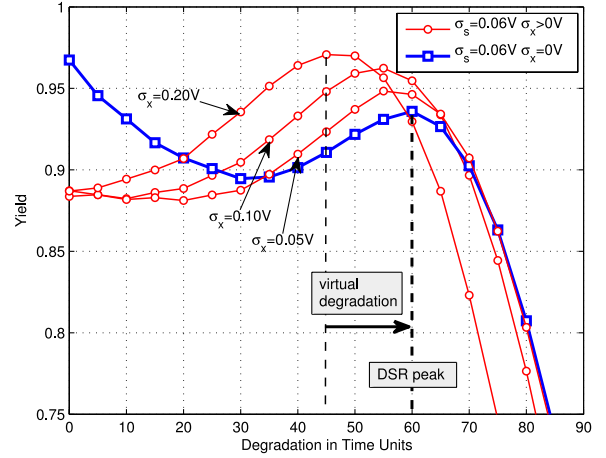


Fig. 7. Yield against degradation of 20-input AD-AVGs with different levels of noise added to the inputs. Thick blue line correspond to the AD-AVG cell yield with noise in the Variability Monitor of magnitude  $\sigma_s = 0.06$  V. Thin red lines correspond to the impact of adding noise to the inputs of this cell with different magnitudes:  $\sigma_x = 0.05, 0.10$ , and  $0.20$  V.

but now we are adding a noise signal  $\epsilon_i$  to each input  $y_i$ .

$$y_i' = y_i + \epsilon_i. \quad (11)$$

We assume that the  $\epsilon_i$  signals are independent from each other and follow a Gaussian distribution with null mean and standard deviation  $\sigma_x$  ( $\epsilon_i \sim N(0, \sigma_x)$ ). Fig. 7 depicts in thick blue line the yield of the AD-AVG cell with noise of magnitude  $\sigma_s = 0.06$  V in the Variability Monitor and in thin red lines the impact of adding noise to the inputs of magnitude  $\sigma_x = 0.05, 0.10$ , and  $0.20$  V. As one can easily observe in Fig. 7 the DSR peak is shifted toward lower levels of degradation by applying different input noise levels  $\sigma_x$ . For example, if we add an input noise of  $\sigma_x = 0.2$  V, we shift the DSR peak from 60 to 45 units of degradation in time. This result proves that we can really control the DSR phenomenon in the AD-AVG structure, and we can get the DSR peak enhancement conditions at any level of degradation below the DSR peak. Besides, one can also observe in the figure that this method is not only providing an enhanced yield earlier than the natural DSR peak but it also improves the yield significantly over the DSR peak depending on the particular amount of degradation. For example, in the previous simulation given a degradation level of 45 units, we can increase the yield from 0.91 to 0.97, which is higher than the resonance peak yield, i.e., 0.94.

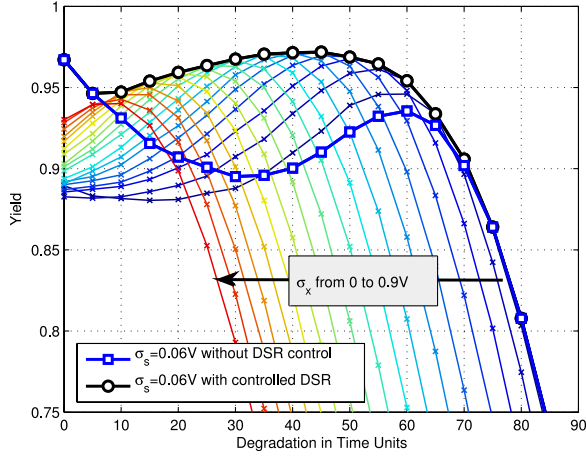


Fig. 8. Yield against degradation of 20-input AD-AVGs with different levels of noise added to the inputs. Thick blue line correspond to the AD-AVG cell yield with noise in the Variability Monitor of magnitude  $\sigma_s = 0.06$  V. Thin colored lines correspond to the impact of adding noise to the inputs of this cell with different magnitudes from  $\sigma_x = 0$  V,  $\sigma_x = 0.9$  V. The thick black line corresponds to the curve followed by the yield when the proper input noise magnitude at each degradation in time is applied in order to maximize the reliability.

Given that we demonstrated that we can control the DSR peak position by means of input variation levels, we can make a step forward and define a strategy that allows us to get the maximum yield during all the circuit lifetime, by enabling DSR peak relocation as a consequence of degradation evolution. The basic principle of the DSR control is to check at runtime the instantaneous amount of degradation in terms of the input variability estimators and update the input noise magnitude accordingly. The target is to keep the reliability characteristic at the highest value regardless of the particular degradation level. In order to observe which is the input noise magnitude that we have to inject into the circuit in order to accomplish our goal, we present in Fig. 8 simulation results for a 20-input AD-AVG with a noise in the Variability Monitor of magnitude  $\sigma_s = 0.06$  V sweeping over different input noise levels from  $\sigma_x = 0$  V to  $\sigma_x = 0.9$  V. Fig. 8 depicts in thick blue line the curve associated to the null input noise case, thin colored lines are the curves associated to the sweeping values of  $\sigma_x$  from 0 to 0.9 V. We also highlight in the figure in thick black line the curve that the yield follows when we apply the proper input noise magnitude at each degradation in time.

If we apply the proper noise magnitude, we can move along the involute of the thin colored curves obtaining a yield even higher than that provided by the resonance peak. Since finding the exact relation between optimum input noise magnitude  $\sigma_x$  and degradation level is impractical, if not impossible, we propose a numerical approach. In the same example simulated before, a 20-input AD-AVG with a noise in the Variability Monitor of magnitude  $\sigma_s = 0.06$  V, we find numerically this relationship and the result is presented in Fig. 9. The curve indicates that a nearly linear decreasing relation between both magnitudes exists. It is, therefore, possible to achieve a good approximation of the noise magnitude  $\sigma_x$  based on a numeric approach. DSR control unit only has to implement a linear decreasing function

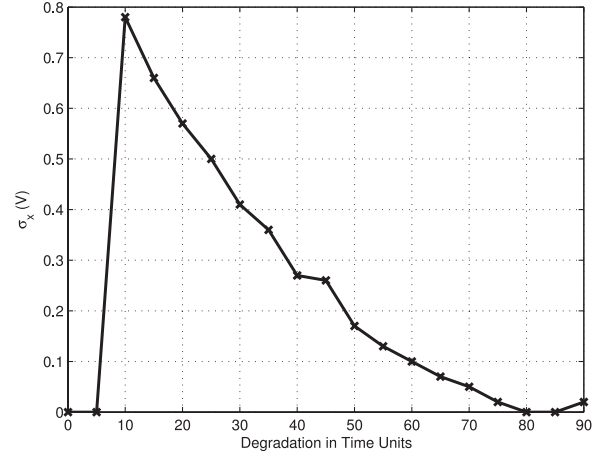


Fig. 9. Magnitude of input noise  $\sigma_x$  against degradation in time that maximizes the reliability of a 20-input AD-AVG with noise in the Variability Monitor of magnitude  $\sigma_s = 0.06$  V based on the DSR effect.

with the estimated input variability levels. We can describe the evolution of the injected noise magnitude  $\sigma_x$  for the DSR control as: 1) We start with an initial stage in which the circuit is young and healthy and no DSR yield enhancement is needed. During this period of time a null input noise magnitude is the best option  $\sigma_x = 0$  V. 2) After six units of degradation in time the DSR control becomes useful with an input noise magnitude of  $\sigma_x = 0.8$  V. From this moment and during the rest of the circuit lifetime, we have to apply an input noise magnitude that decreases approximately linearly against the degradation level. 3) Finally, when the natural DSR peak degradation level is reached, the optimum input noise magnitude arrives to zero and afterward the circuit reliability drops.

### B. Controllable Noise Injectors Implementation

In order to virtually increase the instantaneous amount of degradation, we may think of different strategies. In this study, we choose the option of adding independent noise injectors of controllable magnitude  $\epsilon_i$  to the inputs, see Fig. 6. Using this technique, we can increase the input variability levels at any time with a particular magnitude. We can also gradually reduce the magnitude of added noise to zero as the circuit continues to experience degradation.

To implement the noise injectors, we propose to make use of diodes designed to work through avalanche breakdown. We can artificially generate electrical noise for each input by controlling the avalanche breakdown phenomenon occurring in  $R$  different diodes in the AD-AVG structure, one for each input replica. This phenomenon has been widely studied [20] and it offers us an easy solution for the DSR control.

By adding a controllable noise injector to each input, we modify the input variability levels as

$$\sigma_i^2 = \sigma_i^2 + \sigma_x^2. \quad (12)$$

We assume a normal distribution for the noise added  $\epsilon_i$  to the input signals with a null mean and standard deviation  $\sigma_x$ . With



the proposed implementation the noise magnitudes generated by the injectors are independent as required.

## V. CONCLUSION

In this paper, we present the DSR effect in the context of AD-AVG architectures. This counterintuitive effect implies an enhancement in the system reliability against hardware degradation for specific noise conditions. For example, the yield of a 20-input AD-AVG, with a noise level of 0.06 V in the Variability Monitor, decreases from 1 to 0.89 as the system degradation is increasing, then it grows up to 0.94 at the DSR peak, and finally decreases to zero when the system reaches its end of life. We analytically demonstrate this behavior in the particular case of two-input AD-AVG with null variability in one of the inputs. We perform several Monte-Carlo simulations to generalize the DSR effect implications to multiple input AD-AVGs. Exploring the main features of DSR, we observe that this effect becomes more relevant in AD-AVGs with large number of inputs and that the DSR peak conditions enhance the system reliability over the one provided by equivalent higher redundancy systems, which despite of including more replicas are outside the DSR peak conditions.

Moreover, in order to take the full advantage of the DSR effect, we propose to add controllable noise injectors to the AD-AVG inputs to virtually increase the amount of hardware degradation and create the DSR conditions regardless of the degradation level. By this method, we shift the characteristic yield to the DSR peak, regardless of the degradation level, and significantly enhance the system yield. Simulation results indicate that by applying the proper noise magnitude we can provide an optimum and nearly flat reliability level at any time before the DSR peak degradation level. Returning to the earlier example of a 20-input AD-AVG with a noise level of 0.06 V in the Variability Monitor, we obtain a guaranteed yield level of 0.94 during the system lifespan with a maximum yield of 0.97. This clearly demonstrates that by controlling the DSR phenomenon, we can guarantee a minimum yield level for the entire life of the system. The particular magnitude of input noise that has to be applied in order to control the DSR effect is numerically calculated, and we find that it approximately follows a linearly decreasing relation against the degradation level. Finally, we propose a physical implementation of the controllable noise injectors based on the avalanche breakdown phenomenon occurring in diodes.

## REFERENCES

- [1] M. Mishra and S. Goldstein, "Scalable defect tolerance for molecular electronics," in *Proc. Workshop Nonsilicon Comput.*, Feb. 2002, pp. 78–85.
- [2] S. Borkar, T. Karnik, S. Narendra, J. Tschanz, A. Keshavarzi, and V. De, "Parameter variations and impact on circuits and microarchitecture," in *Proc. 40th Annu. Design Autom. Conf.*, 2003, pp. 338–342.
- [3] S. Borkar, "Electronics beyond nano-scale CMOS," in *Proc. the 43rd Annu. Design Automat. Conf.* New York, NY, USA ACM Press, 2006, pp. 807–808.
- [4] S. Borkar, "Designing reliable systems from unreliable components: The challenges of transistor variability and degradation," *IEEE Micro*, vol. 25, no. 6, pp. 10–16, Nov./Dec. 2005.
- [5] M. Stanisavljevic, A. Schmid, and Y. Leblebici, "Optimization of nanoelectronic systems' reliability under massive defect density using cascaded

- R-fold modular redundancy," *Nanotechnology*, vol. 19, no. 46, pp. 1–9, Nov. 2008.
- [6] M. Stanisavljevic, A. Schmid, and Y. Leblebici, "Optimization of nanoelectronic systems reliability under massive defect density using distributed R-fold modular redundancy," in *Proc. IEEE Int. Symp. Defect and Fault Tolerance VLSI Syst.*, 2009, pp. 340–348.
- [7] A. Schmid and Y. Leblebici, "Robust circuit and system design methodologies for nanometer-scale devices and single-electron transistors," *IEEE Trans. VLSI Syst.*, vol. 12, no. 11, pp. 1156–1166, Nov. 2004.
- [8] F. Martorell, S. Cotoana, and A. Rubio, "An analysis of internal parameter variations effects on nanoscaled gates," *IEEE Trans. Nanotechnol.*, vol. 7, no. 1, pp. 24–33, Jan. 2008.
- [9] M. Stanisavljevic, A. Schmid, and Y. Leblebici, "Optimization of the averaging reliability technique using low redundancy factors for nanoscale technologies," *IEEE Trans. Nanotechnol.*, vol. 8, no. 3, pp. 379–390, May 2009.
- [10] F. Martorell, S. D. Cotoana, and A. Rubio, "Fault tolerant structures for nanoscale gates," in *Proc. 7th IEEE Conf. Nanotechnol.*, 2007 pp. 605–610.
- [11] N. Aymerich, S. D. Cotoana, and A. Rubio, "Adaptive fault-tolerant architecture for unreliable technologies with heterogenous variability," *IEEE Trans. Nanotechnol.*, vol. 11, no. 4, pp. 818–829, Jul. 2012.
- [12] N. Aymerich, S. Cotoana, and A. Rubio, "Degradation stochastic resonance (DSR) in ad-avg architectures," in *Proc. 12th IEEE Conf. Nanotechnol.*, 2012, pp. 1–4.
- [13] N. G. Stocks, "Suprathreshold stochastic resonance in multilevel threshold systems," *Phys. Rev. Lett.*, vol. 84, pp. 2310–2313, 2000.
- [14] O. Oliaci, "Stochastic resonance in sigma-delta modulators," *Electron. Lett.*, vol. 39, no. 2, pp. 173–174, 2003.
- [15] T. Nguyen, "Robust data-optimized stochastic analog-to-digital converters," *IEEE Trans. Signal Process.*, vol. 55, no. 6, pp. 2735–2740, Jun. 2007.
- [16] F. Martorell and A. Rubio, "Defect and fault tolerant cell architecture for feasible nanoelectronic designs," in *Proc. IEEE Int. Conf. Design Test Integr. Syst. Nanoscale Technol.*, 2006, pp. 244–249.
- [17] C. Dekker, "Solid-state nanopores," *Nature Nanotechnol.*, vol. 2, no. 4, pp. 209–215, 2007.
- [18] F. Mathur and A. Avizienis, "Reliability analysis and architecture of a hybrid-redundant digital system: Generalized triple modular redundancy with self-repair," in *Proc., Spring Joint Comput. Conf.*, May 5–7, 1970, pp. 375–383.
- [19] A. R. Brown, V. Huard, and A. Asenov, "Statistical simulation of progressive nbtj degradation in a 45-nm technology pmosfet," *IEEE Trans. Electron Devices*, vol. 57, no. 9, pp. 2320–2323, Sep. 2010.
- [20] R. McIntyre, "Multiplication noise in uniform avalanche diodes," *IEEE Trans. Electron Devices*, vol. 13, no. 1, pp. 164–168, Jan. 1966.



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