# Comparison of Reaction-Diffusion and Atomistic Trap-Based BTI Models for Logic Gates

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***Abstract*—In deeply scaled CMOS technology, time-dependent degradation mechanisms (TDDMs), such as Bias Temperature Instability (BTI), have threatened the transistor performance, hence the overall circuit/system reliability. Two well-known attempts to model BTI mechanism are the reaction-diffusion (R-D) model and the Atomistic trap-based model. This paper presents a thorough comparative analysis of the two models at the gate-level in order to explore when their predictions are the same and when not. The comparison is done by evaluating degradation trends in a set of CMOS logic gates (e.g., INV, NAND, NOR, etc.) while considering seven attributes: 1) gate type, 2) gate drive strength, 3) input frequency, 4) duty factor, 5) non-periodicity, 6) instant degradation versus long-term aging, and 7) simulation CPU time and memory usage. The simulation results show that two models are in consistency in terms of the gate degradation trends w.r.t. the first four attributes (gate type, input frequency, etc.). For the rest of the attributes, the workload-dependent solution of the Atomistic trap-based model is superior from the point of non-periodicity and instant degradation, while the R-D model gets advantageous in case of long-term aging, and simulation CPU time and memory usage due to its lite AC periodic and duty factor dependent solution.**

***Index Terms*—Atomistic trap-based model, BTI, degradation, reaction-diffusion model, reliability.**

## I. Introduction

THE continuity of the CMOS technology scaling is threatened in the deep submicron era by time-zero variability and time-dependent degradation [1]. Time-zero variability in sub 45–32 nm nodes occurs due to the Line Edge/Width Roughness, Random Discrete Doping, Body Thickness Variation, optical proximity effects, etc. [2]–[4]. On the other hand, time-dependent degradation, also known as the parametric degradation, is the gradual shift of the initial time-zero variability cluster on the system's Pareto space during the system lifetime depending on the experienced stress levels [5], [6]. The uneven technology scaling has drastically increased the oxide electric field experienced by the device, resulting in the TDDM failures such as Bias Temperature Instability (BTI) [Negative BTI (NBTI) in PMOS transistors and Positive BTI (PBTI) in NMOS transistors] during their lifetime [7]. The effects of BTI on MOS transistors include: (a) threshold voltage increment in the range of 100 mV, (b) drain current reduction, and (c) delay increment ranging from 4% to 30% [8]–[16].

In recent years, there has been an increased interest in BTI modeling at the transistor level [17]–[22] and at the gate-level [23]–[25].

At the transistor level, no consensus has been achieved yet; the physical origin of BTI is still under debate. Zafar in [19] presented BTI as a statistical mechanism, where the stress and recovery phases of BTI degradation were not distinctly separated. BTI recovery is ascribed to the change in the charge state of the slow oxide traps. On the other hand, Alam [17] modeled the BTI mechanism as an electrochemical process stimulated only by the vertical electric field on the gate-dielectric, where the mechanism is taken as a classical reaction-diffusion (R-D) process, and introduced the R-D model. Furthermore, Yang *et al.* [22] augmented the impact of lateral electric field along the channel that increases NBTI at high drain bias potential. However, some experimental observations (i.e., non-Arrhenius behavior of BTI temperature dependence, $\log(t)$-like recovery phase, etc.) are not well supported by the classical R-D model. Kaczer *et al.* [26] proposed a disorder-controlled diffusion and drift mechanism based on the dispersive transport that covers the points which are not explained well by the classical R-D model. Later on, Grasser *et al.* [27] derived a generalized reaction (dispersive) diffusion formalism. However, the mentioned models still assumed the recovery phase only due to the H passivation. Dispersive transport equations are coupled to the electrochemical R-D model to correct the model's behavior, and the average behavior of the large scale devices are described. Kaczer *et al.* [28] proposed the "atomistic" version of the trap-based model which succeeded in modeling the BTI as well as the Random Telegraph Noise (RTN) behavior of deeply scaled devices (see Section II-B for further details) with the workload dependency feature. The trap-based model does not exclude the generation of interface states, it is agnostic, i.e., all traps are described in terms of voltage and temperature dependent capture and emission time constants. Reisinger *et al.* [29] focused on the statistical analysis of stochastic behavior of single defects with high precision on temperature and field

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dependence, whereas only the DC and AC stress behavior of NBTI was investigated. Finally, Grasser *et al.* [21] introduced a physics-based analytic model applying the Capture/Emission Time (CET) maps for DC, AC, and duty factor dependent stress/recovery, while taking into account the saturation of degradation to extrapolate better optimistic upper bounds on the lifetime predictions compared to the R-D model.

At the gate-level, most of the published work used either the R-D model or the Atomistic trap-based model. Both models can support different input stress types depending on the solving method: only for DC, AC stress (duty factor dependent) or any kind of input stress including the non-periodic workload. Paul *et al.* in [24] pioneered the work by performing NBTI analysis through the R-D model in case of the DC voltage stress that resulted in the pessimistic outbound of the BTI degradation. Wang *et al.* [11] and Kumar *et al.* [30] applied the signal probability and the activity factor concept to the R-D model, where a non-periodic input stream is converted to its equivalent periodic stream. However, the unique degradation history of different workloads was disregarded. Moreover, most of the previous works on the R-D model studied the BTI degradation under the low frequency AC stress in the order of 10 Hz to 10 MHz which is not compatible with today's $GHz$ systems. Kaczer *et al.* in [31] presented the atomistic approach based circuit simulations that inherits the time-dependent variability in a realistic manner. The study was demonstrated on a single PMOS of an inverter. Khan *et al.* in [15] presented BTI analysis of different gates for the dynamic inputs through the R-D model, while including the periodic waveforms only. Kukner *et al.* in [16] analyzed the impacts of BTI w.r.t. the duty factor, periodic/non-periodic stress stimuli, and the gate drive strength using the workload-dependent solution of the Atomistic trap-based model, while focusing on a single inverter. In short, literature lacks of a complete study that compares the coherencies and the distinctions between the R-D model and the *workload-dependent* Atomistic trap-based model at the gate-level with a wide spectrum of aspects, e.g., gate type, drive strength, non-periodicity, etc.

All the aforementioned work indicates that BTI phenomenon is a dynamic mechanism that evolves at different rates depending on gate under consideration (type, drive strength, etc.) and input stimuli (duty factor, stress duration, periodic/non-periodic input sequence, etc.). It is therefore crucial to analyze all these BTI dependencies while considering both well-known BTI models (i.e., R-D model and Atomistic trap-based model). A comparison of the predicted impact of the two models is important in order to explore when the models are consistent, when not and which of them provides accurate estimation and for which cases. This is crucial especially for real-time systems with priorities (e.g., healthcare, aeronautics and automotive, military, etc.), where accurate degradation modeling is extremely crucial to predict the systems' behavior in time and guarantee reliable computing with required performance (timing and power) and lifetime.

This paper targets a thorough BTI comparative analysis at the gate-level, presenting in which cases it is best to use/apply either the R-D model and/or the Atomistic trap-based model. The paper investigates the responses of the models in relation to gate related attributes (i.e., gate type and gate drive strength) as well as in relation to input stimuli (i.e., input frequency, duty factor, non-periodicity and instant degradation versus long-term aging); it also examines the complexity of both models in terms of simulation CPU time and memory usage. To the best of our knowledge, this is the *first* systematic study that performs these analyses and comprehensively compares the two models at the gate-level in order to provide more insights into the two models.

The rest of the paper is organized as follows. Section II describes the applied BTI models. Section III introduces the experimental setup. Section IV presents the simulation results. Section V analyzes and discusses the results, the BTI degradation trends, and the superiority and the bottlenecks of the models in a comparative manner. Finally, the last section concludes the paper.

## II. BTI Models

Although the exact physical mechanism of BTI is not entirely clear yet, it is almost universally attributed to the generation of the traps at the silicon-oxide interface and inside the oxide layer of the transistor. BTI consists of two distinct phases, namely the stress and recovery phases. For the stress phase, the classical R-D model argues that the channel holes tunnel through the 1–2 Å interface layer and are captured by the ≡Si-H bonds. The ≡Si-H bonds are first weakened and then are broken at a higher temperature under the influence of vertical electric field on the gate-dielectric. Furthermore, BTI also depends on the lateral electric field along the channel. Yang *et al.* [22] presented the impact of high lateral field, where the activation energy of Si-H bond dissociation is reduced. However, the primary focus of our study is fully complementary to this, namely the evaluation of BTI models with an emphasis on the workload-dependency at the gate-level w.r.t. the high and low gate bias using the two well-known models. The released H's move away from the interface and leave the charged interface states $(^{+}\mathrm{S})$ that cause the degradation. For the recovery phase, the H species move back to the Si-$SiO_2$ interface to repassivate the dangling ≡Si-H bonds. The repassivation lowers the threshold voltage increment.

Some of the well-known BTI models include the classical R-D model [17], [22], [30], [32], the dispersive R-D model [18], [26], [27], the Atomistic trap-based model [13], [28], [31], and the statistical mechanics based model [19]. Below, the classical R-D model and the Atomistic trap-based model are described due to their well and wide acceptance in academia and industry.

### A. R-D Model

Jeppson and Svensson in [32] proposed the fundamental concept of the R-D model that prompted many researchers to model NBTI. From the R-D model perspective, there are two BTI phases for a MOS transistor, i.e., stress phase and relaxation phase.

In the stress phase, the interface generation rate is initially controlled by the Si-H bond breaking rate $(k_f)$ in the "reaction limited" regime, and later by the diffusion of the hydrogen from the Si-$SiO_2$ interface in the "diffusion limited" regime. In the

*fast* reaction limited regime, the number of the interface traps has the relation of $N_{IT} \sim N_o.k_f.t$, where $N_o$ is number of Si-H bonds available at the Si-$SiO_2$ interface, and $t$ is time. However, once the hydrogen starts to move away from the interface, the generation of the interface traps slows down. Then, the number of the interface traps is determined by the diffusing species, that results in the fractional-power law dependence, i.e., $N_{IT} \sim (Dt)^n$, where $D$ is the diffusion constant. The exact value of the $n$ depends on the diffusing specie, e.g., for the atomic hydrogen $n = 1/4$ and for the molecular hydrogen $n = 1/6$.

Overall, for longer stress time, the R-D model relates $N_{IT}$ generated during the stress phase with the time $(t)$ as [17]:

$$N_{IT}(t) = \left(\frac{k_f.N_o}{k_r}\right)^{2/3}.\left(\frac{k_H}{k_{H_2}}\right)^{1/3}.(6.D_{H_2}.t)^n, \quad (1)$$

where $N_o$, $k_H$, $k_{H_2}$, and n represent the initial ≡Si-H bond density, H to $H_2$ conversion rate, and $H_2$ to H conversion rate inside $SiO_2$ layer, and time exponent, respectively. In the classical R-D model, $n = 1/6$, where only the impact of vertical electric field is represented. Augmenting the impact of lateral electric field elevates the exponent. For instance, at lateral electric field of 0.47 MV/cm, it increases up to 1/5 [22]. The higher exponent will accelerate the interface trap generation, and hence the degradation of the transistor in case of having a large lateral field, i.e., drain-source bias.

In the relaxation phase, there is no ≡Si-H breaking. However, H atoms/molecules diffuse back toward the Si-$SiO_2$ interface and anneal the ≡Si-H bonds. The number of interface traps that *does not* anneal by the approaching H atoms during the relaxation phase is given by [17]:

$$N_{IT}(t_o + t_r) = \frac{N_{IT}(t_o)}{1 + \sqrt{\frac{\xi.t_r}{t_o+t_r}}}. \quad (2)$$

where $N_{IT}(t_o)$ is the number of interface traps at the start of the relaxation phase, $\xi$ is a relaxation coefficient, $t_o$ is the input period, and $t_r$ is the relaxation duration.

### B. Atomistic Trap-Based Model

Kaczer *et al.* in [28] proposed the model that related BTI with the generation of the traps. The model is based on the capture and emission of single traps during the stress and relaxation phases of NBTI/PBTI with time constants. Each trap is represented with its corresponding $\Delta V_{th}$ and the time constants for the capture $\tau_c$ and the emission $\tau_e$ under the high and low gate bias. The probabilities of the defect occupancy in case of capture $P_C$ and emission $P_E$ are defined by

$$P_C(t_{STRESS}) = \frac{\tau_e}{\tau_c+\tau_e}\left\{1 - exp\left[-\left(\frac{1}{\tau_e}+\frac{1}{\tau_c}\right)t_{STRESS}\right]\right\}. \quad (3)$$

$$P_E(t_{RELAX}) = \frac{\tau_c}{\tau_c+\tau_e}\left\{1 - exp\left[-\left(\frac{1}{\tau_e}+\frac{1}{\tau_c}\right)t_{RELAX}\right]\right\} \quad (4)$$

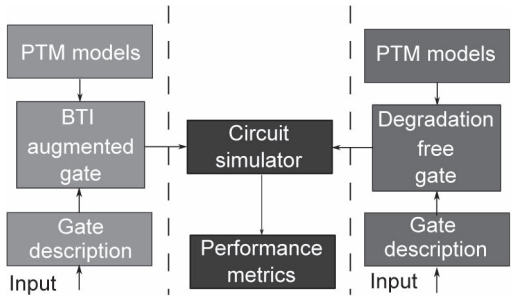


Fig. 1. Simulation framework setup.

where $\tau_e$ and $\tau_c$ are the mean capture and emission time constants, and $t_{STRESS}$ and $t_{RELAX}$ are the simulation time at stress/relaxation voltage level, respectively. Further details can be found in [13], [20], [31], and [33].

## III. Experimental Setup

This section presents first the simulation framework developed for the analysis. Thereafter, it describes the experiments performed.

### A. Simulation Framework Setup

A generic simulation framework, applying the specified BTI models to the specified gates with the specified input stress stimuli, is developed as shown in Fig. 1. The performance metrics of the specified gate, i.e., degradation-free versus BTI augmented version, are compared after SPICE simulations. The open-source Predictive Technology Model (PTM) high performance 45 nm [34] transistor models are used with a nominal supply voltage of 1 V. For the R-D model, the BTI augmented netlists are simulated in SPICE, where the model is implemented in Verilog-A. Depending on the input stimuli per transistor, the Verilog-A module generates the $\Delta V_{th}$ representing the BTI degradation. The transistor degradation are reflected in the gate delay variation. For the Atomistic trap-based model, first $\Delta V_{th}$ versus delay look-up table (LUT) is created for each gate using SPICE simulation by sweeping $V_{th}$. Then, $\Delta V_{th}$ due to the degradation is calculated in MATLAB using the Atomistic trap-based model formulation. Finally, the caused delay due to the degradation is extracted by mapping the found $\Delta V_{th}$ to the corresponding delay in the LUT.

The gate description in the framework includes the Device-under-Degradation (DuD) driving an inverter and an output load capacitance of 1 fF as shown in Fig. 2(a). *DuD* might be any type of gate with any drive strength. The inverter driven by *DuD* enables to measure realistic gate delays (i.e., fan-out of 1 delay, FO1). Stress stimulus for the BTI degradation is applied to the input of *DuD*. The rise $t_{LH}$ and the fall $t_{HL}$ times (50% to 50%) are measured between the input and output nodes of *DuD*. Delay measurements are splitted to the fall and rise times, instead of lumped delay value, to show NBTI as well as PBTI, and to do a relative comparison of them on both models. Experiments are performed with several gates and input stimuli.

For a fair comparison of the two models, the assumptions of Table I are taken into consideration during the simulations,

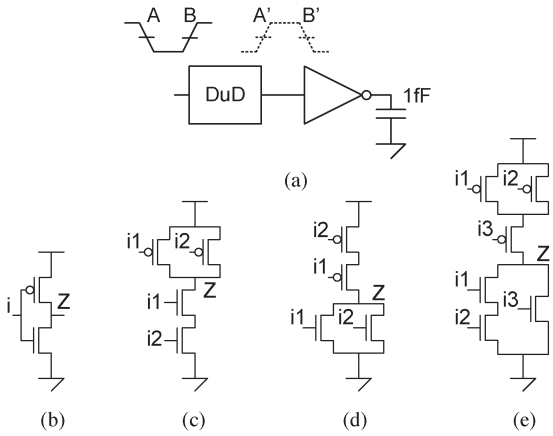


Fig. 2. (a) Circuit setup to measure Device-under-Degradation (DuD) timing, (b) *INV*, (c) *NAND2*, (d) *NOR2*, (e) *AOI21* gate topologies and input positions.

TABLE I
ASSUMPTIONS FOR EXPERIMENTAL SETUP

| | Reaction-Diffusion | Atomistic trap-based |
|---|---|---|
| Age | $10^5 s$ | $0s$ |
| Stress simulation time | $50\mu s$ | $50\mu s$ |
| What is compared? | Degradation (a.u.) (single value) | Degradation (a.u.) (distribution mean & worst-case) |

which are explained next. The R-D model has the circuits with the initial *age* of $10^5 s$, while the Atomistic trap-based model has the initially fresh (i.e., Age $= 0$) circuits. This is due to the higher visibility of the degradation trends in the R-D model in the long-term, while the Atomistic trap-based model does not require such a long period to exhibit the trends, which will be discussed in the following sections. It is valid, since this paper investigates the BTI degradation trends, and the behavior of models, not the absolute values. Secondly, both models *stress* the circuits for a *simulation time* of 50 $\mu$s; it is important to have the equal stress periods for a fair comparison. Due to the stochastic nature of the Atomistic trap-based model, the same circuit results in a different delay degradation after each simulation. 1000 Monte Carlo simulations are done (with the same seed array) each time in order to identify the mean value and the worst-case degradation. For example, Fig. 3 shows the rise $t_{LH}$ and the fall $t_{HL}$ delay distributions of 1000 performed simulations for an inverter after 50 $\mu$s long, 1 GHz periodic stress with a duty factor of 20%. The before-degradation initial timing $t_i$, the distribution mean $\mu$, standard deviation $\sigma$ and the maximum delay $max$ in the distribution are evaluated for the Atomistic trap-based model are reported. Next, the *mean* and the *worst-case* degradation (which are the degradation percentages from the $t_i$ to the after-degradation $\mu$ and $max$) are calculated. It is worth noting that the R-D model reports a single degradation value that we use for our analysis; no need for repeated simulation in this case.

When reporting the impact of BTI on each gate, the results are normalized with respect to the inverter delay without degradation (no BTI impact). For example, the bar graph of Fig. 4 shows the relative degradation (i.e., delay) of a *NAND2* gate

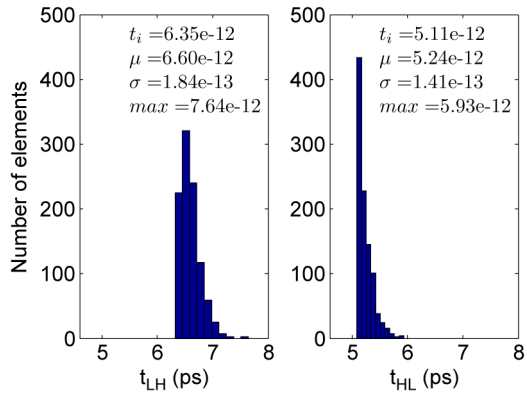


Fig. 3. The rise $t_{LH}$ and the fall $t_{HL}$ timing histograms of *INV* gate after the BTI degradation.

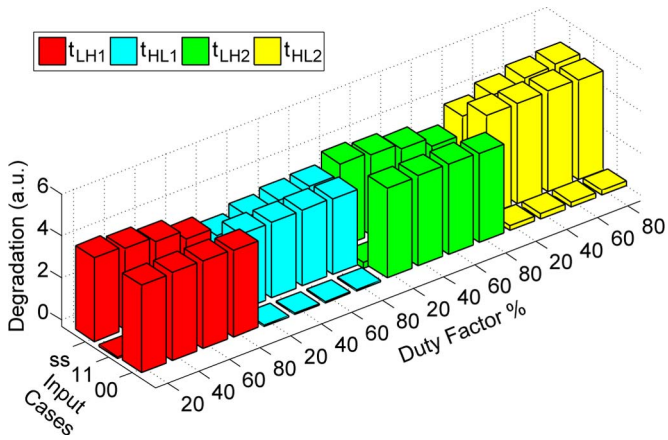


Fig. 4. Normalized mean degradations of *NAND2* gate propagation path delays w.r.t. the input vector and the duty factor.

under the same input stress conditions of the inverter above, and for different *duty factors* when using Atomistic trap-based model. There are 4 different color-grouped propagation path delays for each input combination; these are: $t_{HL1}$ (i.e., $t_{HL}$ when input $i1$ switches; see Fig. 2), $t_{LH1}$, $t_{HL2}$ and $t_{LH2}$. Note that, 1000 Monte Carlo simulations are done for each bar in the graph. The input vector of a gate might be the combinations of a constant 0, 1, or a switching sequence $s$. Due to the page limitations, here only the 00, 11, $ss$ input vector cases are presented. In case of $ss$, both rise and fall times are degraded (i.e., PMOSs and NMOSs). However, the 00 does not degrade the fall times $t_{HL1}$ and $t_{HL2}$ and the case 11 does not degrade the rise times $t_{LH1}$ and $t_{LH2}$ (no change in the inputs).

### B. Experiments Performed

As already mentioned, it is well recognized that BTI is a dynamic mechanism that evolves at different rates depending on the gate type and input stimuli. In order to investigate these dependencies, six experiments have been performed; two related to gate type and four related to input stimuli. They are explained next. It is worth noting that the complexity (simulation time and memory) of the two models under consideration is also analyzed. Remember that the measurement of the BTI impact starts after performing 50 $\mu$s of stress simulation.

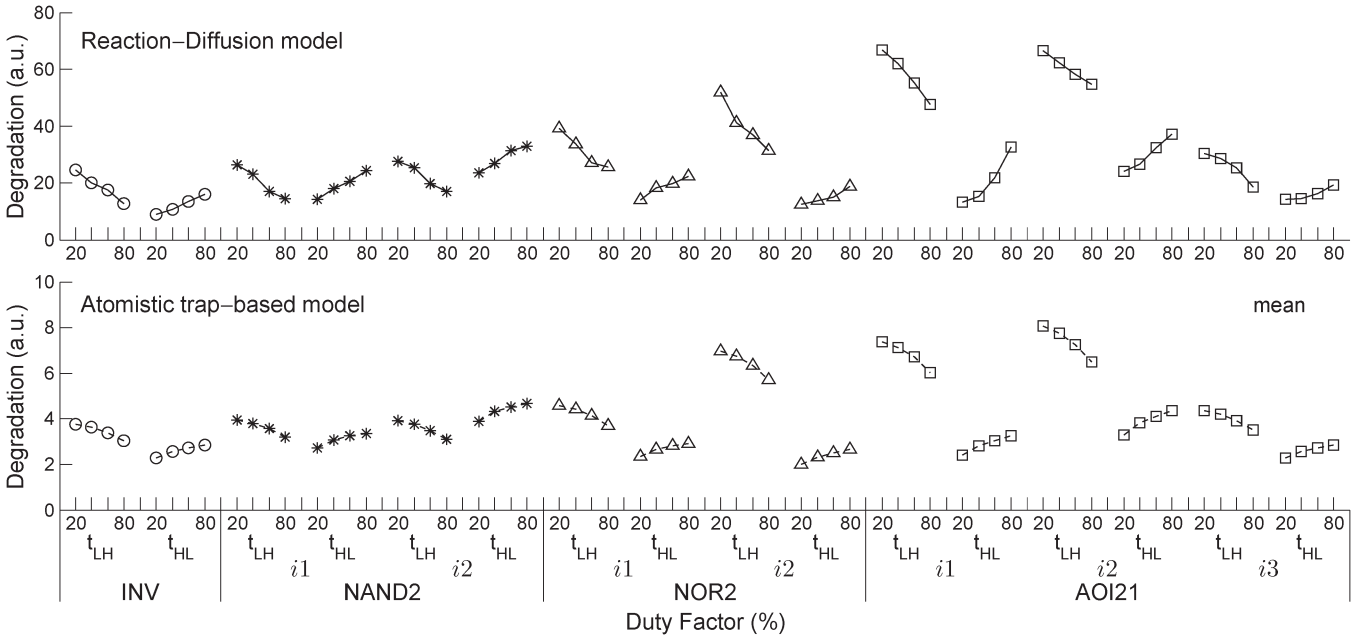


Fig. 5. Relative degradation of gates and propagation path delays.

*Gate dependency experiments:* For the *DuD*, either the gate type or the gate drive strength may differ. Periodic clock-based stress at the frequency of 1 GHz with duty factor varying from 20% to 80% is applied. Delay degradation percentage of each gate propagation path is calculated and is normalized by the *INV* $t_{HL}$ at DF of 20% without degradation. Two experiments have been performed.

- **Gate type:** This experiment presents the relative degradation of gates and propagation path delays w.r.t. the BTI model. A well-known subset of the standard cell library (i.e., INV, NAND2, NOR2, AOI21) is chosen with the same drive strength D0. Note that this subset can be used to further build more complex data path sub-blocks such as adder, shifter, shuffler, multiplexer, etc. Gate topologies and gate input positions are given in Fig. 2(b)–(e).
- **Gate drive strength:** This experiment presents the relative degradation of a gate as a function of the drive strength w.r.t. the BTI model. The width-upscaling scenario that widens the width of the transistor is studied. Inverters with gate drive strengths of D0, D1, and D2 are chosen, where the transistor widths are scaled as 1x, 2x, and 4x, respectively.

*Input stimulus dependency experiments:* For the input stimuli, the frequency, the duty factor, the non-periodicity, and the instant degradation versus long-term aging are investigated. During all experiments, the rise and the fall time of the input stress stimuli are set to 20 ps.

- **Frequency:** This experiment presents the degradation behavior as a function of the frequency w.r.t. the BTI model. Periodic input stress stimuli with the frequencies of 1 GHz, 500 MHz, 100 MHz, and 10 MHz are simulated.
- **Duty factor:** This experiment presents the degradation behavior as a function of the duty factor w.r.t. the BTI model. Input stimuli with the duty factor of 20%, 40%, 60%, 80% are generated at the frequency of 1 GHz. Clock-based periodicity remains the switching sequence same.
- **Non-periodicity:** This experiment compares the workload dependent degradation response w.r.t. the BTI model. The impact of arbitrary input sequences with a fixed duty factor of 20% on the same gate propagation path delay is examined to emphasize the dependency of the BTI degradation on the workload.
- **Instant degradation vs. long-term aging:** This experiment focuses on the instant degradation and the long-term aging trends, and the simulation capabilities w.r.t. the BTI model. Stress range is logarithmically swept from 5 ns to 50 s for the instant degradation and from 0.5 $\mu$s to $5.10^8 s$ for the long-term aging experiments.

## IV. Simulation Results

This section presents the simulation results of the experiments described in the previous section. First the simulation results for the gate dependency experiments will be presented, and thereafter for the input stimulus dependency experiments.

### A. Gate Type

Fig. 5 shows the relative degradation of the gates under consideration and their propagation path delays w.r.t. the BTI impact both using R-D model (top graph) and Atomistic trap-model (bottom graph) for different duty factors; note that the *mean* degradation values of gates are shown for the Atomistic trap-based model. It is worth noting that after the stress simulation (of 50 $\mu$s), the measurement of the impact is done for different cases depending on the number of inputs of the gate. For example, for *NAND2* the measurement is done for two cases as Fig. 5 shows: (a) keep applying the same input stream on $i1$ (as the one applied during the stress simulation) and set up input

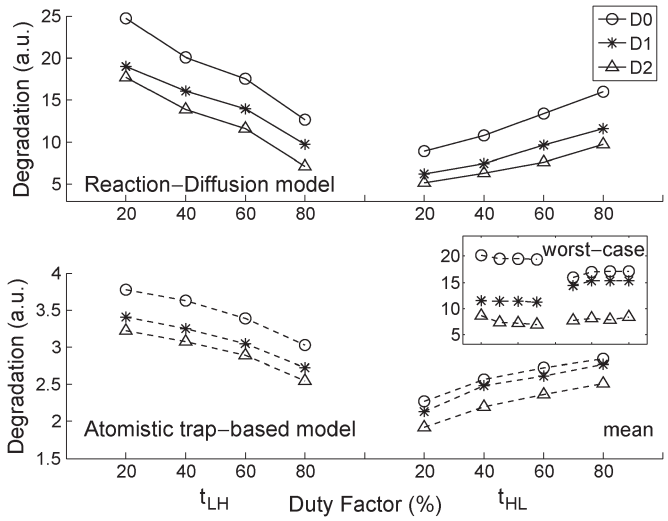


Fig. 6. Degradation of *INV* gate vs. gate drive strength.

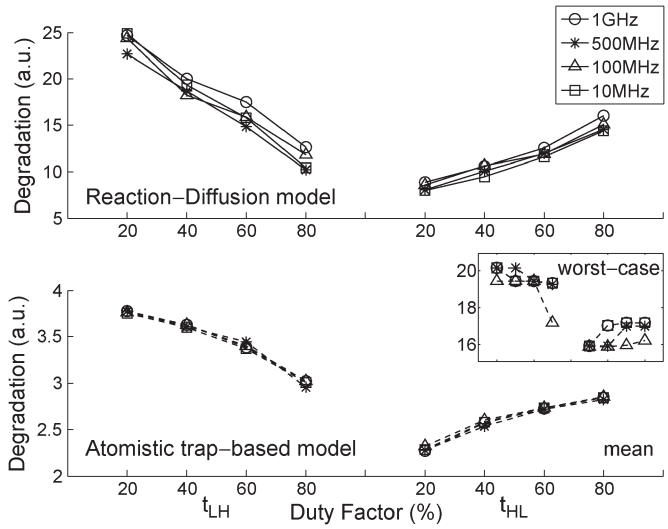


Fig. 7. Degradation of *INV* gate at various frequencies.

$i2$ to a constant value and (b) set up input $i1$ to a constant value and keep applying the same input stream on $i2$. The following conclusions can be drawn from the figure:

1) Both BTI models show the same trends for the gate degradation slopes w.r.t. the duty factor. Models are in consistency with each other.
2) The change of degradation w.r.t. the duty factor varies from 1.4× to 2.5× for the R-D model and from 1.2× to 1.4× for the mean of Atomistic trap-based model.
3) Parallel transistors degrade in the same way; e.g., *NAND2* $t_{LH1}$ and $t_{LH2}$.
4) Stacked transistors accumulate the degradation in the direction from the gate output to the rails, e.g., *NAND2* $t_{HL2}$ degrades more than $t_{HL1}$, similarly *NOR2* $t_{LH2}$ degrades more than $t_{LH1}$.
5) Transistors with a *similar location* in a gate degrade in a similar way. *Similar location* refers to be parallel or stacked, to be close to the rails or the gate output, e.g., *NOR2* $t_{LH2}$, *AOI21* $t_{LH1}$ and $t_{LH2}$, where they are the closest PMOS transistors to the rail, and also there are two stacked transistors between the supply rail and the gate output (see also Fig. 2).
6) The impact of PBTI on $t_{HL}$ propagation path can be less, equal, or higher than the impact of NBTI on $t_{LH}$ propagation path. E.g. *NAND2* $t_{HL2}$ degraded more than the $t_{LH1}$ and $t_{LH2}$ at DF 40–80%.

### B. Gate Drive Strength

Fig. 6 shows the relative degradation of *INV* $t_{LH}$ and $t_{HL}$ propagation path delays for different drive strengths (i.e., D0, D1, D2) w.r.t. the BTI model. Both the *mean* and the *worst-case* degradation values are reported for the Atomistic trap-based model. The following conclusions can be drawn:

1) Both BTI models show the same trends for the gate degradation slopes w.r.t. the gate drive strength.
2) A gate with higher drive strength is less susceptible to the BTI degradation than a gate with lower drive strength. For instance, degradation (a.u.) decreases from D0 to D2 gate for any given duty factor.
3) The change of degradation w.r.t. the gate drive strength varies from 1.4× to 1.8× for the R-D model and from 1.1× to 1.2× for the Atomistic trap-based model.
4) The change of degradation w.r.t. the gate drive strength on the worst-case values of the Atomistic trap-based model varies from 2× to 2.8×. In addition, the duty factor dependence is negligible, i.e., nearly flat lines; this is due to the definition of the *worst-case* degradation and the limitation of feasible Monte-Carlo loop in the Atomistic trap-based model.

### C. Frequency Independence

Fig. 7 shows the relative degradation of *INV* $t_{LH}$ and $t_{HL}$ propagation path delays at several frequencies. Both BTI models show the same trends w.r.t. the frequency. The plotted results overlap since there is a weak frequency dependence of BTI degradation in both models.

### D. Duty Factor

Figs. 5–7 clearly show that there is a strong dependency of the BTI degradation on the duty factor. The degradation due to the NBTI decreases for the increasing duty factor and vice versa for the PBTI.

### E. Non-Periodicity

Fig. 8 shows the gradual $V_{th}$ and delay degradation of a *NAND2* gate during $15s$ stress simulation under two arbitrary input sequences (i.e., *seq.* $a$ and $b$) with the same duty factor of 20%. The continuous and the dotted lines represent the *seq.* $a$ and $b$, respectively. The subfigures at the left column show the gradual $\Delta V_{th}$ on the PMOS device connected to the $i1$ of *NAND2*, while the subfigures at the right column show the gradual delay degradation on $t_{LH1}$ propagation path of *NAND2*. The figure emphasizes the strong correlation between

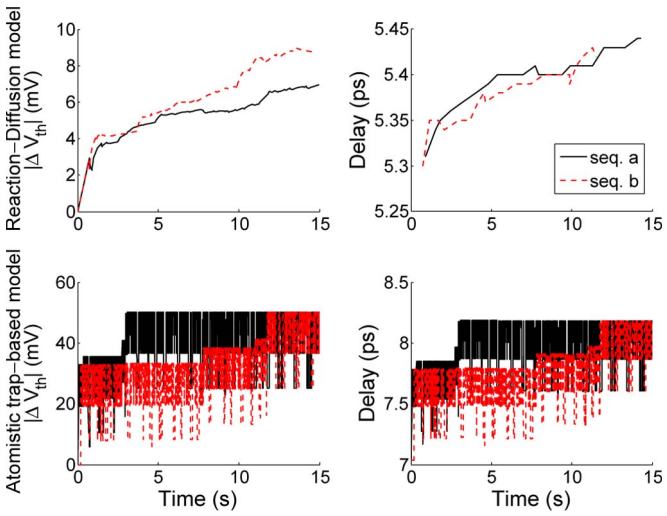


Fig. 8. Instant degradation of *NAND2* gate $t_{LH1}$ propagation path delay under two different arbitrary sequences at the same duty factor.

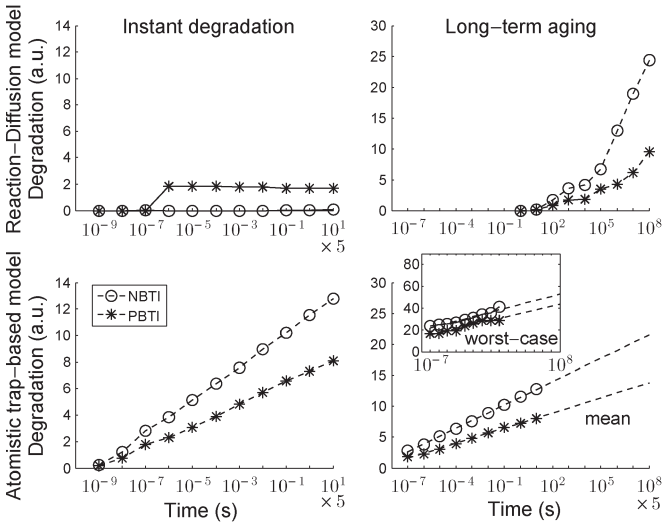


Fig. 9. Instant degradation and long-term aging trends of BTI models on *INV* gate.

the input sequence and the BTI degradation, where the different switching sequences even with the same duty factor result in different delay degradation. Secondly, the Atomistic trap-based model well traces the fast/slow $V_{th}$ changes, whereas the R-D model does not provide a detailed trace for the fast $V_{th}$ changes.

### F. Instant Degradation vs. Long-Term Aging

Fig. 9 shows the instant and the long-term response of the BTI models. The instant degradation window covers the stress simulations from $10^{-9}s$ to $10s$ time scale, while the long-term aging window covers from $10s$ up to $10^{8}s$ time scale.

As shown in the Fig. 9, a *linear* degradation trend fits well for the Atomistic trap-based model on the instant degradation and the long-term aging, whereas an *exponential* trend fits for the R-D model on the long-term aging. Trends of the R-D model become more visible on the long-term periods. It does not present a strong trend for the instant degradation, due to the lack of modeling the fast part of the BTI mechanism.

Both the *mean* and *worst-case* degradation of the Atomistic trap-based model satisfy the linear trend. Note that, the long-term aging tends to close the initial gap between the *mean* and the *worst* degradation. E.g. at 0.5 $\mu$s, the *worst-case* is $8.3-9.8\times$ higher than the *mean*; at $50s$, drops to $3-3.8\times$; finally at $10^{8}s$, drops to $2.5-3.2\times$. The reason is that once the stress simulation time is long enough, the possibility of capturing the rare traps (i.e., worst trap cases) increases. Meaning that, the distance between the distribution *worst-case* tail and the *mean* is pushed closer, hence is narrowed.

## V. Analysis and Discussion

The degradation responses of the R-D and the Atomistic trap-based models in the previous section will be discussed from the point of the gate and the input stimulus dependency. *CPU time* and *memory usage* analysis of the two models is also covered.

### A. Gate Type Dependency

From the gate dependency point, the similarities and differences are as follows:

1) The BTI degradation responses w.r.t. the gate type for both models are consistent. Fig. 5 shows the relative degradation *signatures* of different gates and their propagation path delays, where the slope directions, the shape, and the relative positions of curves match well.
2) The amount of degradation (a.u.) in $y$-axis differs and is higher for the R-D model, since the BTI degradation is measured at $10^{5}s$ for the R-D model, and at 50 $\mu$s for the Atomistic trap-based model (see Table I).

Hence, both BTI models match well with each other and are suitable to obtain the BTI degradation signatures of logic gates, where the relative degradation of different gates and their propagation path delays can be comparatively observed.

### B. Gate Drive Strength Dependency

From the gate drive strength point, the similarities and differences are as follows:

1) The BTI degradation responses w.r.t. the gate drive strength for both models are consistent. Fig. 6 shows the relative degradation *signatures* of inverters with different drive strengths, where the slope directions, the shape, and the relative positions of curves match well.
2) The amount of degradation (a.u.) in $y$-axis differs and is higher for the R-D model as in case of the gate type dependency. Hence, the same reasoning applies here, i.e., $10^{5}s$ vs. 50 $\mu$s (see Table I).
3) The change of degradation w.r.t. the gate drive strength is higher for the R-D model (i.e., $1.4-1.8\times$) than the Atomistic trap-based model mean values (i.e., $1.1-1.2\times$). Implying that, the former model has more sensitivity to the gate drive strength than the latter one.
4) On the other hand, the change of worst-case degradation for the Atomistic trap-based model (i.e., $2-2.8\times$) is higher than the R-D model. Implying that, the former

model has more sensitivity to the gate drive strength than the latter model in terms of the worst-case degradation.

5) The worst-case degradation in the Atomistic trap-based model is in the same order of the averaged out degradation in the R-D model. Meaning that, the Atomistic trap-based model strongly emphasizes and is capable of showing the discrete impact of individual worst-case traps. Hence, it might be a better choice to further investigate the BTI phenomenon in the deeply scaled device dimensions. Given that the number of atoms gets quite low, every small trap matters, thus the discrete model impact is more correct than the contiguous slow mechanism based R-D model.

Hence, both BTI models match well with each other to obtain the BTI degradation signatures of logic gates, where the relative degradation w.r.t. the gate drive strength can be comparatively observed.

### C. Input Frequency Dependency

From the input frequency point, Fig. 7 shows that both models are in coherence that the BTI degradation is independent than the input stress frequency. The frequency parameter is excluded in the BTI degradation models.

### D. Duty Factor Dependency

From the duty factor point, both models confirm that NBTI and PBTI are oppositely impacted w.r.t. the duty factor, which is shown in Figs. 5–7, independent than the gate type or drive strength, or the input frequency. For instance, NBTI in PMOS decreases for increasing duty factor, since PMOS transistor is less stressed by the shorter, low voltage stress duration, and vice versa for the PBTI in NMOS.

Finally, the slope of the degradation curves w.r.t. the duty factor is more steeper for the R-D model (i.e., $1.4-2.5\times$) than the Atomistic trap-based model (i.e., $1.2-1.4\times$) in case of different gate types or gate drive strengths, or input frequencies. Reason behind is that, the occupancy probability $P_C$ of traps as a function of the stress time and the duty factor is not linear, whereas it increases more rapidly at longer stress time w.r.t. the duty factor [13]. Figure 10 of Toledano-Luque *et al.* in [13] pointed out this fact that the $\Delta P_C$ between the duty factor from 20% to 80% at the shorter stress time is much smaller compared to the $\Delta P_C$ at the longer stress time, and hence the change of degradation. Since the initial age of the circuits in the R-D model and the Atomistic trap-based model are different (i.e., $10^5 s$ and 50 $\mu$s, respectively, see Table I), the slope of the degradation curves w.r.t. the duty factor is more steeper for the former model than the latter one.

### E. Non-Periodicity

From the non-periodic input stress point, the behaviors of the models strongly differ from each other due to how the BTI phenomenon is physically perceived and modeled.

The response of the Atomistic trap-based model in Fig. 8 shows that even when the gate type, the propagation path, and the duty factor are the same, different input sequences are unique in terms of degradation. Hence, they distinctly impact the delay degradation. The Atomistic trap-based model handles the BTI degradation in terms of the individual traps and their corresponding discrete $\Delta V_{th}$ and $\tau_{c,e}$. By definition, the model comes with the *fast/slow* and *large/small* traps which are capable of instant discrete shifts on $V_{th}$, hence on the delay as shown in Fig. 8.

In contrast, the response of the R-D model in Fig. 8 does not show the abrupt degradation signature in case of different input sequences. The resulting $\Delta V_{th}$ and delay behaviors are more contiguous. Moreoever, $\Delta V_{th}$ exhibits logarithmic rise and recovery phases which are mainly due to the exponentially modeled diffusion constants of the cumulative trap behavior. Hence, it can be concluded that the R-D model simplifies the BTI interpretation as a slow mechanism in order to speed-up the long-term modeling, while the Atomistic trap-based model views BTI as a mechanism that covers the fast traps as well as the slower ones, which is more complete and closer to reality, and is needed to analyze the short-term degradation behavior. Therefore, the sensitivity of the Atomistic trap-based model is much higher to the input than the R-D model.

As shown in Fig. 8, BTI is a highly workload dependent degradation mechanism that requires a workload dependent modeling for fine-grained predictions on the degradation.

TABLE II
NORMALIZED CPU TIME AND MEMORY USAGE

| | PC1 | | PC2 | |
|---|---|---|---|---|
| | Time | Memory | Time | Memory |
| Reference | $1.28\ t$ | $0.58\ m$ | $t$ | $m$ |
| | Reaction-Diffusion | | Atomistic trap-based | |
| | Time | Memory | Time | Memory |
| INV | $0.95\ t$ | $9.01e$-05 $m$ | $17.27\ t$ | $0.22\ m$ |
| NAND2 | $1.68\ t$ | $1.61e$-04 $m$ | $34.51\ t$ | $0.44\ m$ |
| NOR2 | $1.52\ t$ | $1.61e$-04 $m$ | $34.59\ t$ | $0.45\ m$ |
| AOI21 | $2.49\ t$ | $1.62e$-04 $m$ | $51.79\ t$ | $0.67\ m$ |

### F. Instant Degradation vs. Long-Term Aging

From the instant degradation vs. long-term aging point, the Atomistic trap-based model is capable of simulating the instant BTI impacts in the stress range as low as $ns$ to as high as tens of seconds. The model owes this feature to the detailed separation and the modeling of the $\tau_c$ and $\tau_e$ of the individual traps under the high/low voltage stress levels. Moreover, the model can still validly *extrapolate* the BTI degradation for the long-term simulations up to $10^8 s$ stress range, although it is limited by the simulation run-time. On the other hand, the R-D model is more suitable to *simulate* the long-term aging above tens of seconds.

### G. CPU Time and Memory Usage

Table II compares the models in terms of the CPU time and the memory usage. A set of gates (e.g., INV, NAND, etc.) is simulated with the periodic stress stimuli given at the frequency

of 1 GHz, for 50 $\mu$s duration, and the duty factor of 20%. Since the models locate at different PC platforms, a MATLAB built-in reference benchmark is run for 125 times on both platforms, i.e., PC1 and PC2. Afterwards, the simulation time and the memory usage are normalized w.r.t. the reference benchmark at PC2.

The linearity in the CPU time and the memory usage is clearly visible, which is directly related to the number of transistors in the gate-under-degradation. E.g. the CPU time and the memory usage of *AOI* and *NAND2* are 3× and 2× higher than *INV*, respectively, while *NAND2* and *NOR2* have the same CPU time and memory usage as each other.

The R-D model has 18× faster CPU time and 2600× efficient memory usage than the Atomistic trap-based model, in average. On the other hand, the Atomistic trap-based model parameters are orthogonally generated by the distributions. 1000 Monte-Carlo simulations are run per each gate to obtain the *mean* and the *worst-case* degradation. Note that, in case of a single workload simulation, the CPU time and the memory usage significantly decrease (i.e., 1/1000× in CPU time and ∼1/790× in memory usage). However, the Atomistic trap-based model is still limited for the long-term aging simulations due to its detailed modeling.

To conclude, both models are in coherency in terms of getting the relative degradation signature w.r.t. the gate type, the gate drive strength, the input frequency, and the duty factor. On the other hand, the R-D model lacks of presenting the unique degradation history, where the Atomistic trap-based model can provide very detailed instant degradation logs for any given input sequence. However, this superiority of the model in the detailed degradation modeling becomes a bottleneck in case of the long-term aging simulations. Therefore, the Atomistic trap-based model might apply *calibrated/educated extrapolations* to predict the long-term aging, which are still valid and consistent with the R-D model's long-term conclusions. Finally, the former model has higher CPU time and memory usage than the latter one.

## VI. Conclusion

This study compares the two well-known BTI models, namely the R-D and the Atomistic trap-based models, through the degradation simulations at the gate-level. The coherencies and the distinctions between the models are presented as a function of the 1) gate type, 2) gate drive strength, 3) input frequency, 4) duty factor, 5) non-periodicity, 6) instant degradation vs. long-term aging, and 7) simulation CPU time and memory usage.

To summarize, both models match well to obtain the BTI *degradation signature* as a function of the *gate type*, *drive strength*, *input frequency*, and *the duty factor*. In terms of non-*periodicity*, the Atomistic trap-based model has the ability to catch the fast trap behaviors, hence to present very detailed degradation logs of a given circuit under a given workload. Whereas, the R-D model does not strongly differentiate the degradation of the distinct input sequences. In terms of *instant degradation vs. long-term aging*, the Atomistic trap-based model can target the degradation simulations as fast as in the $ns$ stress time window up to the tens of seconds. However, the detailed nature of the model becomes its bottleneck while looking for the longer stress simulations. On the other hand, the R-D model simplifies the BTI interpretation as a slow mechanism in order to speed-up the long-term modeling. But this has a noticeable impact on the simulation behavior, because it sacrifices its sensitivity for the stress time window below tens of seconds. In terms of *CPU time* and *memory usage*, both models have a high linearity w.r.t. the number of devices in the simulation. The R-D model outperforms the Atomistic trap-based model. Due to the Monte-Carlo simulations and the detailed nature of the Atomistic trap-based model, the total simulation time and the memory usage to characterize a CMOS gate takes several hours even at a single duty factor point.

In conclusion, a hybrid model might be a preferable solution that inherits the most advantageous features of the two models as follows:

- from the Atomistic trap-based model
  1) the degradation resolution as low as in the $ns$ range,
  2) the distinct degradation of different input sequences, workloads, scenarios, etc.
  3) the degradation distributions with $\mu$, $\sigma$, and $max$ values,
  4) the curve-fitting both for the sub-second and above-second stress time windows.
- from the R-D model
  1) the light-weight nature,
  2) the low CPU time,
  3) the low memory usage profile,
- the capability for the long-term aging simulations up to $10^8 s$.

To the best of knowledge, this is the *first* systematic study that analyzes and presents a comprehensive comparison of the two models at the gate-level from the perspective of the mentioned points in the paper.

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In 1986, he was a recipient of the Young Scientist Award from the Marconi International Fellowship Council. He was an Associate Editor for the IEEE TRANSACTIONS ON VLSI SYSTEMS for the period 1995/1998 and for the IEEE TRANSACTIONS ON MULTI-MEDIA in 1999–2001. Since 2002, he has been an Associate Editor of the "ACM Transactions on Design Automation for Embedded Systems (TODAES)," and since 1996, he has been an Editor for Kluwer's "Journal of VLSI Signal Processing." In 1997, he became a member of the steering board for the VLSI Technical Committee of the IEEE Circuits and Systems Society, and since 1999, he has served on the steering board for the IEEE TRANSACTION ON VLSI SYSTEMS. He was the Program Chair of the 1997 IEEE International Symposium on System Synthesis (ISSS) and the General Chair of the 1998 ISSS. He was also the Program Chair and Main Organizer of the 2001 IEEE Signal Processing Systems (SIPS) Conference. He is a Fellow with the Interuniversity Microelectronics Center (IMEC), Leuven, Belgium.

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Dr. Groeseneken became an IMEC Fellow in 2007. He has served as a Technical Program Committee Member of several international scientific conferences, such as IEDM, ESSDERC, IRPS, SISC, and EOS/ESD Symposium. He has authored or coauthored over 500 publications in international scientific journals and in international conference proceedings, six book chapters, and ten patents in his fields of expertise.