Using 3D-COSTAR for 2.5D Test Cost Optimization

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***Abstract*—Selecting an appropriate and efficient test flow for a 2.5D/3D Stacked IC (2.5D-SIC/3D-SIC) is crucial for overall cost optimization. This paper uses 3D-COSTAR, a tool that considers costs involved in the whole 2.5D/3D-SIC chain, including design, manufacturing, test, packaging and logistics, e.g. related to shipping wafers between a foundry and a test house; and provides the estimated overall cost for 2.5D/3D-SICs and its cost breakdown for a given input parameter set, e.g., test flows, die yield and stack yield. As a case study, the tool is used to evaluate the overall 2.5D-SIC cost for three test optimization problems: (a) the impact of the fault coverage of the pre-bond silicon interposer test, (b) the impact of pre-bond testing of active dies using either dedicated probe-pads or micro-bumps, and (c) the impact of mid-bond testing and logistics on the overall cost. The results show that for the selected parameters: (a) pre-bond testing of the interposer die is important for overall 2.5D-SIC cost reduction; the higher the fault coverage, the lower the overall cost, (b) using micro-bump probing results in much lower overall cost as compared to probe-pads, and (c) mid-bond testing can be avoided for high stacking yield.**

I. Introduction

Tremendous effort has been put in place to bring *through-silicon via (TSV)* based 2.5D and 3D-SIC technology closer to market [1–3]. Realizing such ICs is attractive due to major benefits [4] such as (a) increased electrical performance, (b) reduced power consumption due to shortened interconnects, (c) heterogeneous integration, (d) reduced form factor, etc.

One of the major challenges that has to be addressed in order to make 2.5D technology commercially successful is overall cost optimization. A 2.5D-SIC consists of two or more active dies stacked on a passive silicon interposer that forms the interconnection between the active dies and to the external world. As is the case for any IC, TSV-based 2.5D-SICs must be tested in order to guarantee the outgoing product quality and reliability. Hence, test cost is indispensable. Inherent to their manufacturing process, 2.5D-SICs provide several test moments such as before stacking, during manufacturing of partial stacked IC, after the complete manufactured stack, etc. This results into a large space of test flows; each with its own cost. Determining the optimal and most efficient test flow requires the analysis of all test flows, as different design and/or manufacturing parameters may impact the cost differently. Therefore, an appropriate cost model is required. The cost model should be able to evaluate the cost of each test flow, while considering all relevant incurred costs in the production chain of the 2.5-SIC.

Several cost models have been published in this area for 2.5D/3D-SICs. In [5], the author considered a manufacturing cost model for 3D monolithic memory integrated circuits; cost improvement of 3D with respect to 2D (for different 3D stack sizes) was modeled. In [6], the authors developed a 3D-cost model to determine the optimal stack size for a given 3D-SICs circuit, where they restricted the variable parameters to only die yield and area. In [7], the authors proposed a 3D cost model for Die-to-Wafer (D2W) and Wafer-to-Wafer (W2W) stacking. In [8], a detailed cost model of IMEC is presented; the paper primarily focuses on (a) the difference between cost integration for D2W and W2W stacking, (b) the impact of the number of TSVs and (c) the effectiveness of different 3D testing strategies in the pre-bond phase for D2W stacking. In [9], a 3D cost model is presented that focuses on modeling of metal layers and die area impact on 3D-cost integration for D2W and W2W integration. In [10], a 3D cost model is primarily developed to estimate the optimal tier count that leads to a minimal TSV count and subsequently partition the netlist into these tiers. In [11], the authors presented a cost estimation method for 2.5D ICs by extending their 3D floorplanning tool and 3D cost models; their models only include area and wire length, and do not consider testing at all. In [12], the authors proposed a cost model that emphasizes on manufacturing and test cost; the authors investigated the impact of D2W and W2W stacking on overall cost and determined the lower bound of the yield of the final package level test given the number of stacked dies and the final yield.

The state-of-the art described above clearly shows that none of the published cost models incorporated the impact of partial stack tests and different test flows. In our previous work [13], a basic cost model for D2W stacking considering the impact of limited test flows on the overall 3D-SIC cost was presented. However, this model suffers from many limitations such as (a) a lack of support for variable fault coverage (FC), (b) a restriction to a small set of test flows, (c) a focus on D2W stacking only, (d) no consideration of logistics cost, (e) no distinction between die and interconnect tests.In our work [14], we reported the requirements and user cases of a cost model tool that addressed most of the shortcomings of our work in [13]. In this paper, we build on our previous work in [14] to develop 3D-COSTAR; a tool that considers all costs involved in the whole 2.5D/3D-SIC production chain, including design, manufacturing, test, packaging and logistics (e.g. related to

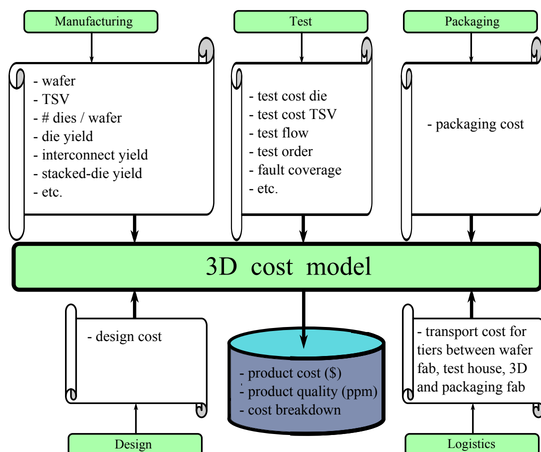

Fig. 1. 3D-COSTAR Organization.

shipping wafers between a foundry and a test house) in order to provide both the estimated overall cost for 2.5D/3D-SICs as well as its cost breakdown. More importantly, this paper analyses and reports about three case studies with respect to 2.5D-SIC test cost optimization; these are: (a) the impact of the FC of the interposer pre-bond test on the overall cost, (b) whether it is more advantageous to perform pre-bond testing for the active dies using dedicated probe pads or through micro-bumps, and (c) the impact of mid-bond testing and logistics on the overall cost.

The rest of this paper is organized as follows. Section II presents the architecture and flow of 3D-COSTAR respectively. Section III covers case studies where the test trade offs are described. Section IV presents the results of the experiments. Finally, Section V concludes the paper.

II. 3D-COSTAR

This section describes the architecture of 3D-COSTAR. First, the tool requirements are discussed followed by the use cases.

A. 3D-COSTAR Requirements and Cost Classes

In order to determine the most cost-effective test flow, the test requirements should be specified. However, taking only the test cost into consideration is not sufficient to provide a fair comparison; a test flow does not only impact test cost, but also design and manufacturing cost. For example, a pre-bond active die test with additional probe-pads increases die area and reduces the number of dies per wafer.

Figure 1 shows the general architecture of 3D-COSTAR, which can both evaluate 2.5D and 3D-SICs. The tool has five input classes which symbolize the costs involved in the whole 2.5D/3D-SIC production flow; these include design, manufacturing, test, logistics and packaging cost.

a) Design: Design for Testability (DfT) starts at the design phase to accommodate for tests at later stages (pre-bond, mid-bond, post-bond and final tests). For example, pre-bond testing of TSVs using probe pads affects the chip layout and chip area, while can detect some faulty TSVs prior to stacking [15]. Similarly, mid-bond testing requires dedicated hardware to support testing during this phase. These types of

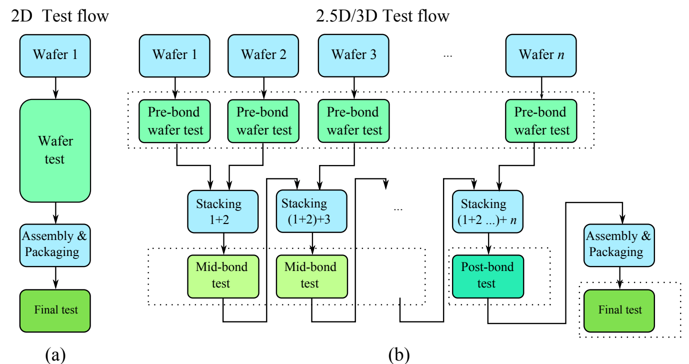

Fig. 2. 2D versus 2.5D/3D D2W test flows.

trade-off are strongly test flow dependent and must be decided at design time as they impact the design and its associated cost.

b) Manufacturing: Manufacturing requirements are related to the fabrication, processing of wafers and the stacking of tiers. As the manufacturing is not perfect, TSV yield, die yield, and stacking yield are required to accurately determine the cost. The manufacturing class covers a wide range of parameters and consists mainly of two parts: (a) manufacturing cost related to 2D IC and (b) cost related to 2.5D/3D stacking processing steps. The first part depends on the wafer cost, die yield, number of dies per wafer, cost of manufacturing steps, etc.; all of these results into a cost of a die per wafer. In case additional hardware is integrated for DfT, the number of dies per wafer reduces and therefore increases the chip cost. The second part depends on the cost of TSVs, wafer thinning, bonding (i.e., Die-to-Die (D2D), D2W and W2W), stacking process (i.e., Face-to-Face (F2F), Back-to-Face (B2F) or Back-to-Back (B2B)), interconnect yield, stacked-die yield, etc.; and it strongly depends on the applied test flow [13]. It is worth noting that the chosen bonding type and stacking process have a large impact on the cost and the yield of the 2.5D/3D-SIC; for instance, in D2D and D2W stacking, Known Good Dies (KGD) can be stacked on each other to maximize the yield. KGD stacking is is not applicable in W2W stacking and therefore generally results in lower yield [16,17]. For the 2.5D-SICs we assume dies to be stacked in a D2W F2F fashion. Moreover, as exact profiles of faults introduced during the stacking are not know/published yet, the tool is built such that it supports any defect distribution of dies during stacking.

c) Test: Figure 2(a) shows the conventional 2D test flow for planar wafers [18]; it consists of two test moments: a wafer test prior to packaging and a final test after packaging. The wafer test can be cost-effective when the yield is low as it prevents unnecessary assembly and packaging costs, while the final test is used to guarantee the final quality of the packaged chips. 2.5D/3D-SICs, however, provide additional test moments; e.g., additional test moments can be defined for each partial stack. Moreover, at each moment a distinction can be made between different tests such as die tests and interconnect tests. In general, four test moments can be distinguished for a 2.5D-SICs consisting of n dies as depicted in Figure 2(b):

(1) n *pre-bond* wafer tests, (2) n-2 *mid-bond* tests, (3) one *post-bond* test prior packaging and (4) one *final* test.
A *test flow* can be can be extracted from the above four defined test moments, which consist in total of $2n$ different moments. A test flow is as a collection of tests applied at these test moments. At each test moment, zero, one or more tests, possibly with different FCs, both for dies and/or interconnects, can be applied. Depending on the used test flow, the test cost might increase significantly. Therefore, skipping or reducing quality requirement at some test moments can restrain the test cost.
In addition, using advanced test equipment to reduce the test cost, parallel testing can be also used. Dies belonging to different layers can be tested in parallel if there is DFT support available for it. 3D-COSTAR does support the calculation of test cost for both simultaneous and serial testing of dies in a 2.5D or 3D-SIC.

The test cost can be company dependent as the quality of the applied tests could differ, e.g., for IDM and fab-less companies. For instance, depending on whether one or more companies are involved in the supply chain for the manufacturing of 2.5D/3D-SICs, different test requirements can be set for the pre-bond wafer test [19]. If the wafers are produced by one or more companies and the final 3D-SIC product is processed and manufactured by another company, a high pre-bond wafer test quality (e.g. a KGD) often is agreed upon. If a KGD contract is in place, high-quality pre-bond testing is required. If such a contract is not in place (e.g., for an IDM), the pre-bond test quality is subject to optimization. Hence, at pre-bond test moment, we can not only perform or skip the pre-bond test, but we can also tune the quality of the applied test for cost optimization. Faulty undetected dies at this test moment can be detected in a later test moment, e.g., when applying a higher quality test in the final test moment. Similarly, a high quality mid- or post-bond test can be applied.

3D-COSTAR calculates test cost for any possible test combinations (test flow). Both the type of test and the used test flow impacts the overall 2.5D/3D-SIC cost. Therefore, specifying an optimized test flow should be with full freedom, i.e., without any restrictions on the test moment, on the used test (die, interconnect or both), neither on the FC, etc. The complexity of the test flow depends on the number of test moments, which increase linearly with the stack size. Hence, 2.5D/3D-SICs could be probed several times. However, having several touch-downs on the bottom wafer for testing purposes can damage the bonding-bumps. Therefore, setting an upper limit of maximal allowed touch-downs is practical.

d) Packaging: After the 2.5D/3D-SIC is manufactured and perhaps tested (a post-bond test), the 2.5D/3D-SIC is assembled and packaged. The cost attributed to packaging depends on the used materials and technology [20]. We assume an independent cost for the packaging, i.e., it has no dependency with the other classes. Since all processing steps are defect-prone, a yield for the packaging has to be considered as well. In this paper, we further ignore the packaging cost as it is irrelevant for the performed experiments.

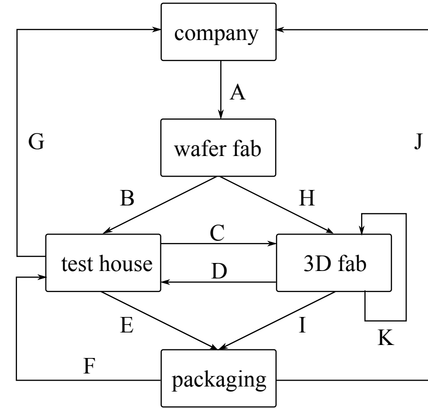

Fig. 3. Logistics cost for 2.5D/3D-SIC.

e) Logistics: The production of 2.5D/3D-SICs requires design, manufacturing, test and packaging costs. However, to make a distinction possible between fab-less, fab-lite and IDM companies, an additional set of hidden costs, referred to as logistics, is needed. For instance, a fab-less company may perform stacking and testing in different houses/countries, while IDM may perform all the required processing steps in a single house/location. Therefore, logistics costs are a direct consequence of moving dies and wafers between different locations. Figure 3 shows an overview of logistics costs considered in our tool. It presents all possible logistics costs for the worst case scenario in which each activity in the 2.5D/3D-SIC production chain can be outsourced; hence, the associated logistics costs have to be separated from each other. The figure assumes five companies/houses to be involved in the production chain: design company, wafer fab, 3D fab, test house and packaging house. A cost is associated to any moving activity of lots/wafers between any of these companies; for example, arrow B defines the cost for the logistics between wafer fab and test house. There are in total 11 possible costs.

It is worth noting that test flows have an impact on the logistics cost. Depending on the company type and test flow, some of the costs are not applicable. For example, in case pre-bond tests are skipped (arrow H), the cost associated with arrow B is inapplicable.

B. Use cases

Use cases define the functionality of the tool in terms of inputs and outputs. There are three main use cases.

1) *Overall cost calculation*. The primary goal of the tool is to calculate the overall cost of the production of 2.5D/3D-SICs for different test flows, based on pre-defined input parameters. The overall cost includes design, manufacturing, test, packaging and logistics cost.
2) *Cost breakdown*. The second use case is the analysis of the cost by breaking it down into design, manufacturing, test, packaging and logistics costs. This analysis reveals the share of each cost and provides insights about possible further cost optimization.

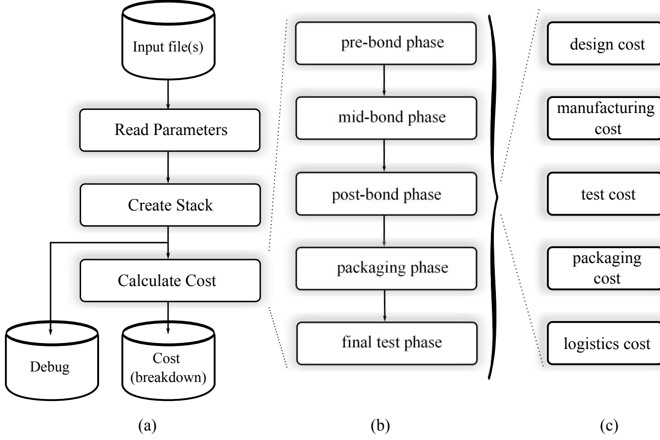

Fig. 4. Tool flow.

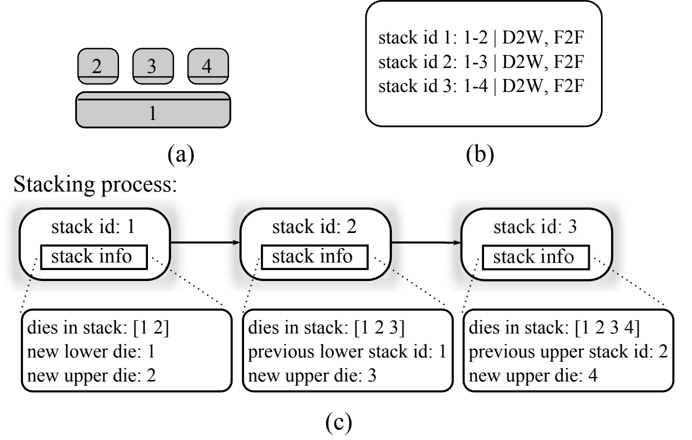

Fig. 5. Creating the stack.

3) *Sensitivity analysis*. The third use case is sensitivity analysis of input parameters; it identifies those parameters that have largest impact on the overall cost. Thus, tuning these parameters first results in largest cost reduction.

C. Tool Flow

Figure 4(a) presents a high-level overview of the tool flow. The tool starts by reading all input parameters from the input files and subsequently creating the stack. Thereafter, the cost is calculated by taking involved costs into consideration and moving through the IC production chain of the IC (see Figure 4(b)). At each step, the tool updates the impacted cost if applicable. For instance, if a mid-bond test is performed, then the test cost has to be updated. Reading the input parameters, creation of the stack and the cost calculation are the core steps of the tool. They are explained next.

Read parameters

The first stage of the tool reads the input parameters of each class. The parameters are specified by keywords and read from a file. For example, keywords that must be specified that are related to manufacturing are *die cost*, *die yield* etc.

Stack creation

Figure 5 shows an example of how the creation of a stack ta ly stored. Part (a) of the figure depicts a particular multiple tower stack IC. It consists of a bottom die/wafer labeled 1, a die labeled 2 stacked on die/wafer 1 using D2W stacking process with a F2F stacking orientation, followed by dies 3 and 4 in a similar manner. Part (b) of the figure, shows how this stack is defined. This particular stack consists of 3 stacking operations; each operation requires a specific stacking process and orientation. Figure 5(c) shows how the stack is internally stored. The stack is stored as an array of stacking operations. For example, after the first stacking operation (stack id: 1), the created stack consists of die 1 as a bottom/lower die and die 2 as an upper die. A debug file is created for verification.

Cost calculation

Given the input parameters, the different involved costs are calculated step by step by moving through the different phases shown in Figure 4. All costs are impacted by one of more of such phases. For example, pre-bond and mid-bond phases contribute to the manufacturing cost and requires DFT hardware (hence impacting the design cost as well), while these two phases together with post-bond phase and final phase contribute to test cost. The logistics cost strongly depends on the required number of movements of lots/wafers; e.g., between wafer fab, 3D stacking fab, test house, etc. The packaging cost is calculated based on the required packages for all the considered good stacked ICs (outgoing yield of the stack) after the post-bond test. The overall cost of 2.5D/3D-SIC is calculated by summing up all the cost of design, manufacturing, test, packaging and logistics.

Not all dies enter the stack. For instance, dies that are tested faulty in the pre-bond phase. To obtain the cost, the ratio of dies that enter the stack have to be calculated properly. We use Equation 1 to define the relation between test escapes TE, ingoing yield Y_{in} and outgoing yield Y_{out}; TE is the ratio of faulty dies that pass the test. The ingoing yield is the actual yield, the outgoing yield is the fraction of dies that is considered good after testing. Equation 2 [21] shows the relation between the test escapes, ingoing yield and the FC. By combining Equations 1 and 2 we obtain Equation 3, the outgoing yield as a function of the ingoing yield and FC.

$$TE = \frac{Y_{out} - Y_{in}}{Y_{out}} \quad (1)$$

$$TE(Y_{in}, FC) = 1 - Y_{in}^{1-FC} \quad (2)$$

$$Y_{out} = \frac{Y_{in}}{1 - TE} = \frac{Y_{in}}{Y_{in}^{1-FC}} = Y_{in}^{FC} \quad (3)$$

We assume that all these equations are valid for all yield operations involved in the manufacturing of the 2.5D-SIC; i.e, for the manufacturing of dies and interconnects. For instance, imagine that dies of type d_2 need to be stacked on the top of dies of type d_1 (see Figure 5); each die has its own yield and FC. If d_1 is total number of bottom dies, then the total number

of dies of type d_2 (say d_2) needed for the stacking will be:

$$d_2 = \frac{d_1 \cdot Y_{out,1}}{Y_{out,2}} \quad (4)$$

All cost and yield operations are based on the principle of updating partial or final stack yields. Consider the IC depicted in Figure 5(a). First, the outgoing yield of each die is calculated before stacking. Subsequently, the yields of the die in the stack are updated each time stacking a new die. Each time a new die enters an already existing partial stack, its quantity is determined by the combined outgoing yield of the dies in the stack. These steps are repeated until all dies are considered. The yields (pre-bond, mid-bond etc.) related to particular dies are tracked and stored individually. This allows us to detect faulty dies that escaped the pre-bond phase in a later stadium (mid-bond/final test). Once all partial and final stack yields are calculated, we can determine the number of dies, the number of tests and logistics for each individual die and partial/complete stack. To calculate the cost-price of a 2.5D-SIC, all costs involved in the production chain are attributed to good 2.5D-SICs only. For example, faulty detected dies in the pre-bond phase have also a manufacturing and test cost share in the overall cost.

III. Experimental Setup

This section describes the experiments performed in this work. Note that the yield and cost parameters considered for these experiments do not describe any processes at Qualcom, IMEC or partners, nor at TU Delft. The inputs of 3D-COSTAR are flexible and fully parameterized. By tuning these input parameters almost anything can be proven. Nevertheless, we provide inputs as realistic as possible. The experiments are performed for two types of applications; a mobile and FPGA application denoted by Case A and Case B respectively.

A. Reference Cases

This section describes the default parameter values of both applications. We assume that for both Case A and B the stack is composed out of four dies as depicted in Figure 5(a). For the mobile application, we assume the active dies to be heterogeneous (one big die and two smaller dies), while for the FPGA application all three active dies are identical. The parameters for both cases are summarized in Table I. In the table, Die 1 denotes the interposer and Dies 2,3 and 4 the active stacked dies.

First, we describe the parameters that are related to the pre-bond phase. As the interposer is passive (no FEOL processing) the wafer cost is much cheaper than the active dies which are usually implemented in the newest technology nodes. We assume standard 300mm diameter wafer with an edge clearance of 3mm, i.e., the effective radius equals 147mm. Wafers that contain interposer dies are assumed to cost 700$ only, while wafers with active dies cost 3000$.

For Case A (mobile application), we assume the passive interposer to be A=210mm^2, large enough to fit the active dies stacked on them. The big die is assumed to have an area of A=100mm^2, and the two smaller dies an area of A=50mm^2 each. For the given die areas and effective wafer radius, the number of gross dies per wafer (GDW) approximately equals to 293, 622, and 1283 [22] for the interposer, the large die, and the two smaller dies respectively. The defect density is considered to be d_0 = 0.5 defects/cm^2 for the silicon interposer (older technology and no FEOL) and 1.0 defect/cm^2 for the active dies, with both a defect clustering parameter $\alpha = 0.5$. The die yield can be estimated by the negative binomial formula as: $y = (1 + \frac{A \cdot d_0}{\alpha})^{-\alpha}$ [21]. This results into die yields of 56.80%, 57.74%, 70.71% for the interposer, the bigger die and two smaller dies respectively.

TABLE I
Default parameters Case A and Case B

Parameter	Case A Die 1	Case A Die 2	Case A Die 3/4	Case B Die 1	Case B Die 2/3/4
Wafer costs ($)	700	3000	3000	700	3000
Effective wafer radius (mm)	147	147	147	147	147
Die Area (mm)	210	100	50	460	150
Dies per wafer	293	622	1283	125	411
Defect density (cm^{-2})	0.5	1	1	0.5	1
Die yield (%)	56.80	57.74	70.71	55.05	50.00
Pre-bond FC (%)	100	99	99	100	99
Pre-bond test cost ($)	0.20	1.00	0.50	0.40	1.50
Stacking cost ($)	0	0.05	0.05	0	0.05
Stacked die yield (%)	99.5	99	99	99.5	99
Interconnect yield (%)	-	99	99	-	99
Mid-/post-bond FC (%)	0	0	0	0	0
Mid-/post-bond test cost ($)	0	0	0	0	0
Final FC (%)	100	99	99	100	99
Final test cost ($)	0.05	1.00	0.50	0.10	1.50

For Case B (FPGA application), the area of the three active dies is assumed to be A=150mm^2, while the interposer has an area of A=460mm^2. Using the same GDW algorithm and negative binomial yield formula the number of dies per wafer yields 411 and 125 with a yield of 55.05 and 50.00% for the interposer and three active dies respectively.

Further we assume a 100% FC for the interposer at a cost of 0.20$ for Case A and 0.40 $ for Case B. For the active dies we assume a test cost of 0.50$ for the smallest dies of 50mm^2, 1.00$ for the dies of 100mm^2 and 1.50$ for the dies of 150mm^2. In all cases, the FC for active dies is assumed to be 99%.

The next group of variables in the table contain parameters related to the mid-bond and post-bond. For both Case A and Case B we assume these parameters to be the same. Each time an active die is stacked on an interposer, the stacked-die yield (stack pass yield) of the active die is assumed to be 99%, while the stacked-die yield of the interposer is assumed to be 99.50%. The yield of the interconnects is assumed to be 99% (which includes the micro-bumps) between each pair of stacked dies, i.e., between Die 2, Die 3 or Die 4 and Die 1. Note that there are 3 stacking operations and 3 sets of interconnects. We assume no mid-bond testing for dies as well as interconnects for the reference cases.

In the final phase, we assume the same test costs for the active dies as in the pre-bond phase. However, we assume that

TABLE II
PROBE-PADS VERSUS MICRO-BUMPS FOR CASE A

	Probe-pads			Micro-bumps		
Parameter	Die 1	Die 2	Die 3/4	Die 1	Die 2	Die 3/4
Die Area (mm)	210	101	51	210	100	50
Dies per wafer	293	618	1254	293	622	1283
Die yield (%)	56.80	57.54	70.36	56.80	57.74	70.71
Pre-bond FC (%)	100	99	99	100	99	99
Pre-bond test cost ($)	0.20	10.00	5.00	0.40	1.05	0.55
Interconnect yield (%)	-	99	99	-	98	98
Final FC (%)	100	99	99	100	99	99
Final test cost ($)	0.05	1.00	0.50	0.10	1.00	0.50

TABLE III
PROBE-PADS VERSUS MICRO-BUMPS FOR CASE B

	Probe-pads		Micro-bumps	
Parameter	Die 1	Die 2/3/4	Die 1	Die 2/3/4
Die Area (mm)	460	151	460	150
Dies per wafer	124	404	124	406
Die yield (%)	55.05	49.88	55.05	50.00
Pre-bond FC (%)	100	99	100	99
Pre-bond test cost ($)	0.40	15.00	0.40	1.55
Interconnect yield (%)	-	99	-	98
Final FC (%)	100	99	100	99
Final test cost ($)	0.10	1.50	0.10	1.50

testing the interposer (Die 1) is less expensive, as they can be tested by an EXTEST [23]. For Case A this cost is assumed to be only 0.05$, while for Case B 0.10$. Note that the test cost for interconnects (including micro-bumps) is not mentioned in the table as they are tested through the interposer die. We assume a 100% default FC for interconnects.

B. Experiments

The values presented in the previous section form the default parameters of each experiment. We explain the experiments in more depth and examine the relevant parameters for each case study. The three experiments are as follows.

1) Impact of the FC of pre-bond test of the interposer.
2) The use of probe-pads versus micro-bump probing.
3) Impact of mid-bond testing and logistics.

The experiments are described in the next sections, and apply both to Case A and Case B. Note that these experiments are only a small subset of what 3D-COSTAR can do.

Impact of the FC of interposer pre-bond testing: In this experiment, the impact of pre-bond testing for the passive silicon interposer is examined. The experiment considers a variable FC for the interposer test, i.e, between 0% and 100%. Similarly, we assume the test cost to scale linearly in the range between 0.00$ and 0.20$ for Case A, e.g., if the FC is 50% then the value of the interposer test cost is 0.10$. The reason for the linear relation is because the interposer consist of wires only.

The remainder parameters are considered to be the same as the reference case described in Table I. For Case B, the relation between test cost and FC for the interposer is applied in a similar manner (0.40$ for 100% FC).

Probe-pads versus Micro-Bump probing: In this second experiment, we investigate the trade-off between pre-bond tests probing dedicated pads and micro-bumps [24] for the active dies. As the active dies have no I/O pads, testing these dies in the pre-bond phase should be performed by one of the two methods. Table II and III show the parameter values that changed with respect to the reference case for Case A and Case B respectively. The extra probe-pads for pre-bond testing occupy additional area and this has to be accounted for. We consider for example the wide-IO memory [25] where 1200 micro-bumps are placed and assume only 10% of these microbumps (i.e. 120) have dedicated probe-pads of size $80\mu m$ by $80\mu m$. Note that if more probe-pads are considered, it will increase the die area. We can estimate the area of these 120 dedicated pads to add an extra area of $120{\cdot}80\mu\text{m}{\cdot}80\mu\text{m} \approx 1\text{mm}^2$. This extra die area impacts the die yield and GDW as shown in the second columns of the tables. For example, for the bigger die of Case A the number of dies that decreases from 622 to 618 if dedicated pads are added, while the yield reduces from 57.74% to 57.54%. Similarly, the table shows the numbers for the other dies. Moreover, as there only 10% of the micro-bumps are used as probe-pads, the pre-bond test cost of the active dies is assumed to be 10 times more expensive as compared to that of the reference case.

For the micro-bump probing we assume that a micro-bump probe-card cost 50k$ for 1 million touch downs. This results into an additional test cost of 0.05$ for each active die in the pre-bond phase. Moreover, as micro-bump touchdowns can cause later defects in the interconnections, we assume the interconnect yield to be 1% less (i.e., 98% instead of 99%) as compared to the case were extra probe-pads are used.

Impact of Mid-Bond Testing and Logistics: In order to investigate the impact of mid-bond testing and logistic cost we consider the following three sub-cases for both Case A and Case B:

1) No mid-bond testing and no logistic cost (reference case)
2) Mid-bond testing and no logistic cost.
3) Mid-bond testing and logistic cost.

We assume the FC and test cost for the mid-bond tests to be same as their values in the final test. For the logistics, we attribute costs to applicable arrows of Figure 3. We assume the cost of moving a single wafer (independent of the number of dies stacked on it) per arrow to be in the range of 1% up to 10% of the wafer manufacturing cost.

IV. SIMULATION RESULTS

This section describes the results of the three experiments.

A. Experiment 1

Figure 6 shows the impact of variable pre-bond interposer FC on the overall 2.5D-SIC cost for Case A and B. The results clearly show that performing a high quality interposer pre-bond tests realizes a significant relative cost reduction; the higher the FC the higher the cost reduction. Moreover, the results reveals that the larger the dies the higher the relative cost reduction; for instance, in Case B (with larger dies) the relative cost reduction is about 52%.

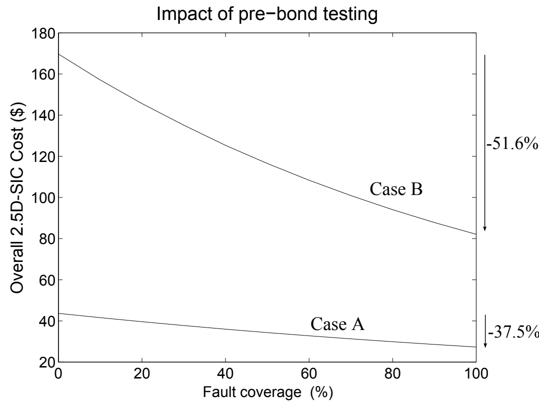

Fig. 6. Impact of pre-bond interposer FC.

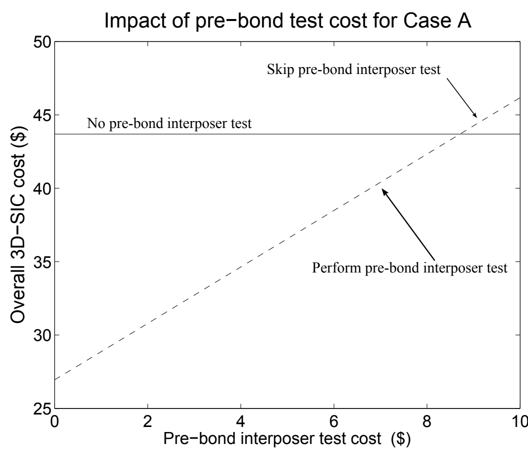

Fig. 7. Break-event cost point for Case A

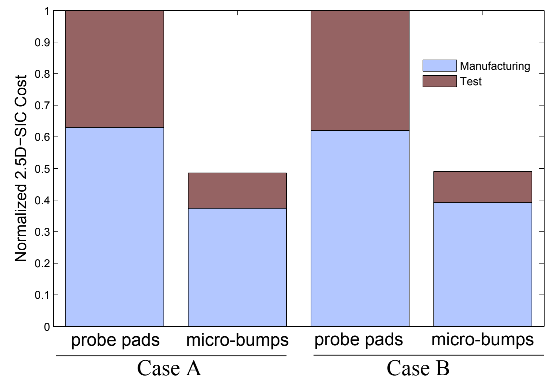

Fig. 8. Dedicated probe pads vs micro-bump probing.

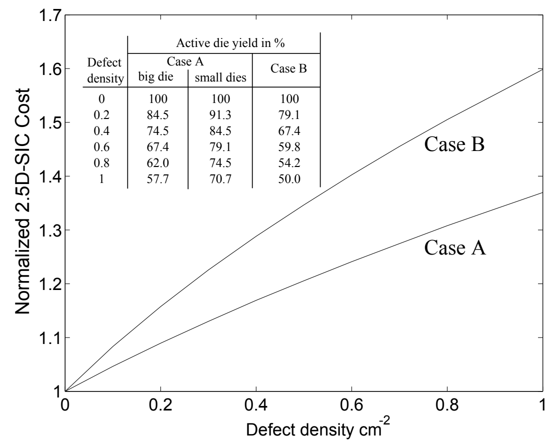

Fig. 9. Impact of defect density on Experiment 2.

However, testing of interposers is still a major challenge; cheap and efficient DFTs are still missing. Therefore, it is worth to analyze (for the given parameters) the break-even cost point where testing the interposer leads to the same overall cost as where no test is performed. This trade-off is depicted in Figure 7 for Case A. The figure contains two lines; the horizontal solid line shows the overall cost in case no pre-bond testing is performed and the dashed rising line shows the overall cost for variable pre-bond interposer cost for 100% FC. Note that for this particular case, the break-even point is around 8.50$. Hence, it is worth to use pre-bond test with maximal FC only if the associated test cost is below this threshold. Similar analysis has done for Case B; the break-even point found to be around 33.00$.

B. Experiment 2

The second experiment considers the analysis of test trade-off between dedicated probe pads and micro-bump probing. Figure 8 reports the results of such analysis; it shows the normalized 2.5D-SIC costs for both cases. Irrespective of the case, additional pads for testing result in higher overall cost, mainly due to test cost increase (as the cost break down shows), but also due to a slight yield loss (extra area of the pads). Moreover, the results show that the expensive probe-cards seems to pay off. The cost break down shows that largest share of costs are due to manufacturing of dies (around 80% in case micro-bumps and around 65% in case probe/extra pads). Note that the difference in the overall cost between using micro-bumps and probe pads is about 50%. This cannot justified with the difference in pre-bond test cost only; there are hidden costs primarily due to the faulty dies thrown away in the pre-bond phase. Therefore, it is important to analyze this behavior for different die yields. We performed a sensitivity analysis for the defect density. Figure 9 shows the results for both cases. As the defect density increases (i.e., the die yield reduces) the overall cost increases. The die yields that correspond to the defect density values are depicted in the table at the top left of figure. The impact of the die yield is more severe for Case B as the dies are larger and more expensive.

C. Experiment 3

Figures 10 and 11 shows the relative cost increase if mid-bond testing and/or logistics are considered; the results are given for various stacked-die Y_{SD} and interconnect yield Y_{INT}.

The figures contain four planes; the non-labeled planar planes shows the normalized base-line (i.e., no mid-bond test and no logistic cost), while the other labeled planes describe the results of the cases where mid-bond testing is performed; Planes 1, 2 and 3 show the impact of the logistics cost when assuming such cost to be 0%, 1% and 10% of the wafer cost respectively. From the figures we conclude the following:

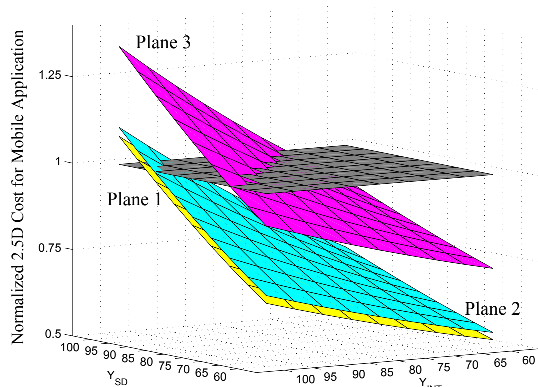

Fig. 10. Impact of mid-bond testing for Case A.

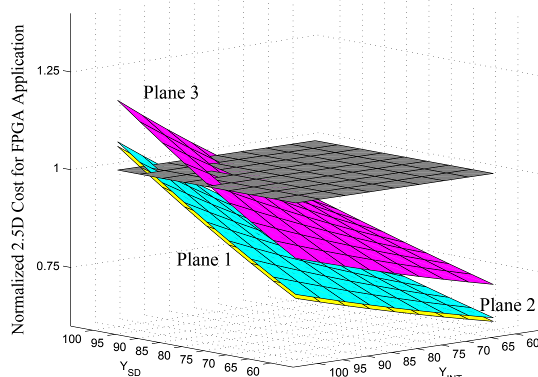

Fig. 11. Impact of mid-bond testing for Case B.

- Irrespective of logistic costs, mid-bond testing can be avoided if the stacked-die yield and the interconnect yield are high; in our case study higher than $> 90\%$. It is worth noting that the simulation has been done while considering an intensive pre-bond test both for interposer (100%) and active dies (99%).
- Logistics cost has a minor impact on the overall cost if they are low. However, they can substantially increase the overall cost if they are high (e.g. 10% of the wafer cost).

The results of all the experiments clearly show that optimizing the overall/test cost is a complex task; it strongly depends on the test flow, FC of each test, different yield components, etc. Therefore using a tool such as 3D-COSTARis extremely important to make appropriate trade-offs at an early stage in the design and optimize overall cost.

V. Conclusion

In this paper, 3D-COSTAR was introduced and used to evaluate different test flows and strategies for 2.5D-SICs; the tool considers all costs involved in the production (including design, manufacturing, testing, packaging and logistic) and produces the overall cost as well as the cost breakdown.

The case studies presented in the paper showed the significant importance of using such a tool in order to make appropriate trade-offs for overall cost optimization. For example, the simulation results showed that when appropriate test strategies (test flow and FC) are used for given design and manufacturing parameters, the overall cost can be reduced. Pre-bond testing of the interposer die is important for overall 2.5D-SIC cost reduction; using micro-bump probing results in much lower overall cost as compared to probe-pads; mid-bond testing can be avoided for high stacking yield.

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