Impact of Mid-Bond Testing in 3D Stacked ICs

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***Abstract*— In contrast to planar ICs, during the manufacturing of three-dimensional stacked ICs (3D-SICs) several tests such as pre-bond, mid-bond, post-bond and final tests can be applied. This in turn results into a huge number of test flows/strategies. Selecting appropriate and efficient test flow (for given design and manufacturing parameters such as stack size, die yield, stack yield, etc) is crucial for overall cost optimization. To evaluate the test flows, a case study is performed in which 3D-COSTAR is used to compare the overall cost of producing a 3D-SIC using variable fault coverage during the mid-bond tests. In addition, we investigate the impact of the logistics cost for various test flows. The impact of logistics costs depend on the outsourced processing steps during the manufacturing. Simulation results show, for our parameters, that by choosing an appropriate test flow the overall 3D-SIC cost for appropriate fault coverages can reduce the overall cost up to 20% for a 5-layered 3D-SIC with die yields of 90%.**

Keywords: *3D integration, cost modeling, test cost, test flows.*

I. Introduction

Tremendous effort has been put in place to bring *Through Silicon Via (TSV)* based 3D-SIC technology closer to market [1–3]. Realizing such ICs is attractive due to major benefits [4] such as (a) increased electrical performance, (b) reduced power consumption due to shortened interconnects, (c) heterogeneous integration supporting optimized logic, memory, RF, MEMs etc., and (d) reduced form factor, etc. The mentioned benefits therefore drive the production of a new generation of 3D chips.

One of the major challenges that has to be addressed in order to make this technology commercially successful is testing. As is the case for any IC, TSV-based 3D-SICs must be tested in order to guarantee the outgoing product quality and reliability. Therefore, making test cost an indispensable part. Inherent to their manufacturing process, 3D-SICs provide several test moments such as before stacking, during manufacturing of partial stacked IC, after the complete manufactured stack, etc. This results into a huge space of test flows; each with its own cost. Determining the optimal and most efficient test flow requires analysis of all test flows, as different design and/or manufacturing parameters may impact the cost differently. Therefore, an appropriate cost model is required.

In this paper, we use 3D-COSTAR to evaluate 3D test flows [5,6]. In [5], we presented a preliminary version of our tool that had many limitations, such as lack of support for variable fault coverage, logistics cost etc. These limitations have been addressed in [6]. The tool is based on a cost model

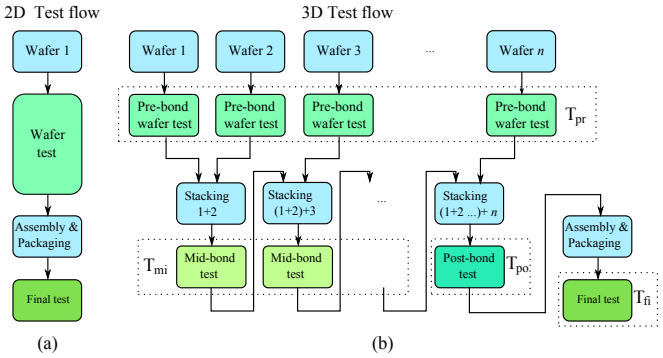

Fig. 1. 2D versus 3D D2W test flows.

considering all costs involved in the 3D-SIC production chain including design, manufacturing, test, packaging and logistics; the logistics costs are due to transport of wafers and dies between different companies during the 3D-SIC production chain. As a case study, the tool is used to evaluate different test flows for 3D-SICs primarily focusing on variable fault coverage during pre- and mid-bond testing. Note that mid-bond testing (partial stack testing) could impact logistics cost, as tiers have to be transported to testers. The main contribution of this paper are as follows.

- To our best knowledge, we are the first to experiment with test flow analysis for 3D-SICs with variable fault coverage during pre-bond and mid-bond testing.
- We investigate and analyze the impact of two logistics models on the overall 3D-SIC cost.

The rest of this paper is organized as follows. Section II provides the background of this paper; it discusses the difference between 2D and 3D test flows and briefly explains 3D-COSTAR. Section IV analyzes the impact of variable fault coverage on the overall 3D-SIC cost. Subsequently, Section V analyzes the impact of logistic costs. Finally, Section VI concludes the paper.

II. Background

A. 2D versus 3D Testing

Figure 1(a) shows the conventional 2D test flow for planar wafers [7]; it consists of two test moments: a wafer test prior to packaging and a final test after packaging. The wafer test can be cost-effective when the yield is low as it prevents unnecessary assembly and packaging costs, while the final test is used to guarantee the final quality of the packaged chips. 3D-SICs, however, provide additional test moments;

e.g., additional test moments can be defined for each partial stack. Moreover, at each moment a distinction can be made between different tests such as die tests and interconnect tests. In general, four test moments can be distinguished for 3D-SICs as it is depicted in Figure 1(b); they are explained next.

1) T_{pr}: n *pre-bond* wafer tests, since there are n layers to be stacked. T_{pr} tests prevent faulty dies entering the stack. Besides die test, preliminary TSV interconnect tests can be applied. Several research work already exists regarding this topics; e.g., in [8] the authors use a capacitance test to detect some of the faulty TSVs and in [9] the authors propose active probing to detect faulty TSVs.
2) T_{mi}: n-2 *mid-bond* tests applicable for partial created stacks. In this case, either the dies, the interconnects, their combinations or none of them can be tested. Good tested dies in the pre-bond test phase could get corrupted during the stacking process as a consequence of e.g., die thinning, and bonding [10].
3) T_{po}: one *post-bond* test. This test can be applied after the complete stack is formed. Analogous to wafer testing in the 2D test flow, T_{pr} can be applied to save unnecessary assembly and packaging costs. Both interconnects and dies can be tested.
4) T_{fi}: one *final* test can be applied after assembly and packaging to ensure the required quality of the complete 3D-SIC. Other specific packaging related tests could be applied at this test moment as well.

A *test flow* can be can be extracted from the above four defined test moments, which consist in total of $2n$ different moments. A test flow is as a collection of tests applied at these test moments. At each test moment, zero, one or more tests, possibly with different fault coverages, both for dies and/or interconnects, can be applied. Depending on the used test flow, the test cost might increase significantly. Therefore, skipping or reducing quality requirement at some test moments can restrain the test cost.

B. 3D-COSTAR

This section describes the high level architecture of 3D-COSTAR. In order to determine the most cost-effective test flow, the test requirements should be specified. However, taking only the test cost into consideration is not sufficient to provide a fair comparison between the different test flow. This is because a test flow does not only impact test cost, but also manufacturing cost and even design cost.

As already mentioned, a pre-bond TSV test requires additional DFT hardware (which might not be reused after stacking), while it prevents faulty dies (due to defects in TSVs) to enter in the stack if detected. As a consequence, the die area increases (less dies per wafer).

Figure 2 shows the general architecture of 3D-COSTAR. The tool has five classes of inputs which reflect the cost involved in the whole 3D-SIC production; these include design cost, manufacturing cost, test cost, logistics cost and packaging

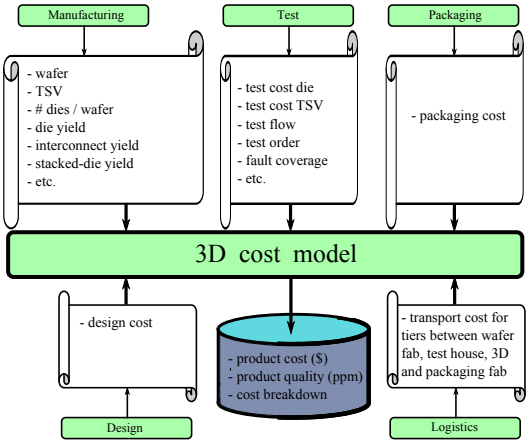

Fig. 2. 3D-COSTAR Organization.

cost. We briefly review the requirements associated with each input class.

a) Design: Design for Testability (DfT) starts at the design phase to accommodate for tests at later stages (pre-bond, mid-bond, post-bond and final tests). Therefore, it is necessary to determine the impact of 3D test flows at this stage. For example, pre-bond testing of TSVs using landing pads affects the chip layout and chip area, while can detect some faulty TSVs prior to stacking using capacitance tests [8]. Similarly, mid-bond testing requires dedicated hardware to support testing during this phase. These types of trade-off are strongly test flow dependent and must be decided at design time as they impact the design and its associated cost.

b) Manufacturing: Manufacturing requirements are related to the fabrication, processing of wafers and the stacking of tiers. The first part depends on the wafer cost, die yield, number of dies per wafer, cost of manufacturing steps, etc.; all of these results into a cost of a die per wafer. In case additional hardware is integrated for DfT, the number of dies per wafer reduces and therefore increases the chip cost. The second part depends on the cost of TSVs, wafer thinning, bonding (i.e., Die-to-Die, Die-to-Wafer and Wafer-to-Wafer), stacking process (i.e., Face-to-Face (F2F), Back-to-Face (B2F) or Back-to-Back (B2B)), interconnect yield, stacked-die yield, etc.; and it strongly depends on the applied test flow [5]. It is worth noting that the chosen bonding type and stacking process have a large impact on the cost and the yield of the 3D-SIC; for instance, in D2D and D2W stacking, Known Good Dies (KGD) can be stacked on each other to maximize the yield. This is not applicable in W2W stacking and therefore generally results in lower yield [11,12]. Moreover, as the exact profile of faults introduced during the 3D stacking is not know/published yet, the tool is built such that it supports any fault distribution during the stacking.

c) Test: The test class defines the test flows as defined in II-A. We will slightly redefine a test flow; a test flow defines what to test (dies or interconnect) and when to test them. A test flow consists of the following attributes:

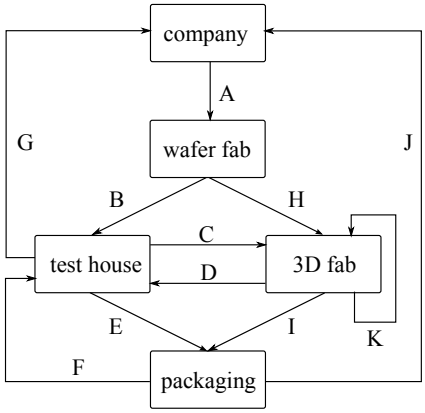

Fig. 3. Logistics cost for 3D-SIC.

- test moments: for each test phase (pre-, mid-, post-bond and final) test you can apply or skip tests for all dies.
- test contents: each time a test is performed the user can specify whether TSVs (restricted to pre-bond only), interconnects or dies are tested. In addition, the user also must define the quality of the tests in terms of fault coverage for each sub-test.
- test order: the test order tell us for each phase the order the sub-tests for dies and interconnects are performed.

In this work, interconnects are assumed to be tested prior dies (in case both are tested for); therefore, if a fault is detected in the interconnects then there is no need to test the dies as the 3D-SIC will is faulty. The reason to test interconnects first is because it is assumed to be cheaper as compared to die tests and vertical interconnects must be working properly in order to access the upper layer(s).

d) Packaging: After the 3D-SIC is manufactured and perhaps tested (a post-bond test), the 3D-SIC is assembled and packaged. The cost attributed to packaging depends on the used materials and technology [13]. We assume an independent cost for the packaging, i.e., it has no dependency with the other classes. Since all processing steps are defect-prone, a yield for the packaging can be considered as well.

e) Logistics: The production of 3D-SICs requires design, manufacturing, test and packaging costs and all of these must be considered as possible input parameters of the tool as depicted in the figure. However, to make a distinction possible between fab-less, fab-lite and IDM companies, an additional set of requirements, referred to as logistic, are needed. For instance, a fab-less company may perform stacking and testing in different houses/countries, while IDM may perform all the required processing steps in a single house/location. Therefore, logistics costs are a direct consequence of moving dies and wafers between different locations. For example, between the wafer fab, test house and 3D stacking fab.

Figure 3 shows an overview of logistics costs considered in our tool. It presents all possible logistics costs for the worst case scenario in which each activity in the 3D-SIC production chain can be outsourced; hence, the associated logistics costs have to be separated from each other. The figure assumes five companies/houses to be involved in the production chain: design company, wafer fab, 3D fab, test house and packaging house. A cost is associated to any moving activity of lots/wafers between any of these companies and is denoted by an arrow with a letter. There are in total 11 possible costs; they are explained next. It is worth noting that test flows have a large impact on the logistics cost. Depending on the test flow, some of the costs are not applicable. For example, in case pre-bond tests are skipped (arrow H), the cost associated with arrow B is inapplicable. Furthermore, depending on the type of the company producing 3D-SICs, some of these values can be not applicable or equal to zero. For example, if a company performs both testing and stacking in-house, costs associated with arrows C and D are zero.

III. Reference process

This section discusses the most relevant parameters for each input class that are used in our experiments.

Manufacturing cost: Manufacturing cost consists of cost related to wafer/die, cost related to TSVs and cost related to stacking process.

Wafer/die cost depends on several parameters, e.g., stack size, die yield, number of dies per wafer, stacking yield, interconnect yield, etc. We consider a stack size n=5 where dies are stacked in a D2W fashion, in which the dies are identical in terms of yield and cost. The yield of the dies is based on the reference process in [11], where a standard 300 mm diameter wafer is used with an edge clearance of 3 mm. This work assumes a defect density of d_0 = 0.5 defects/cm^2 and a defect clustering parameter $\alpha = 0.5$. With a die area $A = 50\ mm^2$, the number of Gross Dies per Wafer (GDW) are estimated to be 1283 [14]. With the negative binomial formula for yield, a die yield of $Y_D = (1 + \frac{A \cdot d_0}{\alpha})^{-\alpha}$ = 81.65% is expected [15]. To estimate the cost to manufacture and process a wafer we use the cost model of [16]; the total price of a 300 mm wafer is estimated at approximately \$2779. The model in [16] considers a variety of costs, including installation, maintenance, lithography and material.

For the cost of manufacturing TSVs, we base our numbers on the work of EMC-3D consortium reported in [5]; the cost of fabricating 5 μm TSVs on a single wafer cost \$190 and these cost are additive to the wafer cost. We assume the cost of manufacturing TSVs to be 60% of the 3D stacking process cost [17]. Further, we assume the TSVs to have a yield of 98% per die.

The 3D stacking process cost (including bonding, thinning etc..) is assumed to be \$126 (40% of total 3D cost) [17]. In addition, the stacking yield is assumed to be composed of two parameters: the interconnect (TSV) yield Y_{INT} and the stacked-die yield Y_{SD}. In our simulations, the interconnect yield Y_{INT} is considered to be 99%. For the good dies that enter the stack, a small probability exists that they get

TABLE I

FAULT COVERAGE VERSUS TEST COST.

fault coverage (%)	ratio test cost (%)	test cost ($cent)
100	100	23
95	28	6.44
85	13	2.99
75	3	0.69
0	0	0.00

corrupted during stacking; this is modeled by the stacked-die yield Y_{SD} and is assumed to be 99%. In [11], a stack yield of approximately 96% is used.

It is worth noting that for our case-study, we assumed that during the stacking only the *top* two dies and the interconnect between them could be corrupted; they are assumed to be defect-prone to stacking/bonding steps like heating, thinning, pressure.

Test cost: To estimate the test cost per die, the model in [15] is used; the model includes depreciation, maintenance and operating cost and assumes five ATE machines operating simultaneously. The derived test cost equals 3.82 $cent/second per die. Assuming a test time of 6 seconds per die, the test cost will be $0.23 per die. We attribute this test cost to a 100% fault coverage. Table I shows the relation between the fault coverage and die test cost [15] for the remaining considered fault coverage values. In [9], the authors estimate a test time of 80 μs to estimate 10000 TSVs using active probing. Hence, we ignore the test cost for pre-bond TSV test. We assume a pre-bond TSV fault coverage of 100%.

For the interconnects between the die, a test cost ratio of 1:100 with respect to the die cost is assumed (as in [11]). For the interconnects a fault coverage of 100% is assumed as well. We assume the fault coverage in the post-bond and final-test to be 100% to prevent faulty packaged ICs and to guarantee the final product quality.

Logistics cost: As discussed in Figure 3, there are many costs related with transportation of tiers during the production of 3D-SICs. For the default process, we assume zero cost for logistics.

Packaging cost: The packaging cost for 3D SICs used in our model is assumed to be 1.25 dollar per 3D-SIC [18]. The costs are comprehensive and include machine, maintenance, labor and material cost. We assume a 100% packaging yield, therefore impacting all the test flows in the same way.

IV. IMPACT OF VARIABLE FAULT COVERAGE

In this section, we analyze the impact of variable fault coverage on the overal 3D-SIC cost. Section IV-A lists the performed experiments. Section IV-B presents and discusses the impact of variable fault coverage. Note that because of space limitations we focus only on the overall cost rather then on the cost break down.

A. Experiments performed

We compare the overall cost of a 3D-SIC by performing the following three experiments given next for the test flows.

TABLE II

FAULT COVERAGE FOR DIFFERENT TEST FLOWS

	Test Flow number											
	1	2	3	4	5	6	7	8	9	10	11	12
pre-bond	100	100	100	95	95	95	85	85	85	75	75	75
mid-bond	100	85	0	100	85	0	100	85	0	100	85	0

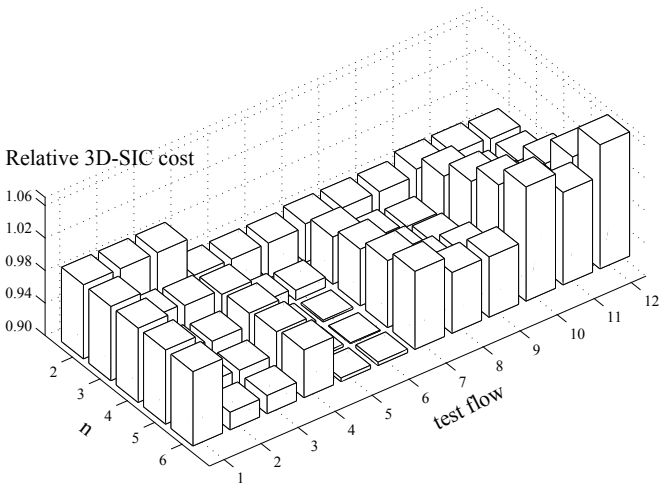

Fig. 4. Impact of variable stack size.

1) **Impact of variable stack size**: The experiment considers a stack size $2 \leq n \leq 6$.
2) **Impact of variable die yield**: The experiment considers a die yield $0.6 \leq Y_d \leq 0.9$.
3) **Impact of variable stack yield**: The experiment considers an interconnect yield $0.91 \leq Y_{INT} \leq 0.99$, and a stacked-die yield $0.91 \leq Y_d \leq 0.99$.

Each experiment is performed for 12 test flows; each test flows consists of the following tests:

1) Pre-bond tests: we assume tests with variable fault coverage for pre-bond testing; see Table II; for example, for test flow 4 we assumed FC=95%.
2) Mid-bond tests: Similarly, as in the pre-bond, we assume again variable FC in this test phase; see Table II; for example, test flows 3, 6 and 9 have no mid-bond test at all while test flows 2, 5, 8, 11 have FC=85%.
3) Post-bond and final tests: The FC for both tests is assumed to be 100%. This to prevent faulty packaged ICs and to guarantee the final product quality.

B. Simulation Results

The section describes the results of the three experiments.

Impact of variable stack size: Figure 4 depicts the relative cost of producing a 3D-SIC for the 12 test flows for stack sizes $2 \leq n \leq 6$; the cost is normalized to Test Flow 1 (TF1). Inspecting Figure 4 reveals the following conclusions.

- Depending on the stack size and the chosen test flow, the overall cost of 3D-SIC increases or decreases for different test flows.
- For a given stack size, the overall cost can be optimized by choosing appropriate test flow combined with appropriate pre-bond and mid-bond fault coverage. For example, for n=3, 4, 5 or 6, the cost is optimal when

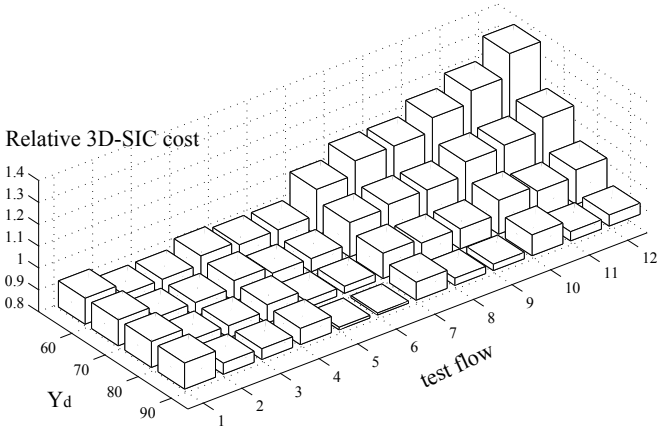

Fig. 5. Impact of variable die yield.

using TF6 with a pre-bond fault coverage of 95% and a mid-bond fault coverage of 0%. A cost reduction of almost 20% can be obtained for a stack size n=6 with respect to TF1.

- Having a pre-bond fault coverage of 100% does not always results in optimal overall cost. In our case, the optimal cost is realized for a pre-bond fault coverage of 95% (TF6).
- Having a mid-bond fault coverage of 100% or a fault coverage of 0% does not always results in optimal overall cost. In our case, the optimal cost is realized for a mid-bond fault coverage of 0% (TF6).

Impact of variable die yield: Figure 5 shows the normalized cost of a 3D-SIC for the 12 test flows for variable die yield $60\% \leq Y_d \leq 90\%$. Inspecting Figure 5 reveals the following conclusions.

- The overall cost depends significantly on the die yield and the chosen test flow. For example, in case the die yield equals 60% TF2 performs best. However, for higher die yields (70% and higher) TF6 peforms best.
- Choosing appropriate values for the pre-bond and mid-bond fault coverage that leads to optimal costs reduction is die yield dependent.

Impact of variable stack yield: Figures 6 and 7 depict the relative cost of a 3D-SIC for the 12 test flows for variable stacked die yield $91\% \leq Y_{SD} \leq 99\%$ and variable interconnect yield $91\% \leq Y_{INT} \leq 99\%$ respectively. Inspecting Figure 6 reveals the following conclusions.

- Depending on the stacked-die yield and the selected test flow, the overall cost significantly depends on the quality of the mid-bond test. For example, test flows with no mid-bond testing (TF3, TF6, TF9 and TF12) result in higher overall cost for lower stacked-die yields.
- For high stacked-die yields (>95%) experiment TF6 performs best. However, for stacked-die yields equal to 95% and lower TF5 results in lowest costs and mid-bond testing pays off.

Figure 7 reveals the following conclusions.

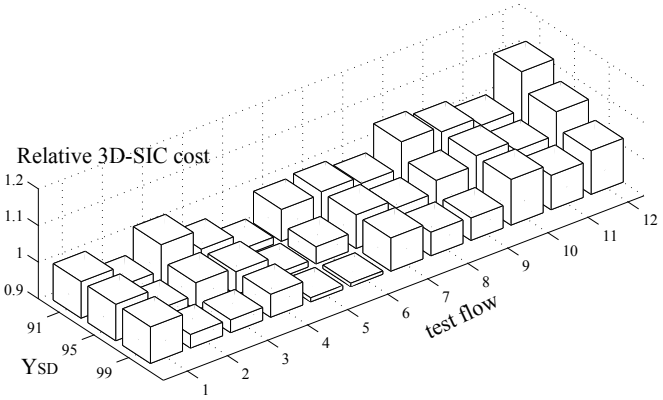

Fig. 6. Impact of variable stacked-die yield.

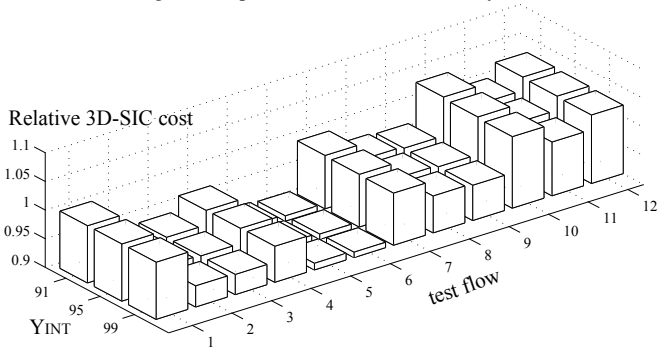

Fig. 7. Impact of variable interconnect yield.

- As the fault coverage for the interconnects is constant and 100%, the relative costs are almost independent of the test flow.
- Relatively, to TF1, the impact of the interconnect yield is almost constant. The reason for this is that we do not modify the interconnect fault coverage. Note however, that the absolute costs for TF1 change for different interconnect yield.
- In this experiment, TF6 always results in overall optimal 3D-SIC cost. Note that the considered interconnect yield is considered to be larger than 91%.

V. Impact of Logistics costs

In this section, 3D-COSTAR will be used to evaluate the impact of logistic cost using the most important tests flows presented in the previous section. The impact of logistic costs is company dependent. For example, the cost for logistics for an IDM company which has all its activities in-house (i.e., manufacturing, testing and packaging) and a fab-less company which outsources its activities are different.

We assume two different models for the logistics cost. In the first model, referred to as the extensive model, we assume non-zero values for all arrows in Figure 3. For the test flows with no mid-bond testing such as TF3, appropriate zero cost values will be for example assigned to arrow D as this arrow is not applicable for this case. For the second model, we assume a reduced logistics model in which some of the activities are joint. Figure 8 shows this model with the applicable arrow labels of Figure 3. In this model, the

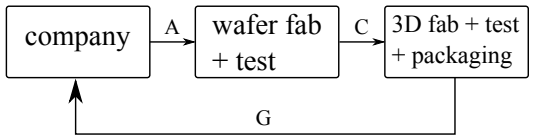

Fig. 8. Reduced logistics model.

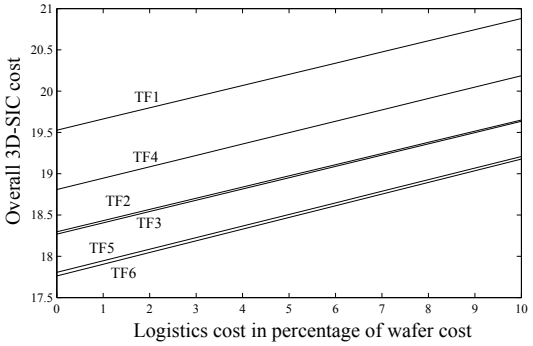

Fig. 9. Impact of extensive logistics cost model.

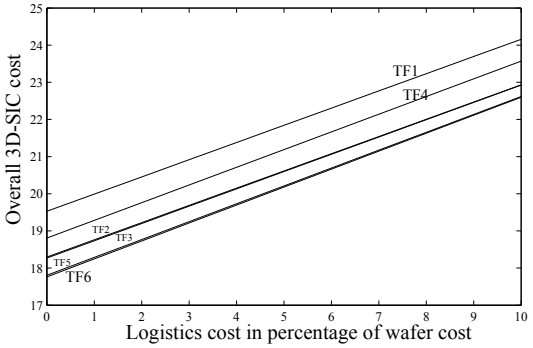

Fig. 10. Impact of reduced logistics cost model.

foundry is responsible for manufacturing the wafer and the OSAT for the remaining steps [19].

We assume the cost to move a single wafer between any to fabs between 0% and 10% of the manufacturing cost of a single wafer (i.e., for each of the involved arrows in Figures 3 and 8), regardless of the stack size.

Figures 9 and 10 show the impact on the overall 3D-SIC cost of variable logistics cost for the reduced and extended logistics cost model; this is performed for the most relevant test flows TF1 up to TF6 of the previous section. Both graphs have the same 3D-SIC cost when the logistics cost is 0%. The figures reveal that (a) with increased logistics cost, the impact of the extensive logistics model on the overall 3D-SIC cost is larger; and (b) the impact of logistics is nearly independent of the test flow, i.e., the slopes of the lines are similar.

In order to optimize the overall test cost, an appropriate test flow should be selected depending on the manufacturing and design parameters. A tool such as 3D-COSTAR can a have an added value in making appropriate trade-offs.

VI. Conclusion

In this paper a tool, 3D-COSTAR, is used to evaluate the different test flows for 3D-SIC; the tool considers all costs involved in the 3D-SIC production (including design, manufacturing, testing, packaging and logistic) and produces the overall cost. As a case study, 3D-COSTAR was used to compare the overall cost of producing a 3D-SIC for variable fault coverage. As mid-bond testing increases the amount of wafer transport, we investigate the impact of logistics as well. Our results show that the optimal test flow strongly depends on design, manufacturing and test parameters such as stack size, die yield, stack yield, fault coverage, etc. In addition, the impact of two logistics models on the most relevant test flows show that as long as the transports costs per single wafer are low, the overall impact of the logistics is relatively minor.

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