BTI Impact on SRAM Sense Amplifier

Innocent Agbo Seyab Khan Said Hamdioui
Delft University of Technology
Faculty of Electrical Engineering, Mathematics and Computer Science
Mekelweg 4, 2628 CD Delft, The Netherlands
{I.O.Agbo, M.S.K.Seyab, S.Hamdioui}@tudelft.nl

***Abstract*—Bias Temperature Instability (BTI) -Negative BTI in PMOS and Positive BTI in NMOS transistors- has become a key reliability bottleneck in the nano-scaled era. This paper presents BTI impact on SRAM's sense amplifier of different technologies, a robust sense amplifier has a lower sensing delay and higher sensing voltage. The results show that as technology scales down (i.e., from 90nm to 65nm, and 45nm), BTI impact on sensing delay increases, while that on the sensing voltage decreases, causing the sense amplifier memory, hence to be less robust and reliable. In addition, the paper also investigate the use of supply voltage to reduce the BTI degradation. The result show that increasing the power supply can reduce the sense amplifier BTI degradadtion with 33% for sensing voltage and with 18% for sensing delay; leading to clear tradeoff engineering question between power and robustness.**

***Index Terms*—BTI, NBTI, PBTI, SRAM sense amplifier**

I. Introduction

In recent decades, CMOS technology has witnessed relentless downscaling. Forces behind the trend are advancements in the fabrication technology, introduction of novel materials and evolution of architecture designs. However, for circuits based on the current CMOS technology, reliability failures have become a major bottleneck [1]–[3]. Bias Temperature Instability (BTI) (i.e., Negative BTI in PMOS transistors and Positive BTI in NMOS transistors) is a reliability failure mechanism which affects the strength of MOS transistors by increasing their threshold voltages and reducing their drain current (I_d) over the operational lifetime [5], [7], [8].

Static Random-Access Memories (SRAM) occupies a large part of semiconductor systems and plays a major role in the silicon area, performance, and critical robustness [9]. Much has been published on SRAM Test (e.g. [10]–[12]) than SRAM reliability (e.g. BTI) as reliability challenges emerged with technology scaling. Moreover, an SRAM system consists of cells array, and its peripherals circuits such as column and row address decoders, control circuits, write drivers, and sense amplifiers. Much have been published on the BTI SRAM cell array and few on the SRAM peripheral circuitry. For example, Binjie et al [17] investigated NBTI impact on Static Noise Margin (SNM) and Write Noise Margin (WNM) degradation of 6T SRAM cell. Kumar et al [18] Analyzed the impact of NBTI on the read stability and SNM of SRAM cells. Bansal et al [19] presented insights on the stability of an SRAM cell under the worst-case conditions and analyzed the effect of NBTI and PBTI, individually and in combination. On the other hand, few authors have focused on reliability analysis of the address decoders. For instance, Hamdioui et al. in [20] presented analysis of spot defects in SRAM address decoders and in [21] identified decoder delay faults due to inter and intra-gate resistive defects. Khan et al [22] investigated the impact of partial opens and BTI in SRAM address decoder. Furthermore, Menchaca et al [23] analyzed the BTI impact on different sense amplifier designs implemented on 32nm technology node by using failure probability (i.e., flipping a wrong value) as a reliability metric. However, the impact of BTI for different technology nodes and varying supply voltages are yet to be investigated on SRAM's sense amplifier. Furthermore, BTI impact on other sense amplifier metrics such as sensing delay and sensing voltage are still un-explored.

Although, it is obvious that BTI can cause timing delay and reduce memory reliability in most of the designs. This paper focuses on drain input latch-type sense amplifier design due to its low power superior performance [26]. In this paper, the parameters considered for analyzing BTI impact on sense amplifier include sensing delay and sensing voltage. In this regard, the main contributions of the paper are:

- Investigation of BTI impact on the sense amplifier's sensing delay and sensing voltage.
- Analysis of BTI impact on sense amplifier synthesis with different technology nodes i.e., 90nm, 65nm, and 45nm.
- Investigation of supply voltage impact to compensate for the BTI degradation on sense amplifier.

The result depicts that as technology scales down, BTI impact on sensing delay increases, while sensing voltage decreases with a significant margin. Furthermore, the icrease in supply voltage leads to reduction in sensing delay and increase in sensing voltage, thereby leading to robust sense amplifier.

The rest of the paper is organized as follows: Section II introduces SRAM systems, drain input latch-type sense amplifier, BTI mechanism and its model. Section III gives the simulation setup, analysis metrics, and the experiments performed. Section IV analyzes the result by using different technology nodes in sense amplifier, and varying supply voltages. Finally, Section V concludes the paper

II. Background

This section explains the functional model of an SRAM system. Afterwards, it explains the behavior of drain input latch-type sense amplifier. Finally, it presents BTI mechanism and its model analyzed in this paper.

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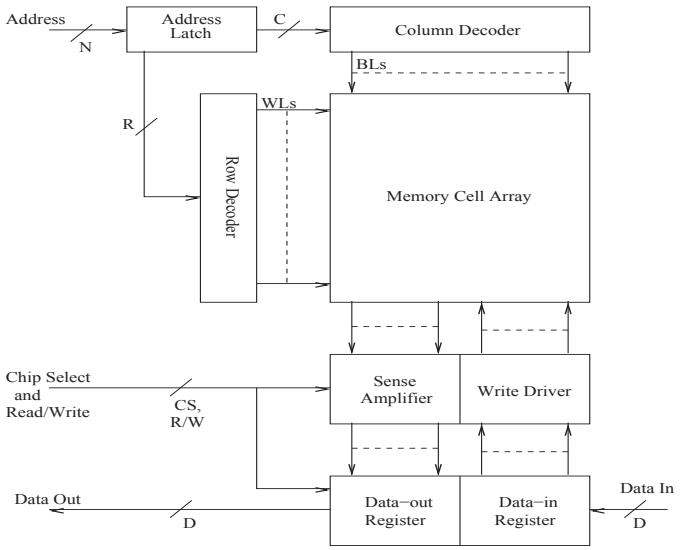

Fig. 1. Functional model of SRAM system

A. Memory model

A Memory system comprises memory cell array, row and column address decoders, read/write circuitry, input/output data registers and control logic as depicted in functional model of SRAM system in Fig. 1. [25]. However, the main focus of the paper is SRAM sense amplifier which is responsible for the amplification of small difference in the input signals.

SRAM Sense Amplifier

A sense amplifier (SA) in SRAMs takes a small voltage difference at the input (i.e., BL and BLBar) shown in Fig. 2., and produce amplified signals on the output (i.e., out and $\overline{out}$ towards memory output). There are different implementation of sense amplifier such as: strobed or non-strobed, voltage-mode or current-mode and traditional, compensated or calibrated sense amplifiers. Furthermore, there are several types of strobed voltage-mode sense amplifier such as: drain-input latch-type, gate-input stacked-latch type, look-ahead, self-closing, pulsed current source and double-tail latch-type strobed voltage-mode SAs. In this paper, drain-input latch-type SRAM sense amplifier will be focused. This design selection is based on the following advantages: (a) the design does not draw static current, (b) easily employ positive feedback to provide fast regeneration, (c) their design is straightforward, (d) the energy consumption in charging and discharging these large capacitances is reduced, and (e) the time the cell requires to develop its swing is also reduced.

The structure of the Drain input latch-type Sense Amplifier as depicted in Fig. 2. [26] consists pull-up transistors (i.e., Mup and MupBar), pull-down transistors (i.e., Mdown and Mdownbar), two access transistors (i.e., Mpass and MpassBar), two switching current source transistors (i.e., Mtop and Mbottom), and two inverters at the output of the Sense Amplifier with a load capacitance of 1fF each. The pull-up transistors and pull-down transistors are made of two PMOS (Mup and MupBar) and two NMOS (Mdown and MdownBar) transistors respectively, access transistors are two NMOS devices, switching current source transistors are one PMOS and one NMOS device at the top and bottom nodes of the Drain input latch-type Sense amplifier. These explained transistors/devices receive their inputs through BL and BLbar input signals.

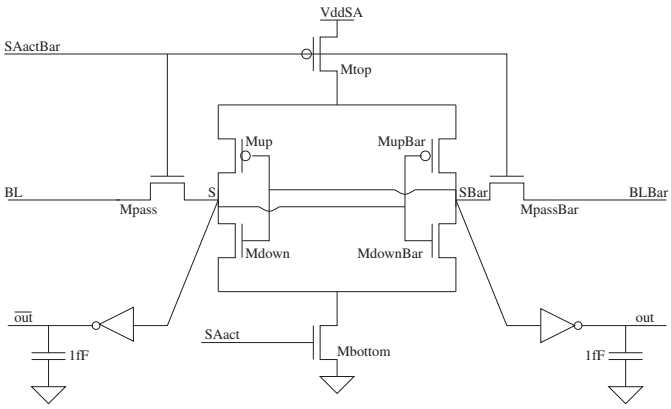

Fig. 2. Drain input latch-type Sense Amplifier

The operation of the sense amplifier circuitry is explained in three phases as follows: In the first phase, if SAact is low and SAactBar is high, the access transistors Mpass and MpassBar connect the BL(bar) inputs with the internal nodes S(Bar). However, when the BL input signal is pulled low, then there is a corresponding rise in the internal node SBar. However, in this phase Mtop and Mbottom transistors are in the off state. In the second phase, if SAact is high and SAactBar is low, then the pass transistors disconnect the inputs from the internal nodes. Then, node S connects MupBar and SBar connects Mup, this causes MupBar to be ON as Mtop pulls up the top node. This is the source for Mup and MupBar causing current to conduct. Furthermore, MupBar draws more current than the Mup which leads to SBar increasing faster than S, thereby leading to quick amplification of the input difference. Moreover, this is based on the PMOS transistors acting as differential amplifier with positive feedback phenomenon. Then, in the third phase, S node is actively pulled down when SBar exceeds the threshold of Mdown. All current paths are disabled when S is at 0V and SBar is at $V\mathrm{dd}_{\mathrm{SA}}$. Next, out goes quickly down when SBar threshold exceeds the output inverter, then $\overline{out}$ is the reverse. The process is repeated when SAact an SAactBar are restored to their original values.

B. Bias Temperature Instability

Bias Temperature Instability (BTI) mechanism takes place inside MOS transistors and causes a threshold shift that translates to additional delay, as described below.

BTI Mechanism

BTI causes threshold voltage ($\mathrm{V_{th}}$) increment to MOS transistors. The $\mathrm{V_{th}}$ increment in a PMOS transistor that occurs under *negative* gate stress is referred to as NBTI, and the one that occur in an NMOS transistor under *positive* gate stress is known as PBTI. For a MOS transistor, there are

two BTI phases, i.e., the stress phase and the relaxation phase.

In recent times, exhaustive efforts has been put to understand NBTI [5]–[7], [22]. Kaczer et al. in [6] have analyzed NBTI reasonably well but have not extended their analysis to deal with NBTI at a higher level. Alam et al. in [5] have modeled NBTI and presented the overall dynamics of NBTI as a reaction diffusion process. The model is usable at a higher level such as circuit level. Since in this work, BTI analysis is done at the circuit level, model of [5] will be used.

Stress Phase: In the stress phase, the Silicon Hydrogen bonds (≡Si-H) break at Silicon-Oxide interface. The broken Silicon bonds (≡Si-) remain at the interface (known as interface traps), and the released H atoms/molecules diffuse towards the poly gate. The number of interface traps (N_{IT}) generated after applying a stress of time (t) is given by [5]:

$$N_{IT}(t) = \left(\frac{N_o.k_f}{k_r}\right)^{2/3} . \left(\frac{k_H}{k_{H_2}}\right)^{1/3} .(6.D_{H_2}.t)^{1/6}, \quad (1)$$

where N_o, k_f, k_r, k_H, and k_{H_2}, represent initial ≡Si-H density, ≡Si-H breaking rate, ≡Si- recovery rate, H to H_2 conversion rate, and H_2 to H conversion rate inside the oxide layer, respectively. While D_{H_2} is the hydrogen diffusion constant.

Relaxation Phase: In the relaxation phase, there is no ≡Si-H breaking. However, the H atoms/molecules diffuse back towards the interface and anneal the ≡Si- bonds. The number of interface traps that *do not* anneal by the approaching H atoms during the relaxation phase is given by [18]:

$$N_{IT}(t_o + t_r) = \frac{N_{IT}(t_o)}{1 + \sqrt{\frac{\xi.t_r}{t_o+t_r}}} \quad (2)$$

where $N_{IT}(t_o)$ is the number of interface traps at the start of the relaxation, ξ is a relaxation coefficient with ξ=0.5 [18], t_o is the duration of the previous stress phase and t_r is the relaxation duration.

Threshold voltage increment: The N_{IT} oppose the gate stress resulting in the threshold voltage increment (ΔV_{th}). The relation between N_{IT} and ΔV_{th} is given by [4]:

$$\Delta V_{th} = (1 + m).q.N_{IT}/C_{ox}.\chi.\gamma, \quad (3)$$

where m, q, and C_{ox} are the holes/mobility degradation that contribute to the V_{th} increment [16], electron charge, and oxide capacitance, respectively. χ is a BTI coefficient with a value χ=1 for NBTI and χ=0.5 for PBTI [14]. Additionally, γ represents the stress duration with respect to the total input period (i.e., *activity factor*) of the transistor. The γ dependence of the ΔV_{th} shows that transistors in a gate/circuit that have different stress and relaxation phases will suffer from different degradations.

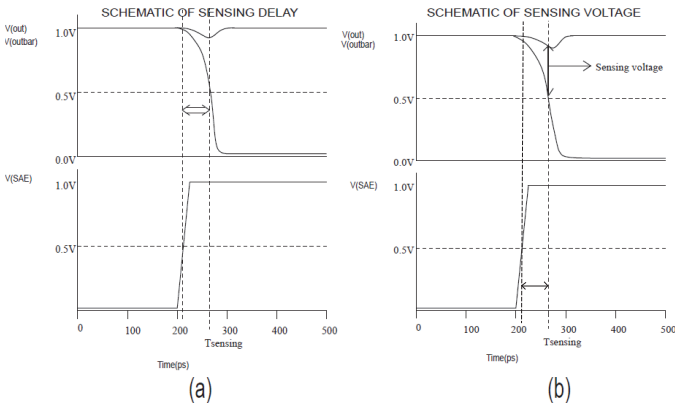

Fig. 3. Metric diagram of (a) Sensing delay and (b) Sensing voltage.

Delay increment: BTI induced ΔV_{th} of each individual MOS transistor has its contribution to the additional delay. A generalized formula that relates BTI induced ΔV_{th} in a transistor to dataline/output signal delay is given by [4], [15]:

$$\Delta D = \frac{n.\Delta V_{th}}{(V_{gs} - V_{th})} \quad (4)$$

where n is the velocity saturation index of majority carriers in MOS channels. Since NBTI causes ΔV_{th} to PMOS transistor and PBTI causes ΔV_{th} to NMOS transistor, the paper considers the threshold voltage shifts to both types of MOS transistors.

III. Analysis Framework

In this section describes the simulation setup, the metrics utilized in the experiments, and the experiments conducted in the paper.

A. Simulation Setup

A netlist of drain input latch type sense amplifier depicted in Fig. 2 has been synthesized using different technology nodes such as 90nm, 65nm, and 45nm PTM transistor models[1] and simulated using HSPICE. In the BTI analysis, the impact is added to each transistor with Verilog-A modules. Furthermore, each module generates voltage shift increment which is a function of the activity factor of the transistor.

B. Analysis Metrics

In this section, the metrics for analyzing BTI impact on sense amplifier are described. First, sensing delay, and then sensing volatge are introduced.

Sensing delay: Sensing delay metric is determined when the trigger signal (i.e., sense amplifier enable input signal) reaches 50% of the supply voltage and the target (i.e., either out or $\overline{out}$ falling output signal) reaches 50% of the supply voltage. The difference between the target and the trigger results in sensing delay as shown in Fig. 3(a). Furthermore, the relative variation of the sensing delay due to BTI is the difference between the measured sensing delay when BTI is added and referenced sensing delay when BTI is not added.

Sensing voltage: Sensing voltage metric refers to the difference between the output signals, for instance v(out) minus v($\overline{out}$) as shown in Fig. 3(b). at a fixed time (i.e., Tsensing). *T*sensing is initially determined as the time when the inverted trigger signal i.e., SAE reaches 50% of the supply voltage and one of the output signals (i.e., either out or $\overline{out}$) falling output signal reaches 50% of the supply voltage in the absence of BTI. Furthermore, the relative % sensing voltage is the difference between the measured sensing voltage and the referenced sensing voltage divided by referenced sensing voltage multiplied by 100.

C. Experiments Performed

In this paper, three sets of experiments are performed to analyze BTI impacts. Initially, it presents temporal degradation of sense amplifier parameters with time. Then, it analyzes variation of BTI impact in different technology nodes. Finally, it demonstrates variations of the impact with supply voltage. These experiments are described below:

1. BTI Impact experiments: BTI impact on sensing delay and sensing voltage of the SRAM sense amplifier is investigated.

2. Technology dependent experiments: BTI impact on the sensing delay and sensing voltage of the SRAM sense amplifier synthesized from different technology nodes is investigated.

3. Supply voltage dependent experiments: BTI impact on sensing delay and sensing voltage of the SRAM sense amplifier for a particular technology node as the supply voltage increases in ascending order (i.e., from 90% of Vdd to Vdd and 110% of Vdd) is investigated as well.

IV. EXPERIMENTAL RESULTS

In this section, we present the analysis results of the experiments mentioned in the previous section.

A. Temporal BTI Impact

Initially, BTI impact on output sensing delay signals is presented and thereafter, BTI impact on output sensing voltage signals is covered.

BTI Impact on sensing delay

BTI in MOS transistors of the above mentioned SRAM sense amplifier affect activation of the amplified output signals (i.e., output signal pulled down to zero) with respect to the differential input. Differential inputs are fixed, choosen in such a manner to obtain a required output signal amplification that meets the critical timing. The differential input depends on the technology node. For example, implementing the above sense amplifier circuitry in 90nm the differential input signals is 135mv, the supply voltage is 1v, and the critical timing for which the input signal fall low is 200ps. Analysis results to depict BTI impact on sense amplifiers sensing delay is given in Fig. 4. The Figure shows that sensing delay as a function of time (i.e., aging lifetime) increases as the sense amplifier output signals ages. For this case, sensing delay increases from 30.03ps to 36.19ps which is about 20.51% increase due to BTI impact.

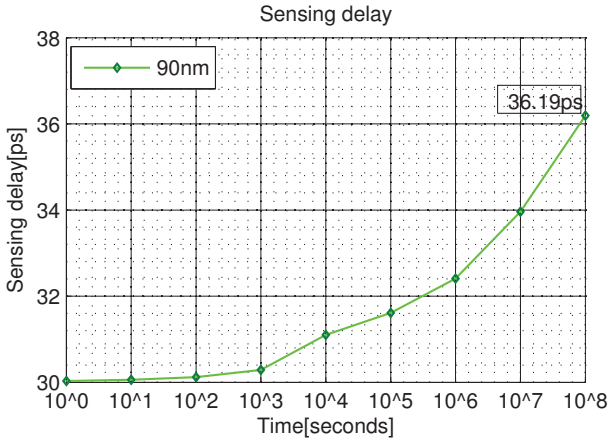

Fig. 4. BTI impact on Sensing delay for 90nm technology.

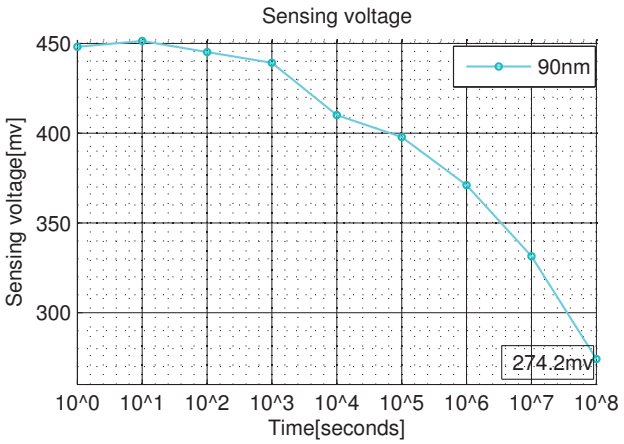

Fig. 5. BTI impact on Sensing voltage for 90nm technology.

BTI Impact on sensing voltage

In this subsection, we explore BTI impact on the sensing voltage metric considered in this paper. For this metric, the difference between two output signals (i.e., vout and v$\overline{out}$) at a given time is considered. The difference between the signals at the time of sensing changes with aging. For a given technology node (i.e., 90nm), Fig. 5 plots sensing voltage variation as a function of time (i.e., aging lifetime). This figure depicts that sensing voltage decreases with respect to increment in time. For this particular case, sensing voltage decreases from 448.1mv to 274.2mv with respect to the increase in time from 10^0 second to 10^8 seconds, and this is about -38.81% reduction in sensing voltage due to BTI impact.

B. Technology dependent BTI impact

Technology scaling down leads to oxide field increment, and this accelerates bond breaking phenomenon of BTI impact. In this section, experiments are performed for SA with different technology nodes at a nominal voltage (i.e., 0.833X of the standard supply voltage) to achieve the required impact [26]. For example, standard supply voltage of 45nm node is 1.0v and when multiplied by this factor it results to 0.833v. However, experiments are performed on different technology

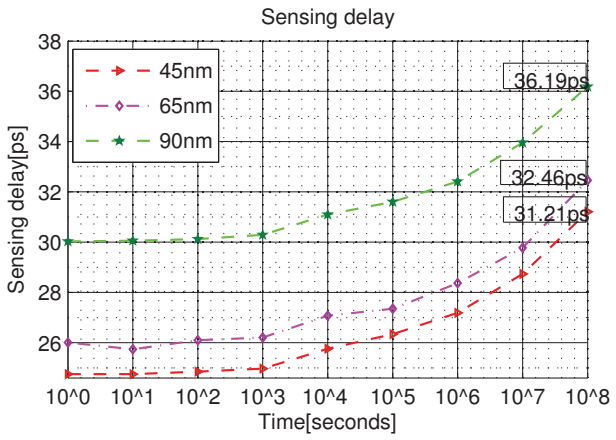

Fig. 6. Technology dependent Sensing delay.

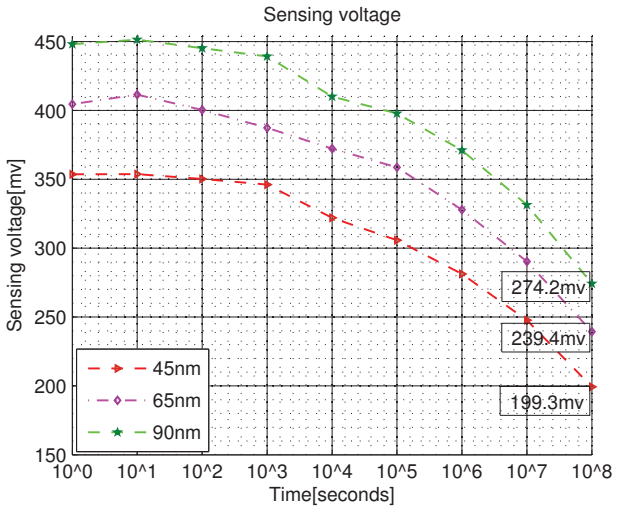

Fig. 7. Technology dependent Sensing voltage.

nodes as 45nm, 65nm, and 90nm. Experiments are performed to explore first, BTI induced sensing delay increment in different technologies. Thereafter, the sensing voltage technology dependence is investigated.

Sensing delay variation

Sensing delay (i.e., interval between SAE activation and falling output signal as shown in Fig. 3(a)) is strongly dependent on technology nodes. For instance, as shown in Fig. 6., in degradation free case, 90nm, 65nm, and 45nm based sense amplifier have the sensing delay of 30.03ps, 26.01ps, and 24.75ps, respectively. The figure also shows BTI induced degradation in sensing delay of sense amplifier based on different technology nodes i.e., 31.21ps, 32.46ps, and 36.19ps in 45nm, 65nm, and 90nm, respectively. There is significant variation in the increment. For instance, the variation is 20.51% in 90nm, and approaches 24.80%, and 26.10% in 65nm, and 45nm, respectively. An important point in the result is that although the impact on 45nm is higher with a small margin. This shows that the smaller the technology node, the higher the impact on sensing delay.

Sensing voltage variation

Sensing voltage (i.e., voltage difference between the bit lines at a particular instant of time as shown in Fig. 3(b)) varies significantly with technology scaling. Fig. 7. represent reduction in the sensing voltage with technology scaling. For instance, in degradation free case, the sensing voltage is 448.1mv for 90nm and approaches 404.6mv and 353.6mv in 65nm and 45nm technology base sense amplifier, respectively. The figure also shows BTI induced degradation in sensing voltage of SA based on different technology i.e., 199.3mv, 239.4mv, and 274.2mv in 45nm, 65nm, and 90nm, respectively. There is significant variation in the reduction. For instance, the variation is -38.81% in 90nm and approaches -40.83% and -43.67% in 65nm and 45nm, respectively. This also shows that the lower the technology node, the higher the impact on sensing voltage.

C. Supply voltage dependent BTI impact

This section presents result of supply voltage dependence experiments. First, supply voltage dependence of sensing delay is investigated. Afterwards, supply voltage dependence of sensing voltage is explored.

Sensing delay variation

Transistors experience significant supply voltage variation during operation. The variation affect oxide field and consequently BTI impact. To investigate the variation, the supply voltage is +/-10 of its nominal Vdd. Fig. 8. shows the investigation results. The figure shows that for the degradation free case, by lowering the supply voltage, sensing delay increases significantly. Additionally, impact of BTI is more significant at lower supply voltage. Fig. 8. represent increment in sensing delay with supply voltage reduction. For instance, in degradation free case, the sensing delay is 22.44ps for 0.9163v and approaches 24.75ps and 26.10ps for 0.8330v and 0.7497v supply voltage, respectively. The figure also shows

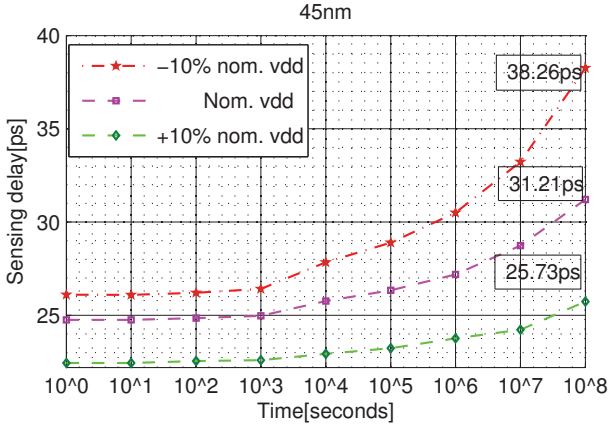

Fig. 8. 45nm supply voltage dependent sensing delay.

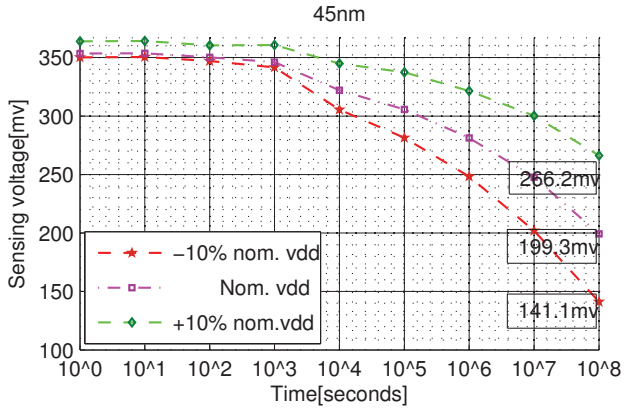

Fig. 9. 45nm supply voltage dependent sensing voltage.

BTI induced degradation in sensing delay of sense amplifer based on different supply voltages, i.e., 25.73ps, 31.21ps, and 38.26ps for 0.9163v, 0.8330v, and 0.7497v respectively. This shows % increment of 14.66% for 0.9163v and 26.10% and 46.59% for 0.8330v and 0.7497v respectively. This shows that higher supply voltage reduces the sensing delay with approx. 18% from the nominal voltage.

Sensing voltage variation

In this section, supply voltage dependence of sensing voltage is presented. Supply voltage varies significantly with sensing voltage. To investigate the variation, Fig. 9. shows the results. The figure shows that for the degradation free case by increasing the supply voltage, sensing voltage increases significantly. Besides, impact of BTI is more significant at higher supply voltage. Fig. 9. represent increment in sensing voltage with supply voltage increment. For instance, in degradation free case, sensing voltage is 350.2mv for 0.7497v and approaches 353.6mv and 363.9mv for 0.8330v and 0.9163v supply voltage, respectively. The figure also shows BTI induced degradation in sensing voltage of sense amplifer based on different supply voltages, i.e., 141.1mv for 0.7497v and approaches 199.3mv and 266.2mv for 0.8330v and 0.9163v, respectively. This shows % reduction of sensing voltage is -26.85% for 0.9163v and -43.64% and -59.71% for 0.833v and 0.7497v respectively. This implies that the higher supply voltage, BTI degradation with 33% for sensing voltage from the nominal supply voltage.

V. Conclusion

This paper investigates the impact of Bias Temperature Instability (BTI) on drain input latch-type memory sense amplifier of different technologies. First, BTI impact increases the sensing delay and reduces the sensing voltage causing the memory sense amplifier to be less reliable and robust. Second, increase in supply voltage per technology node compensate the sensing delay and sensing voltage causing the sense amplifier to be more robust and reliable. These results are validated with HSPICE.

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