# Is the Road Towards "Zero-Energy" Paved with NEMFET-based Power Management?

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***Abstract*—In this paper we explore the potential that the use of state-of-the-art Nano-Electro-Mechanical (NEM) devices, i.e., NEMFETs and NEM Relays, in the implementation of power management circuitry, in combination with efficient energy harvesters through 3D stacking integration, have in meeting the tight energy budgets of "Zero-Energy" autonomous sensor systems. We propose various 3D hybrid embodiments of an openMPS430 embedded processor augmented with NEMFET and/or NEM Relay based power management mechanisms and investigate their energy consumption when executing a heart beat detection application. Our investigations indicate that the hybrid NEMFET-oriented approach, which relies on sleep transistors and associated management logic implemented on a dedicated NEMFET die, is the most promising in terms of energy consumption and reliability. Moreover, when combined with a thermal energy harvester, potentially implementable on the same die, it can enable the road towards autonomous computing.**

## I. INTRODUCTION

Nowadays, CMOS technology is approaching its physical limits, i.e., the scalability frontier of the threshold voltage ($V_T$) forces a saturated supply voltage owing to the fact that the thermal voltage $k_B \cdot T/q$ does not scale, therefore the power density of integrated circuits increases abruptly [1].

As an alternative, emerging technologies have been proposed and investigated to supersede the basic CMOS device, e.g., Nano-Electro-Mechanical Systems (NEMS), carbon nano tubes, quantum-dot cellular automata, spintronics, ferromagnetic logic, and single-electron devices [1].

The goal of our work is to create an ultra low-power programmable processing platform for embedded smart nodes for pervasive computing (see Figure 1). In achieving long life, low energy embedded systems, we cannot realize an architecture based exclusively on eco-friendly (relatively speaking) emerging technologies due to the fact that at this time, only low complexity circuits were successfully designed with the above technologies. In fact, we claim that the road to achieving "green computing" is paved with hybrid solutions, in which CMOS and emerging devices cohabitate.

A first attempt towards our goal was presented in [2], however a more efficient solution is required. In this paper we continue our investigation on energy effective 3D stacked hybrid computation platforms and concentrate on the feasibility of autonomous smart sensor nodes implementations relying on such a hardware infrastructure.

In particular, we propose and evaluate the "zero-energy" potential of an improved version of the 3D-Stacked NEMS based power management architecture in [2], achieved via the following three embodiments: (i) an ultra low power processing core appropriate for wireless sensor nodes, (ii) NEMS based devices for the implementation of sleep transistors (STs) and the additional power management low frequency circuitry necessary for power gating, and (iii) energy harvesters to provide enough energy for the processing core in a low duty cycle application.

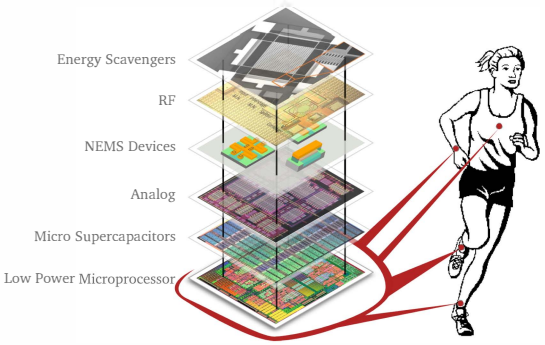


Figure 1 Emerging autonomous hybrid 3D stacked bio-sensor embodiment.

In this line of reasoning we propose a number of 3D embodiments of an openMSP430 [3] embedded processor equipped with different power gating mechanisms and evaluate the possibility to power it, when executing a heart beat monitoring application, only by energy harvesting means. We consider the following approaches, all powered at 1 V: (i) a NEMFET-oriented embodiment with both STs and always-on power gating cells implemented with NEMFETs, (ii) a NEM Relay power gating approach with STs implemented with NEM Relays and always-on power gating cells in CMOS technology, and (iii) a mixed NEMFET/NEM Relay solution with NEM Relay STs and NEMFETs always-on power gating cells. We make use of 3D stacking technology with Through-Silicon-Vias, which greatly reduces the drop-out voltage on the power supply lines between the CMOS logic circuit and the STs on the NEMS die. Moreover, it facilitates further integration for the entire sensor node, through stacking of dies containing analog sensing circuits, energy harvesters, capacitors, etc.

We implement the three proposed designs and compare them with the original 3D Stacked hybrid NEMFET/CMOS power management architecture from [2]. Our investigation suggests that the reduction in energy consumption for the three approaches are: 21.4%, 17.9%, and 23%, respectively. We note that the NEM Relays need an additional on-chip control volt-

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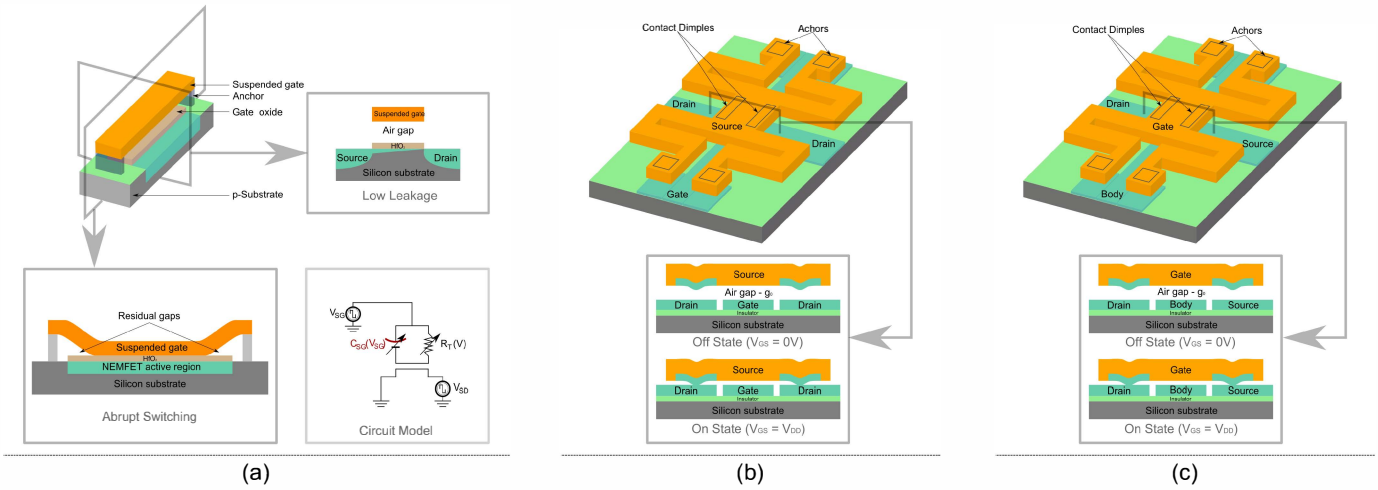


Figure 2 Schematic diagram of (a) NEMFET, (b) 3T NEM-Relay, and (c) 4T NEM-Relay.

age of at least 6 V for proper operation, and they degrade their ON resistance with switching cycles, drawbacks that could cancel out their energy savings advantages. Thus, the hybrid NEMFET-oriented approach is, for the time being, the best suited solution, and coupled with a thermal energy harvester of only $0.23\,\mathrm{cm}^2$ can enable the road towards autonomous computing.

The rest of the paper is organized as follows. First, in Section II, we give a overview of the state-of-the-art NEMS devices used in digital ICs. Section III describes the energy budget provided by up-to-date harvesters techniques. In Section IV we present and discuss experimental results and finally, Section V presents the conclusions.

## II. Nano-Electro-Mechanical Devices as Replacement for MOSFET

The switching energy efficiency of a device is given by the effective subthreshold swing ($S_{eff}$). With this consideration in mind, alternative transistor designs which offer perfectly abrupt off-to-on transition are attractive for energy-efficient electronics, since they provide high on/off current ratio with a smaller supply voltage, i.e., a small $S_{eff}$ value. Two such devices are: (i) the Nano-Electro-Mechanical FET (NEMFET) [4], which utilizes the pull-in and pull-out behavior of a mechanical beam (Suspended Gate) to achieve a perfectly abrupt switching transition, and (ii) the micrometer-scale mechanical switches that have been developed for radio frequency electronics (NEM Relay) [5], which function on the same principle as NEMFET with the difference that a mechanical beam is used as the Source of the device to enhance the on/off current ratio.

### A. Nano-Electro-Mechanical Field Effect Transistor

The Nano-Electro-Mechanical FET (NEMFET) is a rather complex device with a 3D geometry and cross-section as presented in Figure 2a.

Essentially speaking the device behaves like an electromechanical switch which responds to gate bias changes as follows. When the gate voltage $V_G$ is low the gate-oxide capacitance is in series with the air-gap capacitance resulting in low electrostatic coupling of the gate to the channel, thus in a negligible drain current $I_D$. If $V_G$ increases the situation remains unchanged until it reaches the pull-in voltage $V_{PI}$ in which case the electrostatic force cannot be compensated anymore by the mechanical restoring force and the suspended gate (beam) snaps onto the gate oxide, thus turning on the device. After the pull-in, the $I_D$ increase with $V_G$ is comparable with the one of a standard MOSFET. On the other way around when $V_G$ is decreased from some high value $I_D$ starts decreasing until at a certain $V_G$ value when the system becomes unstable due to combined electro-mechanical force and the beam is pulled-out. This causes an abrupt $I_D$ decrease due to a large decrease in capacitance, i.e., pull-out effect.

As indicated in [6] NEMFET devices can potentially replace High-$V_T$ sleep transistors (ST) due to their ultra low leakage characteristics. Note that for power gated designs two major features are desirable for the sleep transistors:(i)low sub-threshold leakage current to minimize the static power consumption, and (ii) low "ON" state resistance to minimize the voltage difference between the virtual and the real power supply nodes.

A comparison between the "ON" state resistance $R_{\mathrm{ON}}$ and "OFF" state leakage current $I_{\mathrm{OFF}}$ of an optimal NEMFET in terms of area and on-to-off ratio having $W_{Beam}$=250 nm, $L_{Beam}$=7.5 µm, air$_{gap}$=20 nm, $V_{PI}$=1.1 V and 65 nm High-$V_T$ CMOS based STs was presented in [2]. It suggests that the NEMFET ST $R_{ON}$ tends to become equal with the CMOS ST $R_{ON}$, while NEMFET ST $I_{OFF}$ (leakage) is about 2 orders of magnitude smaller than the one of the CMOS counterpart.

### B. NEM Relays

The scalability of the NEMFET due to the presence of air-gap and short channel effects is limited. In face of this limitation, micro-electro-mechanical relays, also termed "micro-relays" [7], appear to be an attractive alternative for zero-standby power logic applications. The attractiveness of micro-relays stems from the fact that a mechanical switch offers nearly ideal switching characteristics: zero off state drain-to-

TABLE I Various energy sources and harvested power densities [11].

| Source type | Source power | Harvested power |
|---|---|---|
| Indoor ambient light | 0.1 mW/cm$^2$ | 10 µW/cm$^2$ |
| Vibration/motion | 0.5 m @ 1 Hz 1 m/s$^2$ @ 50 Hz | 4 µW/cm$^2$ |
| Thermal | 20 mW/cm$^2$ | 30 µW/cm$^2$ |
| Radiofrequency | 0.3 µW/cm$^2$ | 0.1 µW/cm$^2$ |

source and gate leakage currents, and perfectly abrupt off-to-on switching transition. Since there is no trade-off between off-state leakage current and on-state drive current, the relay threshold voltage and therefore $V_{dd}$ can be in principle reduced much more aggressively than for a MOSFET in order to improve the energy efficiency.

The 3T NEM Relay described in [8] is a device with a rather similar 3D geometry when compared with the NEMFET. It essentially is an electrostatic switch having three terminals, as illustrated in Figure 2b. In the off state, when the source and the drain electrodes are separated by an air gap, the behavior is similar with an open relay, thus no current can flow between the electrodes. When the amplitude of the gate-to-source voltage $V_{GS}$ is sufficiently large, above $V_{PI}$, the source electrode is actuated downward into contact with the drain electrode so that current can flow under the influence of the drain-to-source voltage $V_{DS}$. Various 3T switch designs have been reported in the literature [8], [9]. However, their performance is limited by the high operating voltage larger than 5 V), and a slow actuation of about 100 ns [5].

A 4T relay, depicted in Figure 2c, has been also proposed. To cope with high operation voltage and actuation time, the 4T relay design, a normally off device, adds a body terminal. With the beam acting now as the gate, the voltage between the gate and the body $V_{GB}$ determines the state of the relay. When the amplitude of the $V_{GB}$ is higher than $V_{PI}$, the relay will be turned on. Thus, a fixed voltage, and independent from the source and drain voltages is required for the body terminal to limit the variation of the gate switching voltage. Low switching voltages are desirable for low active power consumption. $V_{PI}$ can be reduced by applying more advanced manufacturing techniques, i.e., increasing the actuation area (W×L), decreasing the thicknesses of the movable structure, or decreasing the height of the fabricated actuation gap $g_0$. However, all of these negatively affect the device density. Another post-process solution is to tune the gate switching voltages via body biasing, but extra circuitry and power consumption are required in order to generate on-chip large $V_B$ values, approximately 8 V as presented in [10], for a device suited for 10 MHz circuitry. Moreover, the ON state resistance of the 4T Relays is increasing from kΩ to tens of kΩ after only $10^4$ actuations, practically limiting the digital implementation range only to low activity circuits.

## III. Power Budgeting of Energy Harvesters

To address the problem of finite node lifetime of battery-powered smart systems energy harvesting is employed. Different forms of energy from the ambient environment or from other sources are converted to electrical energy which powers the node. If the harvested energy is large enough and continuously available, a smart node can even be powered forever (or at least until a failure in the power supply circuitry appears). Furthermore, by monitoring the amplitude and periodicity of the harvested energy, the smart sensor can self-allocate its available energy and alter at run-time the functioning duty-cycle to match the supply energy.

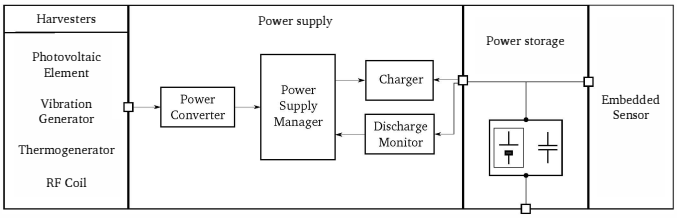


Figure 3 System-level power supply architecture.

The architecture of the power supply of the sensor node is depicted in Figure 3. The harvester transforms the ambient energy (e.g., photonic, kinetic, thermal, RF energy) in a variable voltage. A power converter performs voltage rectification and smoothens/regulates the voltage to the desired value. The power supply manager controls the operation of the converter and the optional charging circuits, when a storage element (battery, super-/ultra-capacitor) is needed.

Since our end goal is to achieve a fully autonomous smart sensor node we need to know the power budgets that harvesters can produce. Note that the form in which the energy is harvested, the energy source characteristics, and the conversion efficiency dictate the power budget. Table I summarizes the typical produced and expected harvested power densities for the most used energy sources in a human ambient environment.

Harvesting photovoltaic energy offers zero or close to zero output during nighttime, and a battery is required for continuous operation. A temperature gradient can be converted in electrical energy via micro-machined thermopiles integrated in the same package with the sensor node. The human skin is a favorite energy source since it provides a significant temperature difference from the surrounding environment. However, it requires a more complex package, with one surface being a plate with the exterior side in thermal contact with the human skin, and the interior side in direct electrical contact with one end of the thermopiles. Due to their ease of integration within the same package, micro-machined piezoelectric resonant vibration devices are the most promising in harvesting motion energy for smart sensor nodes. Finally, radiofrequency (RF) energy, though covering large surfaces of the inhabited land nowadays offers the less power compared with all other sources.

## IV. Evaluation Results and Discussions

The base 3D stacked power management architecture described in [2] consists of two dies connected with Through-Silicon Vias. The bottom CMOS tier comprises the active digital logic circuit, and can be power gated through the NEMFET STs incorporated on the top tier.

TABLE II Energy budgeting.

| Implementation | Energy [µJ] | Required Harvester Area [cm$^2$] Light | Vibration | Thermal | RF |
|---|---|---|---|---|---|
| *NEMFET-based STs* | | | | | |
| Hybrid [2], $V_{DD} = 1.2\,\text{V}$ | 8.611 | 0.86 | 2.15 | 0.29 | 86.11 |
| Enhanced Hybrid | 6.761 | 0.67 | 1.69 | 0.23 | 67.61 |
| *NEM Relay-based STs* | | | | | |
| Always-on cells w/ CMOS | 7.073 | 0.71 | 1.77 | 0.24 | 70.73 |
| Always-on cells w/ NEMFET | 6.579 | 0.66 | 1.64 | 0.22 | 65.79 |

We first consider an Enhanced architecture which improves the energy efficiency of the platform by two means: (i) relocation of the openMSP power management controller (PMC) and power gating overhead circuitry, i.e., isolation and state-retention cells, on the NEMS die, and (ii) reduction the supply voltage from 1.2 V to 1.0 V. The first approach entails redesigning the referred blocks in the ultra low leakage NEMS technology, hence alleviating part of the leakage overhead associated with the use of CMOS devices. Thus, the bottom CMOS tier comprises the active logic circuit, while the top tier incorporates the always-on cells and the PMC implemented in NEMS technology. Moreover we consider two additional platforms both having STs implemented with NEM Relays and always-on power gating cells implemented in CMOS and NEMFET technology, respectively.

For evaluation we use the same test vehicle used to validate the base architecture, i.e., the *Hybrid* design, a typical SoC for low power embedded devices running a heart rate monitor application [2]. To asses the impact of using NEM Relays as sleep transistors, we use the same methodology previously applied for NEMFET-based power gating.

The energy consumption values obtained after simulation in worst-case technology corner, with respect to power consumption, for both the Enhanced NEMFET- and NEM Relays-based power management architectures, as well as the original reference *Hybrid* are presented in Table II. One can observe that due to the supply voltage reduction and the placement of the low-activity power management logic on the NEMS die, the *Enhanced Hybrid* NEMFET-based implementation provides an energy consumption reduction of 21.4%.

For the NEM relay based implementations we have to make use of MOSFETs or NEMFETs for the implementation of the PMC block. This is motivated by the fact that, even for the considered biomedical application, which has a rather low switching activity of 200 cycles per second, the NEM Relays' $R_{ON}$ is increasing with one order of magnitude within tens of seconds of circuit life time. This makes NEM Relays not suited to implement the logic gates from the always-on cells and the PMC block.

Even though at circuit level the NEM relay based approach does not provide a significant energy improvement over the NEMFET counterpart, this can be mostly explained by the fact that the considered application has a rather high duty cycle, and the ON power term is dominant in the total energy equation. Seen from device level, the advantages of the NEM Relays are obvious when compared with NEMFETs, as they offer almost ideal switching characteristics, "zero" off state leakage current, "infinite" on current, and abrupt off-to-on and on-to-off switching transitions. However for the time being their integration in a hybrid CMOS/NEMS architecture for low power embedded smart sensor nodes requires the on-chip generation of high voltages of approximately 6 V. Hence such an approach adds extra circuitry overhead which will most likely cancel out its advantages over the NEMFET solution. Moreover NEM Relay are less reliable and substantially increase their $R_{ON}$ after tens of thousands switching cycles. This result in an IR drop increase that may make the entire circuit to malfunction.

Based on the total energy requirements we also compute in Table II the area that an energy harvester needs to have to be able to autonomously power our platform. One can observe in Table II that the NEMS based schemes we proposed can be potentially powered from harvesting sources thus opening the road towards the implementation of zero-energy autonomous computing nodes. Light and thermal energy sources seem to be the most promising candidates to supply miniature autonomous smart sensors. While vibration generators do not offer the same power density, they do not need to be in visible or thermal contact with the environment so they are more easily to be integrated in future smart micro-sensors with a stacked layout.

## V. CONCLUSIONS

In this paper we explored the possibilities to achieve autonomous, self-powered embedded smart sensors, by an in-depth investigation of the use of NEMS devices as power gating circuitry, followed by an energy budgeting of autonomous smart sensor nodes powered by various types of energy harvesters. Our investigations suggests that due to obvious advantages of the NEMS switches at device level, efficient energy harvesters design and 3D stacked integration technology we are entitled to answer affirmatively to our research question.

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