An Overview of Power Reduction Techniques for Single and Multicore Systems

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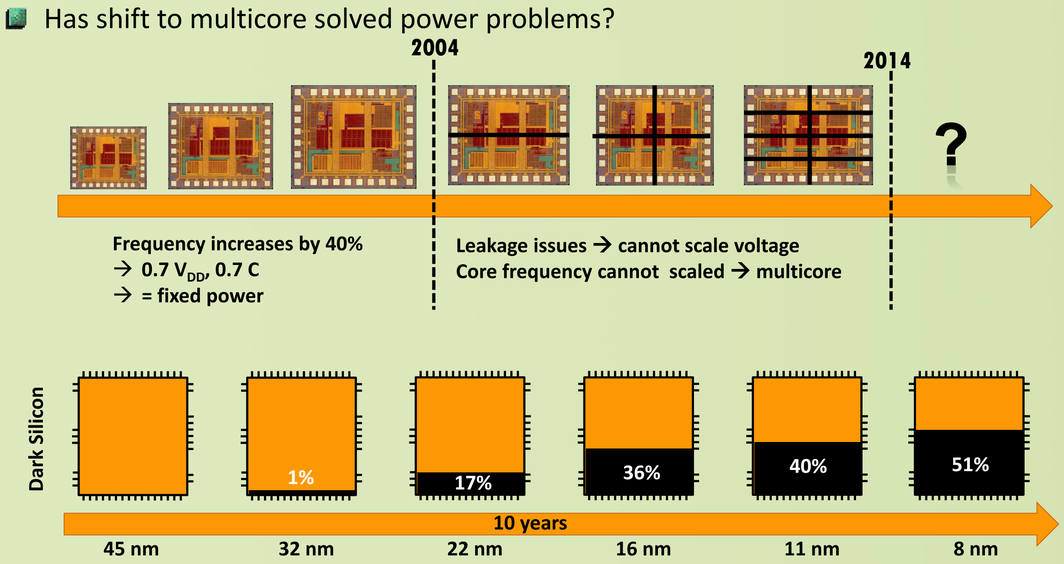
Introduction/Motivation

- Has shift to multicore solved power problems?



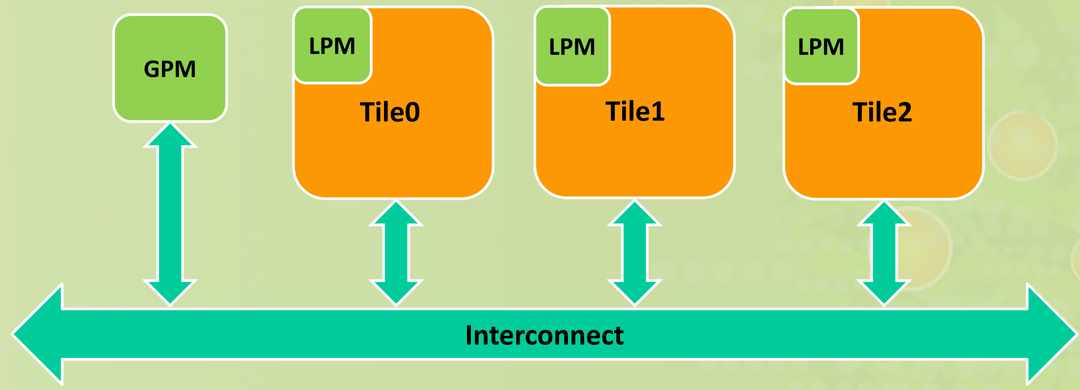
Sources of power consumption:
- **Static power** (idle power or leakage) is dissipated irrespective of system's idle or active state
- **Dynamic power** is consumed during circuit activity when charges in inputs occur

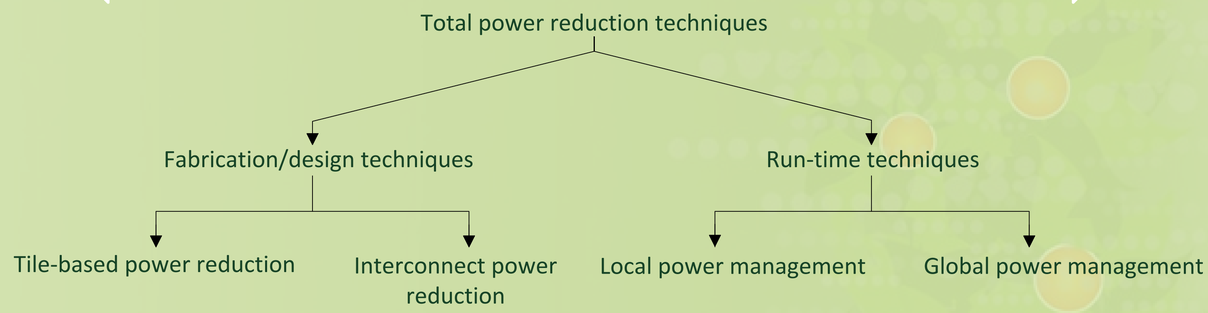
- Based on ITRS, subthreshold leakage power exceeds dynamic power from 65-nm feature size

Power reduction techniques:
- Leakage power reduction techniques
- Total power reduction techniques, including both dynamic and leakage power

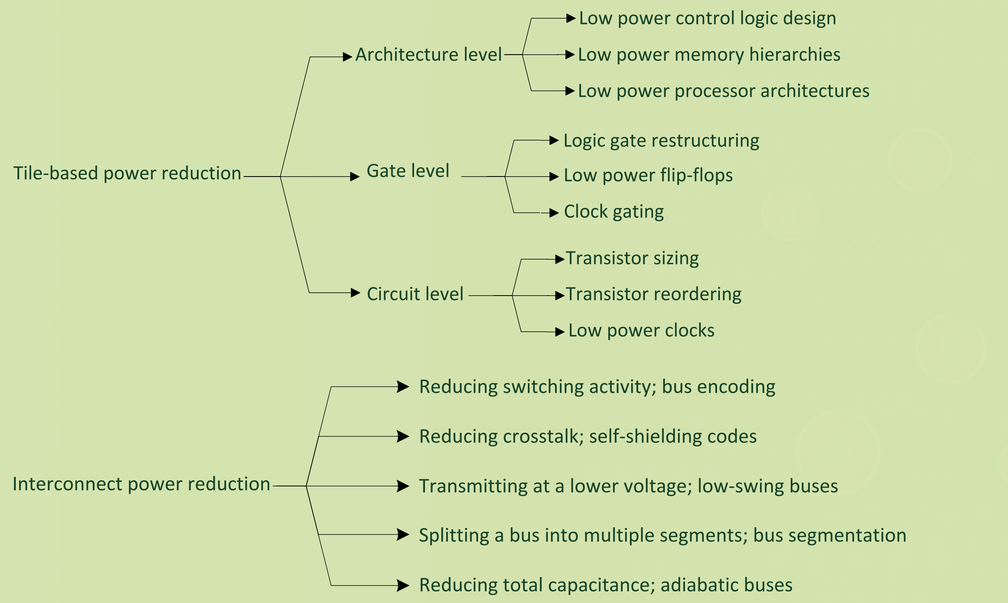
Total Power Reduction Techniques

System model block diagram



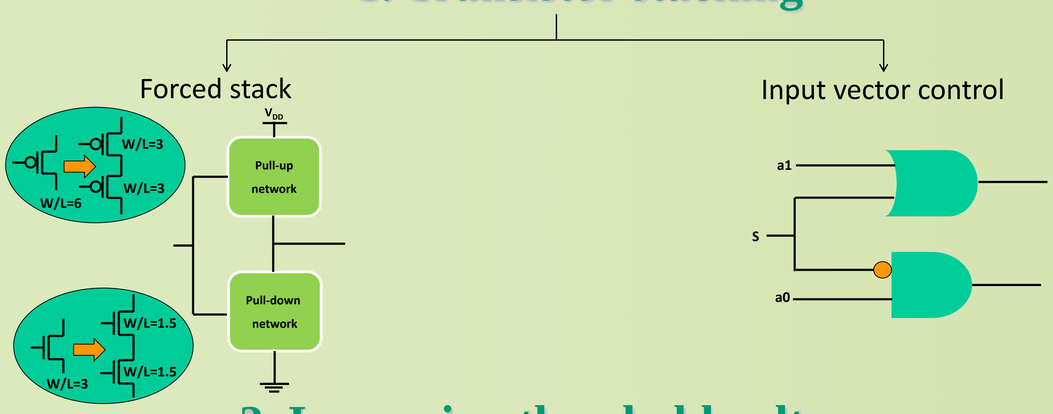


Fabrication/design Techniques

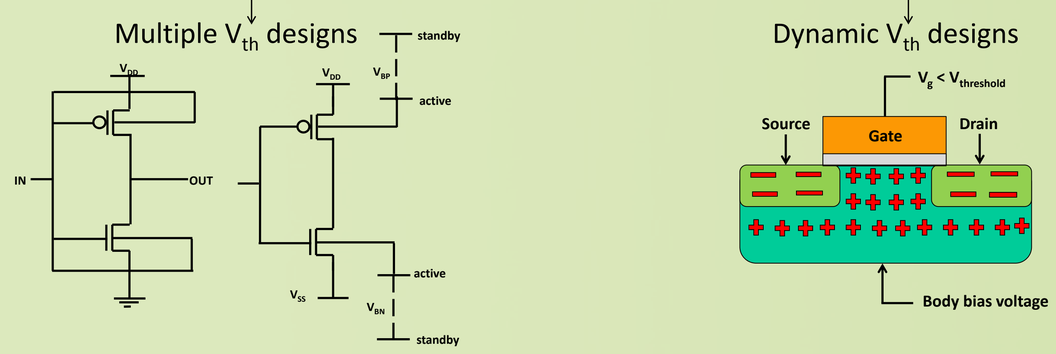


Leakage Power Reduction Techniques

1. Transistor stacking



2. Increasing threshold voltage

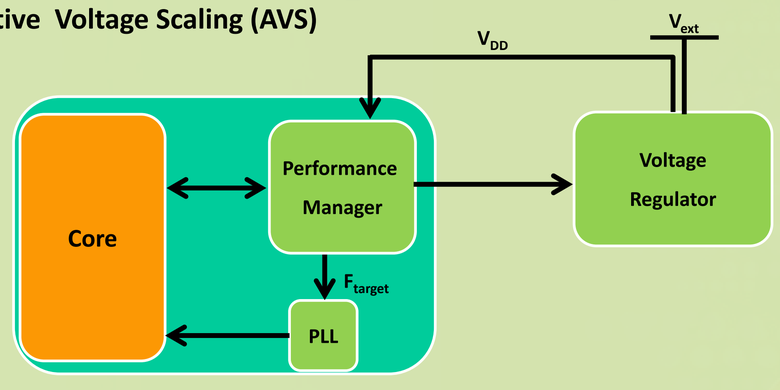


3. Supply voltage gating

Run-time Techniques

Local power management

Adaptive Voltage Scaling (AVS)



Joint Adaptive Voltage Scaling and Body Biasing

- Using dynamic voltage scaling together with adaptive body biasing
- Much more effective than using any of them individually

Global power management

AVS techniques can also be utilized for multi-core processors at different levels of granularity:
1) Per-chip, the supply voltage is set globally for the whole chip
2) Per-core, the supply voltage is set for each core, which means that only cores that require higher frequency are set to the higher supply voltage, while other cores operate at lower supply voltage or are completely shut down

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