Impact of BTI on SRAM Sense Amplifier in the Presence of Temperature and Process Variation

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***Abstract*—Bias Temperature Instability (BTI) has become a major reliability failure mechanism in the nano-scale era. This paper presents BTI impact of the standard SRAM latch-type sense amplifier for different temperatures and process variations for 45nm technology node. The results show that the BTI impact on sensing delay increases as the temperature scales up (i.e., from 298K to 398K), hence affecting its robustness and reliability. In addition, result show that process variations may further degrade the sense amplifier sensing delay, but with minor impact as compared to the temperature impact.**

***Index Terms*—BTI, NBTI, PBTI, SRAM sense amplifier**

I. Introduction

In recent decades, CMOS technology has witnessed aggressive downscaling that led to increase process variation and reduced the reliability of MOS transistors [1]. Among major failure mechanisms, Bias Temperature Instability increases transistor V_{th} due to generation of charges at the silicon-oxide interface and/or inside the oxide layer. The BTI induced V_{th} shift is temperature and workload dependent.

SRAM occupies a large part of semiconductor systems and significantly affect the area, performance, and critical robustness. The SRAM consist of a cell array, and peripheral circuits such as column and row address decoders, control circuits, write drivers, and sense amplifiers (SA). Several works focused on the BTI SRAM cell array and only few considered the SRAM peripheral circuitry. The impact of BTI for different temperatures and process variations are yet to be explored on the sense amplifier.

This paper investigates the impact of BTI on the sense amplifier's sensing delay. Thereafter, it presents the combined impact of temperature and process variation on SRAM sense amplifier.

II. BTI, Temperature and Process variation Impact

In this section, we explore the impact of BTI on the sensing delay after 10^8s by modeling Negative-BTI and Positive-BTI in the PMOS and NMOS transistors of the sense amplifier, respectively. Thereafter, we analyze the combined impact of temperature (from 298K to 398K) and process variation by performing monte-carlo simulations with a normal distribution for the V_{th} of the transistors [2]. We assume a worstcase workload in which the SA is assumed to operate 75% of the time, i.e., 75% of all instructions are assumed to be read operations. The analysis results of these cases are presented next.

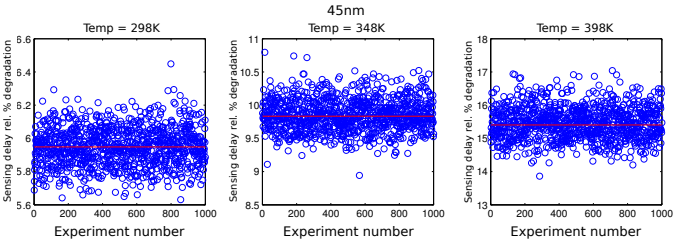

Fig. 1. BTI impact on Sensing delay under temperature and process variations

Temperature impact on sensing delay: Figure 1 depicts the sensing delay of the SA for 1000 monte-carlo simulations at three different temperatures (i.e., T1= 298K, T2= 348K, and T3= 398K). The red line indicates the BTI impact for the normal PMOS/NMOS V_{th} values. The relative BTI induced sensing delay degradation is about 5.95%, 9.83%, and 15.40% for temperatures, T1, T2, and T3, respectively, which may significantly affect the reliability of the device.

Process variation impact: Figure 1 also depicts the impact of process variations of V_{th} parameter on sensing delay of the sense amplifier; each blue circle present a single monte-carlo simulation. The figure shows that the process variations have larger impact on higher temperatures; the standard deviation of the simulations are 0.12%, 0.24%, and 0.49% for T1, T2, and T3, respectively. Therefore, for future designs, SA designers need to consider proper safe-margins for long-term operations.

III. Conclusion

This paper investigated the impact of BTI on standard memory latch-type sense amplifier for varying temperatures and process variations. BTI impact under temperature and process variation increases the sensing delay leading to less reliable and robust sense amplifiers.

References

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