BTI Analysis for High Performance and Low power SRAM Sense Amplifier Designs

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***Abstract*—Bias Temperature Instability (BTI) has led to more vulnerable ICs with the continuous downscaling of CMOS technologies. This paper presents the impact of BTI for two different SRAM sense amplifiers which target two applications, i.e., low power (LP), and high performance (HP). The evaluation metrics, the sensing delay (SD) and energy, are analyzed for three workloads. In contrast to earlier work, this paper thoroughly quantifies the increased impact of BTI in such sense amplifiers for the different applications for 45nm technology node. The results show that the sensing delay degrades faster for high performance application. We observed an increase in energy consumption for the HP application when BTI is applied, while this consumption reduces for the LP application. The results further show that the BTI impact sensing delay is 4.00% for LP, and 5.02% for HP when typical workload is applied for a 10^8s lifetime, while there is no significant change in energy consumption for both LP and HP applications. Furthermore, the results show that, the BTI sensing delay impact is higher for Standard-latch type Sense Amplifier (SLT-SA) than for Double-tail ltach-type Sense Amplifier (DTLT-SA) for the worst case workload. BTI impact on energy is lower for DTLT-SA as compared to SLT-SA.**

***Index Terms*—BTI, NBTI, PBTI, SRAM sense amplifier**

I. INTRODUCTION

In recent decades, CMOS technology has been sustained with aggressive downscaling that severely impacts the reliability of devices [1–3]. These trends are a consequence of advancements in the fabrication technology, introduction of novel materials and evolution of architecture designs. Bias Temperature Instability (BTI) (i.e., Negative BTI in PMOS transistors and Positive BTI in NMOS transistors) is a reliability failure mechanism which affects the performance of MOS transistors by increasing their threshold voltage and reducing their drain current (I_d) over the operational lifetime [4,5]. However, studies of such individual devices or small composites do not allow extrapolation of these effects on larger circuits like SRAMs.

Static Random-Access Memories (SRAM) occupy a large fraction of semiconductor chip and play a major role in the silicon area, performance, and critical robustness [6]. An SRAM system consists of an array of cells, its peripherals circuits such as row and column address decoders, control circuits, write drivers, and sense amplifiers.

Many publications analyzed the BTI impact on SRAM cell array, while very limited work is published on the SRAM peripheral circuitry. For instance, Binjie *et al.* [7] investigated NBTI impact on Static Noise Margin (SNM) and Write Noise Margin (WNM) degradation of 6T SRAM cell. Kumar *et al.* [8] Analyzed the impact of NBTI on the read stability and SNM of SRAM cells. On the other hand, few authors have focused on reliability analysis of the SRAM peripheral circuit. Khan *et al* [9] anlyzed the impact of partial resistive defects and bias temperature instability on SRAM decoder reliability. Menchaca *et al.* [10] analyzed the BTI impact on different sense amplifier designs implemented on 32nm technology node by using failure probability (i.e., flipping a wrong value) as a reliability metric. Agbo *et al.* [11] investigated the BTI impact on SRAM drain-input latch type sense amplifier design implemented on 90nm, 65nm, and 45nm for different supply voltages by using sensing delay and sensing voltage as reliability metrics. However, quantitative analysis of BTI impact of peripheral circuits (including sense amplifiers) while considering different workloads and designs is still to be explored. It is worth noting that understanding and quantifying the aging rate of each memory part is needed for optimal reliable memory design; this is because the different parts may degrade with different rates depending e.g. on the workload (application).

This paper focuses on two different SRAM sense amplifiers each targeted for a different application. The standard latch-type sense amplifier design is selected for its superior performance [12] for HP, and double tail latch type SA due to its low power properties [12] for LP. The BTI impact for each design is analyzed using different workloads. The main contributions of the paper are as follows:

- Investigation of BTI impact on the sense amplifier's sensing delay and energy; two different target applications are considered.
- Thorough quantitative analysis of the BTI impact using different workloads.
- Comparison between two different sense amplifiers designs.

The rest of the paper is organized as follows: Section II introduces the architectures of the sense amplifiers, i.e.; standard latch type and double-tail latch type sense amplifier, and bias temperature instability model. Section III provides our analysis framework, it presents also the performed experiments. Section IV analyzes the result for different workloads, and

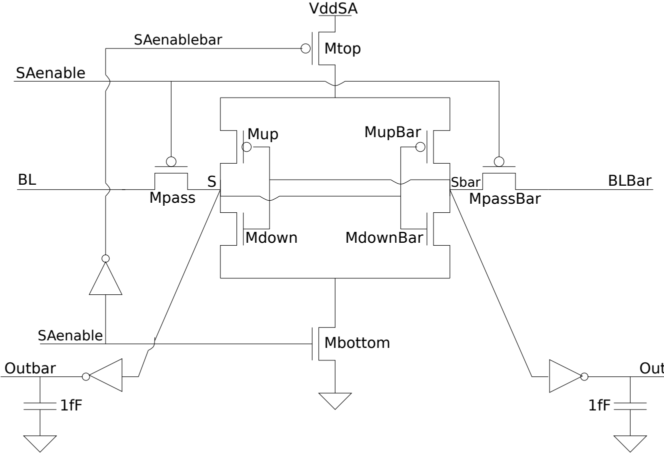

Fig. 1. Standard latch-type sense amplifier.

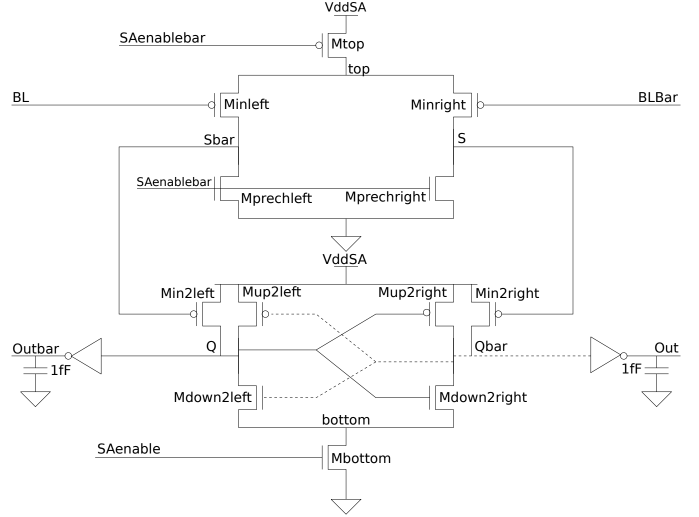

Fig. 2. The double tail latch type sense amplifier

SA designs. Finally, Section V concludes the paper.

II. Background

This section presents the working principles of the targeted sense amplifiers. Thereafter, it explains the bias temperature instability model analyzed in this paper.

A. Sense Amplifiers

Several implementations of sense amplifiers have been proposed. In this section, first the standard latch-type SRAM strobed sense amplifier will be addressed which is representative for HP industrial SA designs [12]. Thereafter, the LP double-tail latch type sense amplifier is described [12].

Standard Latch-Type Sense Amplifier (SLT SA)

The structure of the Standard latch-type Sense Amplifier is depicted in Fig. 1. The operation of the sense amplifier consists of two phases. In the first phase, when SAenable is low, the access transistors Mpass and MpassBar connect to the BL (BLBar) with the internal nodes S (Sbar). In this phase, Mtop and Mbottom transistors are switched off. In the second phase, when SAenable is high, the pass transistors disconnect the BL (BLBar) input from the internal nodes. The cross coupled inverters get their current from Mtop and Mbottom and subsequently amplify the difference between S and Sbar and produce digital outputs on Out and Outbar. S (Sbar) node is actively pulled down when Sbar (S) exceeds the threshold voltage of Mdown. The positive feedback loop ensures low amplification time and produces the read value at its output. Moreover, all current paths are disabled when S (Sbar) is at 0V and S (Sbar) is at $V_{dd\mathrm{SA}}$ or vice versa. This process is repeated for each read operation.

Double-tail latch-type Sense Amplifier (DTLT SA)

Fig. 2 introduces the double-tail latch-type SA. It uses two tails, one for capturing the input and the other for amplification and latching. Initially, when SAenable = 0V, Mtop and Mbottom are disabled. Nevertheless, S and Sbar are pulled to ground by Mprechleft and Mprechright, respectively. Subsequently, Q and Qbar are pulled up. Thereafter, when SAenable = 1V, the capturing tail will charge up nodes S and Sbar; their charge time depends on the inputs BL and BLBar. The ΔS creates a voltage difference at Q and Qbar through transistors Min2left and Min2right. Finally, the amplification and latching tail will amplify this voltage difference.

B. Atomistic Model

Kaczer *et al*. proposed the atomistic model in [13,14]. It is based on the capture and emission of single traps during stress and relaxation phases of NBTI/PBTI, respectively. The threshold voltage shift of the device ΔV_{th} is the accumulated result of all the capture and emission of carriers in gate oxide defect traps. The probabilities of the defect occupancy in case of capture P_C and emission P_E are defined by [15]

$$P_C(t_{STRESS}) = \frac{\tau_e}{\tau_c+\tau_e}\left\{1 - exp\left[-(\frac{1}{\tau_e}+\frac{1}{\tau_c})t_{STRESS}\right]\right\} \quad (1)$$

$$P_E(t_{RELAX}) = \frac{\tau_c}{\tau_c+\tau_e}\left\{1 - exp\left[-(\frac{1}{\tau_e}+\frac{1}{\tau_c})t_{RELAX}\right]\right\} \quad (2)$$

where τ_c and τ_e are the mean capture and emission time constants, and t_{STRESS} and t_{RELAX} are the stress and relaxation periods, respectively. For more insight between the relation of Eq. (1), Eq. (2), and V_{th} see [16].

III. Analysis Framework

A. Framework Flow

Fig. 3 depicts our generic framework to evaluate the BTI impact on the two considered sense amplifier circuits. Next, its inputs, processing and output blocks are described.

Input: The general input blocks of the framework are the technology library, Sense Amplifier design, and BTI input parameters. They are explained as follows. In this section, the analysis framework and the conducted experiments are presented.

- Technology library: In this work we only use the 45nm PTM library [17]. For the LP SA we use the LP library,

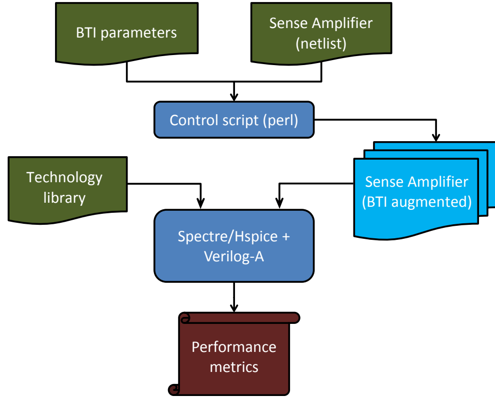

Fig. 3. Analysis framework.

while for HP SA the HP library. Note that in general any library card can be used.

- SA design: Generally, all sense amplifier design can be used. In this paper we focus only on the standard latch-type SA and double-tail latch-type SA. The SA designs are described by a SPICE netlist.
- BTI parameters: The BTI induced degradation depends strongly on the stress time duration. The stress time defines how long the workload sequence is being applied. The workload sequence is assumed to be repeated until the age time is reached. To perform realistic workload analysis, we assume that today's applications consist of 10% - 90% memory instructions and the percentage of read instructions is typically 50% - 90%. We derive from these assumptions the following cases: *best-case* with stress period of 0.1 * 0.1 = 0.01, *worst-case* with 0.9 * 0.9 = 0.81, and *mid-case* with 0.5 * 0.5 = 0.25. They lead to the following workload sequences: best-case: $R0R1I^{198}$, worst-case: $R0^4I^1$ and mid-case: $R0I^{24}$. In these sequences, $R0$ stands for read 0, $R1$ stands for read 1, I for idle operation (which includes memory write operations).

Processing: Based on the transistor dimensions and the other specified inputs, the Control script (perl) generates several instances of BTI augmented SRAM sense amplifier circuits. Every generated instance has a distinct number of traps (with their unique timing constants) in each transistor, and are incorporated in a Verilog-A module of the SA netlist. The module responds to the every individual trap, and alters the transistors concerned parameters such as V_{th}. After inserting BTI in every transistor of the SA design, a Monte Carlo (MC) is performed at different time steps (100 runs at each time step) where circuit simulator (HSPICE/Spectre) is used to investigate the BTI impact.

B. Output Metrics

In this section, the sensing delay metric used for analyzing BTI impact on sense amplifier is described.

Sensing delay: The sensing delay metric is determined when the trigger signal (i.e., sense amplifier enable input signal) reaches 50% of the supply voltage and the target (i.e., either Out or Outbar falling output signal) reaches 50% of the supply voltage. The difference between the target and the trigger results in sensing delay as shown in Fig. 4.

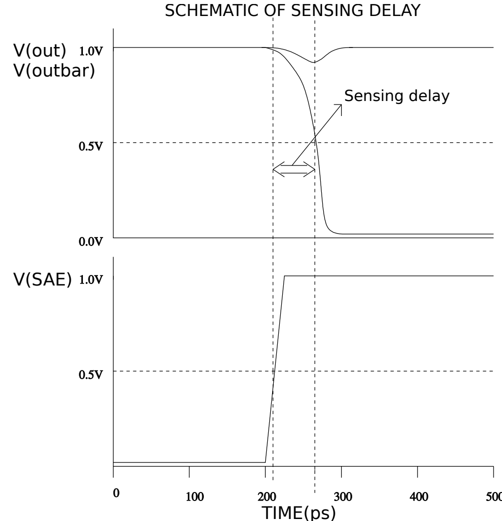

Fig. 4. Metric diagram of Sensing delay.

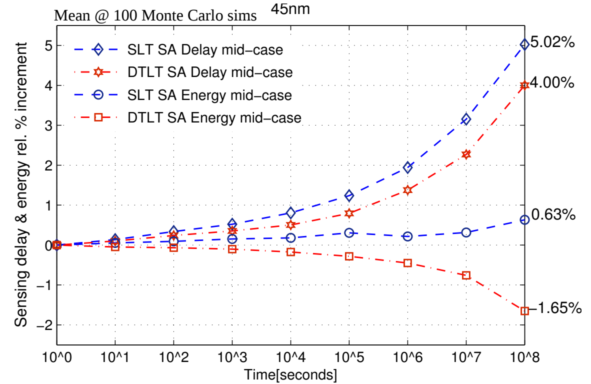

Fig. 5. BTI impact on sensing delay and energy.

Energy: The energy metric is defined as the energy consumption for a single read operation.

C. Experiments Performed

In this paper, two sets of experiments are performed to analyze BTI impacts. These experiments are described below:

1 **Temporal Impact Experiments:** BTI impact on sensing delay and energy of the two SA designs is investigated.
2 **Workload and Design Dependent Experiments:** BTI impact on the sensing delay and energy of the SRAM sense amplifier for three workloads is investigated for both SA.

IV. Experimental Results

In this section, we present the analysis results of the experiments mentioned in the previous section.

A. Temporal Impact Experiments

The BTI in MOS transistors affects the sensing delay and the energy of the sense amplifier, i.e., the time required to amplify the input from BL and BLBar to outputs Out and Outbar (see Fig. 1, 2). In order to quantify this delay, we simulate the initial BTI-free SA design, for each technology

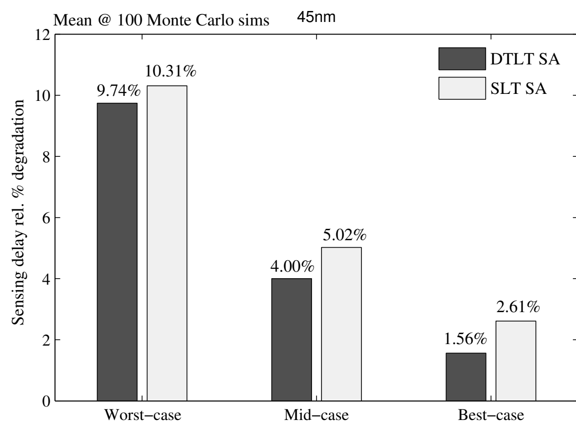

Fig. 6. BTI impact on sensing delay for all workloads and designs.

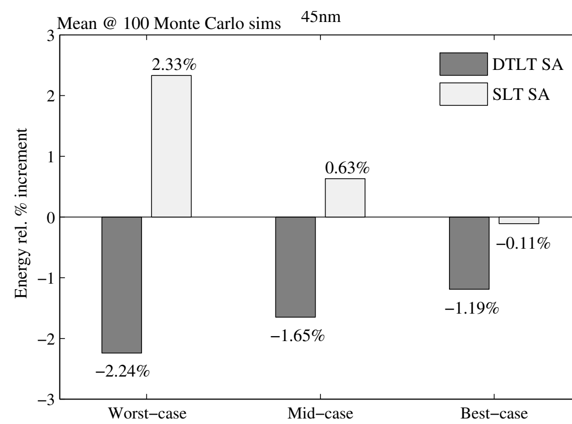

Fig. 7. BTI impact on energy for all workloads and designs.

node and take their sensing delays as references. To obtain proper sensing delays, appropriate values of BL and BLBar should be selected. For 45nm, we assume the differential input to be 100mV (V_{dd}) [12].

Fig. 5 shows the relative increment of the sensing delay and energy w.r.t. the stress time (aging) for mid-case workload. The figure shows a quadratic type of delay increment w.r.t., the stress time. For example, after an operation of 10^8sec, the delay increments equals 5.02% for SLT SA and approaches 4.00% for DTLT SA. Furthermore, the energy consumption increases with 0.63% for SLT SA and reduces with 1.65% for DTLT SA.

B. Workload and Design Dependent Experiments

The BTI induced degradation is sensitive to the workload. The workload defines when and how long each transistor is stressed. Fig. 6 and 7 show the BTI impact on sensing delay and energy consumption, respectively for both SA designs. For the DTLT, i.e., LP application, the sensing delay increases to 9.74% for the worst case workload; while it is 4.00% and 1.56% for mid-case and best-case workload, respectively. The relative energy consumption reduces with severe workloads. Furthermore, for the SLT-SA, i.e., HP application, the sensing delay increases to 10.31% for the worst-case workload; while it is 5.02% and 2.61% for mid-case and best-case workloads, respectively. The energy consumption increases for SLT-SA with severe workloads.

C. Discussion

Reliable and robust SRAM SA designs are crucial for the overall design of memory systems. The current analysis focused on double tail latch type SA and standard latch type SA designs for the nominal supply voltage and room temperature. Sensing delay degrades faster for SLT SA. We observed a reduction in energy consumption for DTLT SA. This is due to the fact that the V_{th} increases for the devices, when the devices get stressed (BTI). However, the increase in energy consumption is not observed for the SLT SA design despite the V_{th} increment. This can be attributed to the fact that the sensing delay increment results in higher dynamic power consumption which negatively impacts the energy consumption.

V. Conclusion

This paper investigated the combined impact of Bias Temperature Instability (BTI) and different workloads on the standard latch type (SLT) and double-tail latch type (DTLT) memory sense amplifiers. In this paper, we have shown that the sensing delay degradation is more impacted by workload that contain more and longer stress periods. We observed for both the DTLT SA and SLT SA an increment in sensing delay when BTI is considered. However, the energy consumption reduces for DTLT while it increases for SLT SA. Therefore, it is crucial for designers to analyze BTI impact at the early design stages.

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