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Comparative Analysis of RD and Atomistic Trap-Based BTI models on SRAM Sense Amplifier

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***Abstract*—Bias Temperature Instability (BTI) in transistors has become a key reliability bottleneck with sub-45nm CMOS technologies. The most common models to characterize BTI are the Reaction-Diffusion (RD) and Atomistic trap-based models. This paper presents comparative impact analysis of RD and Atomistic trap-based BTI models for the SRAM Sense Amplifier. The evaluation metric, the sensing delay is analyzed for both models for the different workloads and supply voltages for 45nm technology node. The results show that the sensing delay degradation is slightly higher in RD model than Atomistic trap-based model for different workloads. Nevertheless, we observe a similar trend for both models. For example the BTI impact degradation is 6.69% for RD model and 6.57% for Atomistic trap-based model when worst case workload is applied for a 10^8s life time.**

***Index Terms*—BTI, NBTI, PBTI, SRAM sense amplifier**

I. Introduction

In recent decades, CMOS technology has been sustained with aggressive downscaling that severely impacts the reliability of devices [1,2,26]. These trends are a consequence of advancements in the fabrication technology, introduction of novel materials and evolution of architecture designs. Bias Temperature Instability (BTI) (i.e., Negative BTI in PMOS transistors and Positive BTI in NMOS transistors) is a reliability failure mechanism which affects the performance of MOS transistors by increasing their threshold voltage and reducing their drain current (I_d) over the operational lifetime [4,21]. However, studies of such individual devices or small composites do not allow extrapolation of these effects on larger circuits like SRAMs.

Static Random-Access Memories (SRAM) occupy a large fraction of semiconductor chip and play a major role in the silicon area, performance, and critical robustness [13]. An SRAM system consists of an array of cells, its peripherals circuits such as row and column address decoders, control circuits, write drivers, and sense amplifiers.

In recent years, there has been an increased attention in modeling BTI failure mechanisms. There are two well known BTI models (i.e., Reaction-Diffusion (RD) models and Atomistic trap-based models) in the field of aging failure mechanisms. Several work has been published on RD and Atomistic models. For instance, Zafar [21] presented BTI as a statistical mechanism based model for negative bias temperature instability induced degradation. Alam [22] presented a critical examination of the mechanics of dynamic NBTI for PMOS. Kaczer et al. [18] proposed Atomistic trap-based model which model BTI and Random Telegraph Noise (RTN) behavior for Sub-45nm devices with workload dependencies. Both models have been independently used at the gate level by researchers. Khan et al. [16] presented BTI analysis of different gates for the dynamic inputs using RD models while including the periodic waveforms only. Kukner et al. [23] analyzed BTI impact on a single inverter using Atomistic trap-based model. However, very limited work is done in comparing both BTI models. Kukner et al. in [19] presents comparison of RD and Atomistic trap-based BTI models for logic gates only while no comparison of the two models has been reported in literature at circuit levels. Further also, Agbo et al. in [5] analyzed an integral impact of BTI and voltage temperature variation on SRAM sense amplifier using RD model while including different workloads, supply voltages and temperatures. Again, Agbo et al. in [20] investigated BTI analysis for high performance and low power SRAM sense amplifier designs using Atomistic model while considering different SA designs. However, comparative analysis of RD and Atomistic trap-based model on circuit level (including sense amplifier) while considering different workloads and supply voltages still needs to be explored. It is worth noting that comparative study of both models at circuit level will help in understanding and selection of the best suited model for quantifying the aging rate of each memory parts required for optimal reliable memory design. This paper focuses on the comparative study of two different BTI models (i.e., RD and Atomistic trap-based models) on SRAM sense amplifiers each targeted for a different application. The standard latch-type sense amplifier design is selected for its superior performance and industrial representativeness [17]. The comparison of the two BTI models impact for standard latch sense amplifier is analyzed using different workloads and supply voltages. The main contributions of the paper are as follows.

- Investigation of BTI impact on the sense amplifier's sensing delay, two different target BTI models are considered.
- Thorough quantitative analysis of the BTI impact using different workloads for 45nm technology node for the two BTI models are investigated.
- Analysis of BTI impact under different supply voltages for SRAM sense amplifier sensing delay using different

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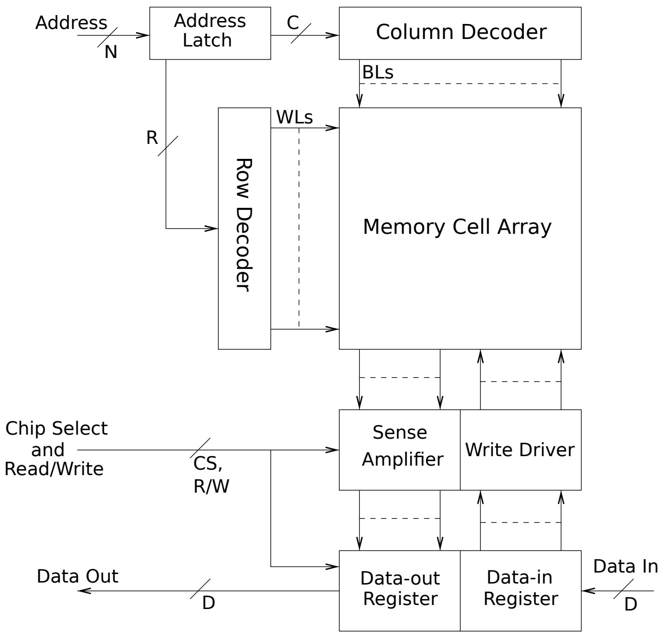

Fig. 1. Functional model of SRAM system

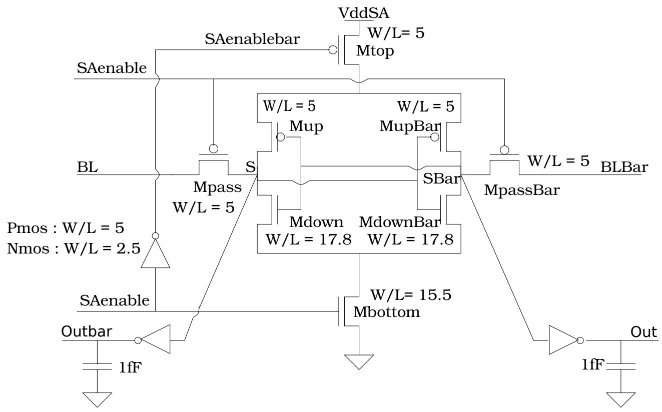

Fig. 2. Standard latch-type Sense Amplifier

workloads for both Reaction-Diffusion (R-D) and Atomistic trap-based models are explored.

- Comparison between RD and Atomistic model for the above mentioned.

The rest of the paper is organized as follows: Section II introduces the sense amplifiers and both BTI models. Section III provides our analysis framework, it presents also the performed experiments. Section IV analyzes the results for comparing both models for different workloads and supply voltages. Finally, Section V concludes the paper.

II. Background

This section presents the working principles of the targeted sense amplifier. Thereafter, it explains the Reaction Diffusion and Atomistic trap-based BTI models analyzed in this paper.

A. Memory model

Figure 1 shows a functional model of the SRAM system [26]. A memory system is comprised of a memory cell array, row and column address decoders, read/write circuitry, input/output data registers and control logic. The main target of this paper is the comparative investigation of Atomistic and RD model on sense amplifier.

B. SRAM Sense Amplifier

Several implementations of sense amplifiers have been proposed. In this section, first the standard latch-type SRAM strobed sense amplifier will be addressed which is representative for industrial SA designs [17].

Standard Latch-Type Sense Amplifier (SLT SA)

A sense amplifier (SA) in SRAMs is responsible for the amplification of a small voltage difference at the bit lines (i.e., BL (BLBar)) during read operations.

The structure of the Standard latch-type Sense Amplifier is depicted in Fig. 2. The width length ratio of each transistor is presented by W/L.

The operation of the sense amplifier comprises of two phases. In the first phase, when SAenable is low, the access transistors Mpass and MpassBar connect to the bitlines (i.e., BL and BLBar) with the internal nodes S (SBar). In this phase, Mtop and Mbottom transistors are switched off. In the second phase, when SAenable is high, the pass transistors disconnect the BL (BLBar) input from the internal nodes. The cross coupled inverters get their current from Mtop and Mbottom and subsequently amplify the difference between S and SBar and produce digital outputs on Out and Outbar. S (SBar) node is actively pulled down when SBar (S) exceeds the threshold voltage of Mdown. The positive feedback loop ensures low amplification time and produces the read value at its output. Moreover, all current paths are disabled when S (SBar) is at 0V and SBar (S) is at $V_{dd\mathrm{SA}}$ or vice versa. This process is repeated for each read operation.

C. Reaction Diffusion Model

The Bias Temperature Instability (BTI) mechanism takes place inside the MOS transistors and causes a threshold voltage shift that impacts the delay negatively; its mechanism is described below.

BTI Mechanism

BTI increases the absolute $\mathrm{V_{th}}$ value in MOS transistors. For the PMOS, the negative $\mathrm{V_{th}}$ is further lower while for NMOS the $\mathrm{V_{th}}$ increases. The increment in the absolute value of the $\mathrm{V_{th}}$ in a PMOS transistor that occurs under *negative* gate stress is referred to as NBTI, and the one that occurs in an NMOS transistor under *positive* gate stress is known as PBTI. For a MOS transistor, there are two BTI phases, i.e., the stress phase and the relaxation phase.

Recently, exhaustive efforts have been put to understand NBTI [4,7,21]. Kaczer *et al.* in [7] have analyzed NBTI using an atomistic model. Alam *et al.* [4] have modeled NBTI and presented the overall dynamics of NBTI as a reaction diffusion process. The model is usable at a higher level such as circuit level. In Kukner *et al.* in [19], both the atomistic and RD models have been compared. The authors conclude that for the long-term simulation time, RD model is lightweight than the atomistic model. For this reason we select this model [4].

Stress Phase: In the stress phase, the Silicon Hydrogen bonds (≡Si-H) break at Silicon-Oxide interface. The broken Silicon bonds (≡Si-) remain at the interface (known as interface traps), and the released H atoms/molecules diffuse towards the gate oxide. The number of interface traps ($\mathrm{N_{IT}}$) generated after applying a stress of time (t) is given by [4]:

$$N_{IT}(t) = \left(\frac{N_o \cdot k_f}{k_r}\right)^{2/3} \cdot \left(\frac{k_H}{k_{H_2}}\right)^{1/3} \cdot (6 \cdot D_0 \cdot t)^{1/6} \quad (1)$$

where $\mathrm{N_o}$, $\mathrm{k_f}$, $\mathrm{k_r}$, $\mathrm{k_H}$, and $\mathrm{k_{H_2}}$, represent initial ≡Si-H density, ≡Si-H breaking rate, ≡Si- recovery rate, H to $\mathrm{H_2}$ conversion rate, and $\mathrm{H_2}$ to H conversion rate inside the oxide layer, respectively. D_0=$\mathrm{D_{H_2}}$.exp$(-\mathrm{E_A}/\mathrm{kT})$ [11] is the diffusion coefficient of the produced $\mathrm{H_2}$ species and $\mathrm{E_A}$ is the activation energy, k is the boltzman constant, and T is the temperature in Kelvin.

Relaxation Phase: In the relaxation phase, there is no ≡Si-H breaking. However, the H atoms/molecules diffuse back towards the interface and anneal the ≡Si- bonds. The number of interface traps that *do not* anneal by the approaching H atoms during the relaxation phase is given by [15]:

$$N_{IT}(t_o + t_r) = \frac{N_{IT}(t_o)}{1 + \sqrt{\frac{\xi \cdot t_r}{t_o + t_r}}} \quad (2)$$

where $\mathrm{N_{IT}(t_o)}$ is the number of interface traps at the start of the relaxation, ξ is a relaxation coefficient with ξ=0.5 [15], $\mathrm{t_o}$ is the duration of the previous stress phase and $\mathrm{t_r}$ is the relaxation duration.

Threshold voltage increment: The $\mathrm{N_{IT}}$ oppose the gate voltage which result in a threshold voltage increment ($\Delta\mathrm{V_{th}}$). The relation between $\mathrm{N_{IT}}$ and $\Delta\mathrm{V_{th}}$ is given by [8]:

$$\Delta V_{th} = (1 + m) \cdot q \cdot N_{IT}/C_{ox} \cdot \chi, \quad (3)$$

where m, q, and $\mathrm{C_{ox}}$ are the holes/mobility degradation that contribute to the $\mathrm{V_{th}}$ increment [9], electron charge, and oxide capacitance, respectively. χ is a BTI coefficient with a value χ=1 for NBTI and χ=0.5 for PBTI [10].

D. Atomistic Model

Kaczer et al. proposed the atomistic model in [18,19]. It is based on the capture and emission of single traps during stress and relaxation phases of NBTI/PBTI respectively. The threshold voltage shift of the device ΔV_{th} is the accumulated results of all the capture and emission of carriers in gate oxide defect traps. The probabilities of the defect occupancy in case of capture P_C and emission P_E are defined by [24]

$$P_C(t_{STRESS}) = \frac{\tau_e}{\tau_c + \tau_e}\left\{1 - exp\left[-(\frac{1}{\tau_e} + \frac{1}{\tau_c})t_{STRESS}\right]\right\} \quad (4)$$

$$P_E(t_{RELAX}) = \frac{\tau_c}{\tau_c + \tau_e}\left\{1 - exp\left[-(\frac{1}{\tau_e} + \frac{1}{\tau_c})t_{RELAX}\right]\right\} \quad (5)$$

where τ_c and τ_e are the mean capture and emission time constants, and t_{STRESS} and t_{RELAX} are the stress and relaxation periods, respectively. [25], gives insight for the relation between (1), (2), and the V_{th}.

III. Analysis Framework

A. Framework Flow

In order to evaluate the BTI impact of both models, we replicate the flows of [5] for RD and [6] for Atomistic model. Next, the generic inputs of both models are described.

Generic input: The general input blocks of the framework are the technology library, Sense Amplifier design, and BTI input parameters.

- Technology library: In this work we only use the 45nm PTM library [27]. Note that in general any library card can be used.
- SA design: Generally, all sense amplifier design can be used. In this paper we focus only on the standard latch-type SA. The SA design is described by a SPICE netlist.
- BTI parameters: The BTI induced degradation depends strongly on the stress time duration. The stress time defines how long the workload sequence is being applied. The workload sequence is assumed to be repeated until the age time is reached. To perform realistic workload analysis, we assume that today's application consists of 10% - 90% memory instructions and the percentage of read instructions is typically 50% - 90%. Furthermore, we derive from this the following cases: best case with a stress period of 0.1 * 0.1 = 0.01, worst case with 0.9 * 0.9 = 0.81, and mid case with 0.5 * 0.5 = 0.25. They lead to the following workload sequences: best-case: $R0R1I^{198}$, worst-case: $R0^4I^1$, mid-case: $(R0)I^{24}$. In these sequences, $R0$ stands for read 0, $R1$ stands for read 1, I for idle operation (which includes memory write operations).

Processing: Here, we described shortly the flows of [5] RD model and [6] Atomistic model.

- RD: There are two processing blocks, the BTI predictor and the HSPICE simulation unit. The long term BTI predictor uses the duty factor, frequency, and aging to predict the interface traps/ threshold voltage increment of each device in the sense amplifier. In addition to workload inputs, inputs are required from the reaction-diffusion model (such as K_f, K_r, D_H, etc.), technology parameters, and voltage temperature (VT). Once the BTI induced V_{TH} increments are calculated per transistor, the original BTI free netlist will be updated. This new netlist is simulated in HSPICE/Verilog-A. **Output:** Finally, post-analysis of the results are performed for varying voltages and temperatures in MATLAB environment.
- Atomistic: Based on the transistor dimensions and the other specified inputs, a Control script (perl) generates several instances of BTI augmented SRAM sense amplifier circuits. Every generated instance has a distinct

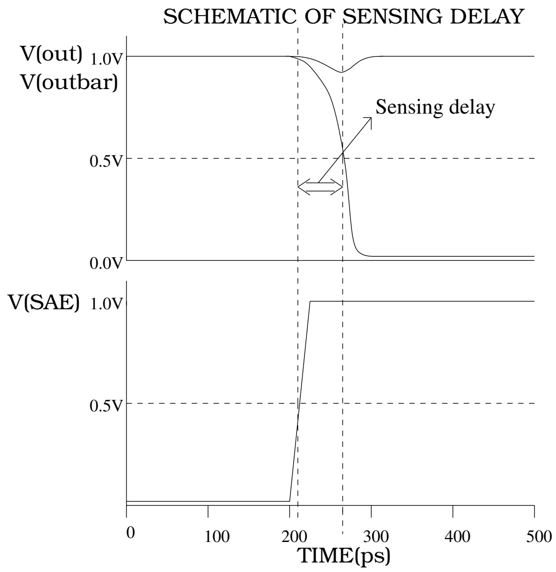

Fig. 3. Metric diagram of Sensing delay.

number of traps (with their unique timing constants) in each transistor, and are incorporated in a Verilog-A module of the SA netlist. The module responds to the every individual trap, and alters the transistors concerned parameters such as V_{th}. After inserting BTI in every transistor of the SA design, a Monte Carlo (MC) is performed at different time steps (100 runs at each time step) where circuit simulator (HSPICE/Spectre) is used to investigate the BTI impact.

B. Output Metrics

In this section, the sensing delay metric used for analyzing BTI impact on sense amplifier is described.

Sensing delay: The sensing delay metric is determined when the trigger signal (i.e.; sense amplifier enable input signal) reaches 50% of the supply voltage and the target (i.e.; either out or outbar falling output signal) reaches 50% of the supply voltage. The sensing delay is defined as the time difference between the target and the trigger as shown in Fig. 3.

C. Experiments Performed

In this paper, three sets of experiments are performed to analyze BTI impacts. These experiments are described below:

1 **Temporal Impact Experiments:** BTI impact on sensing delay for the two models on Sense Amplifier design is investigated for different periods of stress.
2 **Workload Dependent Experiments:** BTI impact on the sensing delay for the two models using three workloads is investigated.
3 **Supply Voltage Dependent Experiments:** BTI impact on the sensing delay of the SRAM sense amplifier for varying supply voltages (i.e., from -10% of V_{dd} to V_{dd} and +10% of V_{dd}) for two workloads (i.e., worst case and best case) and two BTI models (i.e., Atomistic trap-based and Reaction Diffusion) is explored.

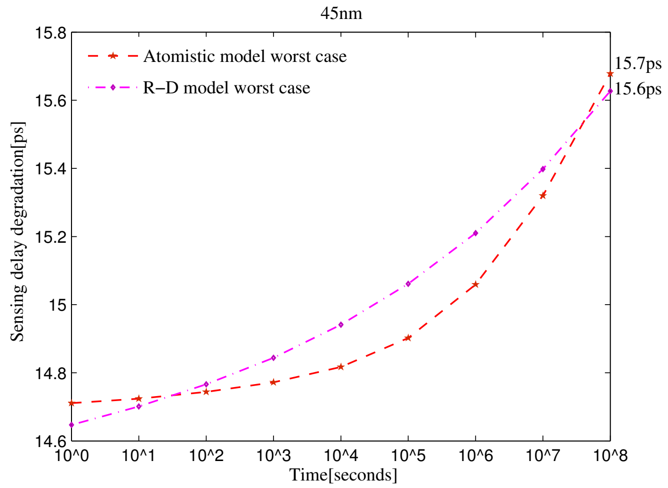

Fig. 4. Reaction Diffusion and Atomistic model BTI impact on sensing delay.

IV. Experimental Results

In this section, we present the analysis results of the experiments mentioned in the previous section. BTI affects the sensing delay of the sense amplifier, i.e., the time required to amplify the input from BL and BLBar to outputs *out* and *outbar* (see Figures 1 and 2). In order to quantify this delay, we simulate the initial BTI-free SA design, for 45nm technology node and take its sensing delay as reference. To obtain proper sensing delays, appropriate values of BL and BLBar should be selected. For 45nm, we assume the differential input to be 89.4mV (V_{dd}) [17].

A. Temporal Impact Experiments

Figure 4 shows the relative increment of the sensing delay w.r.t. the stress time (aging) for worst-case workload for both Atomistic model and R-D model. Both models show a similar trends. For example, for an operation time between 10^0sec and 10^8sec, the delay increases from 14.7ps to 15.7ps for Atomistic model approximately 6.6% and approaches 14.7ps to 15.6ps for R-D model which is 6.7%.

B. Workload Dependent Experiments

The BTI induced degradation is sensitive to the workload. The workload defines when and how long each transistor is stressed. Figure 5 shows the BTI impact on sensing delay for both Atomistic and RD models. For the Atomistic model, the BTI sensing delay degradation for worst case, mid case, and best case equals 14.71ps, 14.67ps and 14.64ps at 10^0s stress, respectively. At 10^8s they equal to 15.69ps, 15.13ps and 14.85ps, respectively. For RD model, these values are 14.65ps, 14.55ps, and 14.50ps at 10^0s and 15.63ps, 15.08ps, and 14.76ps, at 10^8s, respectively. Both models observe the same trends. However, the relative numbers may differ. For example, the relative sensing delay increment equals 6.57% from 10^0s to 10^8s for Atomistic model when worst case is applied. However, for RD model, this degradation at 10^0s worst case is equal to 14.65ps and approaches 14.55ps and 14.50ps for mid case and best case, respectively.

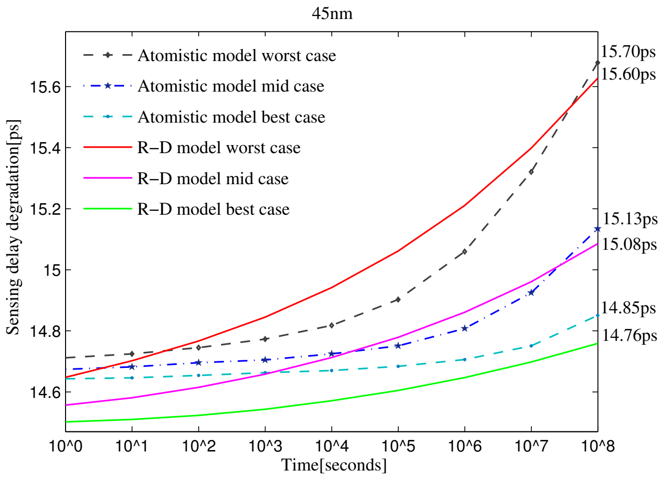

Fig. 5. Atomistic and R-D model BTI impact on sensing delay for all workloads.

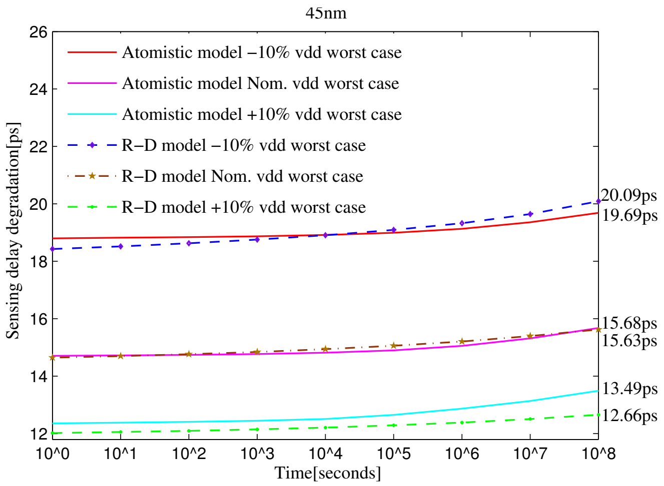

Fig. 6. Atomistic and R-D model BTI impact on varying supply voltage for worst case workload.

There is also significant BTI impact variation for Reaction Diffusion model. For instance, the BTI impact variation is equal to 6.69% for worst case, and approaches 3.63% and 1.78% for mid case and best case, respectively. When comparing the two model w.r.t. sensing delay, in the degradation free case, Atomistic model is 14.71ps for worst case while R-D model is 14.65ps for worst case workload which is 0.41% and approaches 0.76% and 0.97% for the mid case and best case, respectively. There is significant change relatively in the BTI induced degradation for the two models. For instance, Reaction Diffusion model is worse than Atomistic model with 0.12% for the worst case and approaches 0.49% and 0.36% for the mid case and worst case, respectively. Moreover, the two models maintain the same trends for the three workloads considered.

C. Supply Voltage Dependent Experiments

Supply voltage fluctuations generally impact the operating condition of MOS transistors. Supply voltage variations in a transistor can impact the sensing delay significantly as it impacts the operational speed. In addition, variation in supply

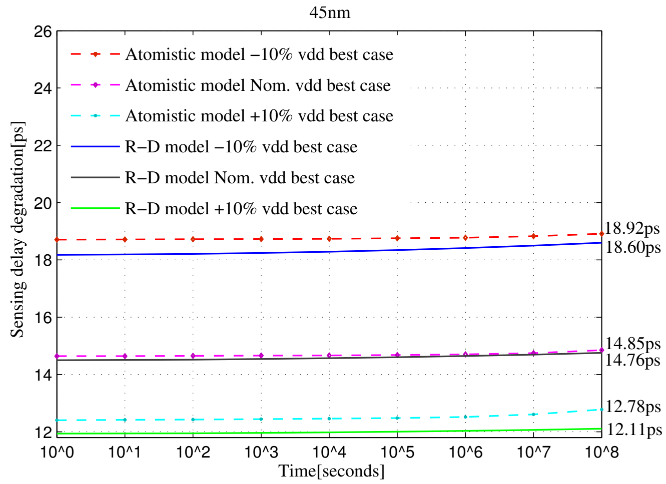

Fig. 7. Atomistic and R-D model BTI impact on varying supply voltage for best case workload.

voltage also affects the oxide field (capacitance) and subsequently the BTI impact (see C_{ox} in Eqn. 3) for RD model. The analysis of the supply voltage variation is performed for both BTI models (i.e., Atomistic and Reaction Diffusion models) and two workloads, (i.e., worst case and best case) for 45nm technology. The supply voltage is varied between -10% and +10% of nominal V_{dd}, i.e., between 0.9V and 1.1V. Figures 6 and 7 depict the BTI induced sensing delay for various supply voltages and BTI models for the worst case and best case workloads, respectively. From the figures we conclude the following:

- Increasing the supply voltage reduces the sensing delay degradation. For instance, in Figure 6, for an Atomistic trap-based model, the BTI degradation at 10^0s is 12.36ps, 14.71ps and 18.80ps for $+10\%$ V_{dd}, nominal V_{dd} and -10% V_{dd}, respectively. At 10^8s, the sensing delay equals 13.49ps, 15.68ps and 19.69ps for $+10\%$ V_{dd}, nominal V_{dd} and -10% V_{dd}, respectively. The absolute numbers of varying supply voltage for Atomistic trap-based model maintain the claim of increase in supply voltage reduces the sensing delay degradation. The relative increment of the varying supply voltage for Atomistic trap-based model shows an opposite trend, for $+10\%$ V_{dd} the sensing delay increment equals 9.19% while 6.57% and 4.72% for nominal V_{dd} and -10% V_{dd}, respectively.

  The figure also shows, for Reaction Diffusion model, the BTI degradation at 10^0s is 12.02ps, 14.65ps and 18.43ps for $+10\%$ V_{dd}, nominal V_{dd} and -10% V_{dd}, respectively. Then, for BTI induced degradation at 10^8s is 12.66ps, 15.63ps and 20.09ps for $+10\%$ V_{dd}, nominal V_{dd} and -10% V_{dd}, respectively. The Reaction Diffusion model varying supply voltage absolute numbers also maintain the claim that increasing the supply voltage mitigates the sensing delay degradation. Furthermore, the relative numbers for R-D model varying supply voltages shows a consistent trend with the absolute numbers, for $+10\%$ V_{dd} the sensing delay is 5.26% while 6.69% and

9.03% for nominal V_{dd} and -10% V_{dd}, respectively.

- Figure 7 shows also increasing the supply voltage reduces the sensing delay degradation for best case workload. For instance, for an Atomistic model, e.g., +10% V_{dd}, the BTI degradation free case is 12.41ps while 14.64ps and 18.71ps for nominal V_{dd} and -10% V_{dd}, respectively. Furthermore, in the BTI induced degradation at 10^8s, +10% V_{dd} = 12.78ps and approaches 14.85ps and 18.92ps for nominal V_{dd} and -10% V_{dd}, respectively. The absolute numbers of the best case maintains the trend that increasing the V_{dd} mitigates the sensing delay degradation. However, this trends relatively is reversed, for e.g., +10% V_{dd} is equal to 3.01% while 1.43% and 1.10% for nominal V_{dd} and -10% V_{dd}, respectively.

  Besides, the figure shows varying supply voltages (i.e., -10% V_{dd}, Nom. V_{dd}, and +10% V_{dd}) for RD model best case. For instance, in BTI degradation at 10^0s is 11.94ps while 14.50ps and 18.18ps for +10% V_{dd}, nominal V_{dd} and -10% V_{dd}, respectively. Then, for BTI induced degradation at 10^8s is 12.11ps, 14.76ps and 18.60ps for +10% V_{dd}, nominal V_{dd} and -10% V_{dd}, respectively. For RD model best case varying V_{dd} absolute numbers sensing delay BTI impact keep to the trend that increasing the supply voltage reduces the sensing degradation. Moreover, the same trends is observed in the relative increment, for $+10\%$ V_{dd} is 1.45% while 1.78% and 2.34% for $+10\%$ V_{dd}, nominal V_{dd} and -10% V_{dd}, respectively. In conclusion, both models absolute numbers for worst case and best case workload varying supply voltage sensing delay are consistent with the trends, increase in supply voltages results in reduced BTI induced sensing delay degradation. However, both models show opposite trend relatively for increasing supply voltages in the presence of BTI induced degradation.

D. Discussion

Reliable and robust SRAM SA designs are crucial for the overall design of memory systems, and also to the design community. The current analysis focused on comparative study of both Atomistic trap-based and Reaction-Diffusion model on standard latch type SA for different supply voltages and workloads. Both models predict a similar reliability impact (in terms of delay) for the considered SA. We observed slightly higher sensing delay degradation in RD model than Atomistic model for various workloads. The V_{th} for Atomistic model is based on stochastic analysis. So the same circuit will result in a range of sensing delay increments, while for the RD model a single sensing delay increment value is used in our analysis. Therefore, based on the calibrations and the stochastic nature of Atomistic model, we conclude that it is best suited for BTI as it also includes worst-case and best-case analysis.

V. Conclusion

This paper investigated the combined impact of Bias Temperature Instability (BTI), different workloads and supply voltages on the standard latch type (SLT). The sensing delay degradation is more impacted by workload that contain more and longer stress periods and reduces with higher supply voltages. These trends have been observed by both the Reaction Diffusion and Atomistic trap-based BTI models.

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