Integral Impact of BTI and Voltage Temperature Variation on SRAM Sense Amplifier

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***Abstract*—With the continuous downscaling of CMOS technologies, ICs become more vulnerable to transistor aging mainly due to Bias Temperature Instability (BTI). A lot of work is published on the impact of BTI in SRAMs; however most of the work focused mainly on the memory cell array. An SRAM consists also of peripheral circuitries such as address decoders, sense amplifiers, etc. This paper characterizes the combined impact of BTI and voltage temperature fluctuations on the memory sense amplifier for different technology nodes (45nm up to 16nm). The evaluation metric, the sensing delay (SD), is analyzed for various workloads. In contrast to earlier work, this paper thoroughly quantifies the increased impact of BTI in such sense amplifiers for all the relevant technology scaling parameters. The results show that the BTI impact for nominal voltage and temperature is 6.7% for 45nm and 12.0% for 16nm when applying the worst case workload, while this is 1.8% for 45nm technology and 3.6% higher for 16nm when applying the best case workload. In addition, the results show that the increase in power supply significantly reduces the BTI degradation; e.g., the degradation at $-10\%V_{dd}$ is 9.0%, while this does not exceed 5.3% at $+10\%V_{dd}$ at room temperature. Moreover, the results that the increase in temperature can double the degradation; for instance, the degradation at room temperature and nominal V_{dd} is 6.7% while this goes up to 18.5% at 398K.**

***Index Terms*—BTI, NBTI, PBTI, SRAM sense amplifier**

I. Introduction

In recent decades, CMOS technology has been sustained with aggressive downscaling that severely impacts the reliability of devices [1,2,28]. These trends are due to advancements in the fabrication technology, introduction of novel materials and evolution of architecture designs. Bias Temperature Instability (BTI) (i.e., Negative BTI in PMOS transistors and Positive BTI in NMOS transistors) is a reliability failure mechanism which affects the performance of MOS transistors by increasing their threshold voltage and reducing their drain current (I_d) over the operational lifetime [5,11]. However, studies of such individual devices or small composites do not allow extrapolation of these effects on larger circuits like SRAMs.

Static Random-Access Memories (SRAM) occupy a large fraction of semiconductor chip and play a major role in the silicon area, performance, and critical robustness [12]. An SRAM system consists of an array of cells, its peripherals circuits such as row and column address decoders, control circuits, write drivers, and sense amplifiers. Designing an optimal reliable memory system requires the consideration of all its sub-parts, i.e., their degradation rate depends on the application (e.g. workload, temperature, etc); for instance, the aging rate of the sense amplifier may differ from that of the memory array and other peripheral circuits.

Many publications analyzed the BTI impact on SRAM cell array, while very limited work is published on the SRAM peripheral circuitry. For instance, Binjie *et al.* [17] investigated NBTI impact on Static Noise Margin (SNM) and Write Noise Margin (WNM) degradation of 6T SRAM cell. Kumar *et al.* [18] Analyzed the impact of NBTI on the read stability and SNM of SRAM cells. Andrew [19] investigated the mechanism of NBTI degradation on SRAM metrics such as SNM. Bansal et al [20] presented insights on the stability of an SRAM cell under the worst-case conditions and analyzed the effect of NBTI and PBTI, individually and collectively. Rodopoulos *et al.* [22] investigated the atomistic pseudo-transient BTI simulation with built-in workloads. Khan et al [23] investigated BTI analysis of FinFET based SRAM cell.

On the other hand, few authors have focused on reliability analysis of the SRAM peripheral circuit. Khan *et al.* [21] investigated the impact of partial opens conjuction BTI in SRAM address decoders. Menchaca *et al.* [24] analyzed the BTI impact on different sense amplifier designs implemented on 32nm technology node by using failure probability (i.e., flipping a wrong value) as a reliability metric. Agbo *et al.* [25] investigated the BTI impact on SRAM drain-input latch type sense amplifier design implemented on 90nm, 65nm, and 45nm for different supply voltages by using sensing delay and sensing voltage as reliability metrics. However, quantitative analysis of BTI impact of peripheral circuits (including sense amplifiers) while considering different workloads, temperatures, supply voltages and how they correlate with technology scaling is still to be explored. It is worth noting that understanding and quantifying the aging rate of each memory part is needed for optimal reliable memory design; this is because the different parts may degrade with different rates depending e.g. on the workload (application).

This paper focuses on standard latch-type sense amplifier design due to its superior performance [30] and analyzes the BTI impact for different temperatures and supply voltages, and different workloads. The main contributions of the paper are as follows:

- Investigation of BTI impact on the sense amplifier's sensing delay. In contrast to previous work, we analyze the BTI stress and relaxation cycles for each transistor individually to obtain more accurate results. These stress and relaxation cycles are workload dependent. In this

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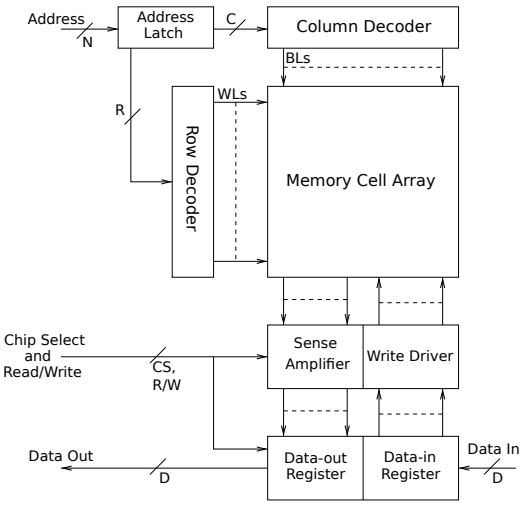

Fig. 1. Functional model of SRAM system

work we define eight realistic workloads.

- Investigation of BTI impact on different workloads for different technology nodes.
- Thorough quantitative analysis of the BTI impact on the sense amplifier for deeply nano-scaled technology nodes, i.e., 45nm, 32nm, 22nm, and 16nm.
- Analysis of BTI impact under different supply voltages and temperatures on the SRAM sense amplifier sensing delay using different workloads.

The rest of the paper is organized as follows: Section II introduces the SRAM model, standard latch-type sense amplifier, BTI mechanism and its model. Section III provides our analysis framework, analysis metric, and the performed experiments. Section IV analyzes the result for different technology nodes, workloads, varying supply voltages and temperatures. Finally, Section V concludes the paper.

II. Background

This section presents first the functional SRAM model. Afterwards, it focuses on the behavior of the standard latch-type sense amplifier. Finally, it explains the BTI mechanisms and its model analyzed in this paper.

A. Memory model

Figure 1 depicts a functional model of the SRAM system [28]. A memory system is comprised of a memory cell array, row and column address decoders, read/write circuitry, input/output data registers and control logic. The main focus of the paper is the sense amplifier.

SRAM Sense Amplifier

Several implementations of sense amplifiers have been proposed. In this paper, the standard latch-type SRAM strobed sense amplifier will be addressed which is representative for industrial SA designs [30].

The structure of the Standard latch-type Sense Amplifier is depicted in Fig. 2. The width length ratio of each transistor is presented by W/L.

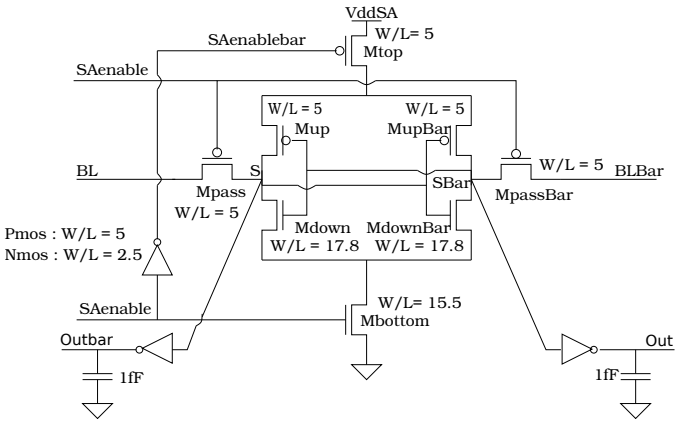

Fig. 2. Standard latch-type Sense Amplifier

The operation of the sense amplifier consists of two phases. In the first phase, when SAenable is low, the access transistors Mpass and MpassBar connect to the BL (BLBar) with the internal nodes S (SBar). In this phase, Mtop and Mbottom transistors are switched off. In the second phase, when SAenable is high, the pass transistors disconnect the BL (BLBar) input from the internal nodes. The cross coupled inverters get their current from Mtop and Mbottom and subsequently amplify the difference between S and SBar and produce digital outputs on Out and Outbar. S (SBar) node is actively pulled down when SBar (S) exceeds the threshold voltage of Mdown. The positive feedback loop ensures low amplification time and produces the read value at its output. Moreover, all current paths are disabled when S (SBar) is at 0V and SBar (S) is at $V_{dd\mathrm{SA}}$ or vice versa. This process is repeated for each read operation.

B. Bias Temperature Instability

BTI mechanism takes place inside the MOS transistors and causes a threshold voltage shift that impacts the delay negatively; its mechanism is described below.

BTI Mechanism

BTI increases the absolute $\mathrm{V_{th}}$ value in MOS transistors. For PMOS, negative BTI (NBTI) reduces the $\mathrm{V_{th}}$ while for NMOS, positive BTI (PBTI) the $\mathrm{V_{th}}$ increases. Recently, exhaustive efforts have been put to understand NBTI [5,10,11]. Kaczer *et al.* in [10] have analyzed NBTI using an atomistic model. Alam *et al.* [5] have modeled NBTI and presented the overall dynamics of NBTI as a reaction diffusion process. The model is usable at a higher level such as circuit level. In Kukner *et al.* in [26], both the atomistic and RD models have been compared. The authors conclude that for the long-term simulation time, RD model is lightweight than the atomistic model. For this reason we select this model [5]. For a MOS transistor, there are two BTI phases, i.e., the stress phase and the relaxation phase.

Stress Phase: In the stress phase, the Silicon Hydrogen bonds (≡Si-H) break at Silicon-Oxide interface. The broken Silicon bonds (≡Si-) remain at the interface (known as interface traps), and the released H atoms/molecules diffuse towards the gate

oxide. The number of interface traps (N_{IT}) generated after applying a stress of time (t) is given by [5]:

$$N_{IT}(t) = \left(\frac{N_o \cdot k_f}{k_r}\right)^{2/3} \cdot \left(\frac{k_H}{k_{H_2}}\right)^{1/3} \cdot (6 \cdot D_0 \cdot t)^{1/6} \quad (1)$$

where N_o, k_f, k_r, k_H, and k_{H_2}, represent initial ≡Si-H density, ≡Si-H breaking rate, ≡Si- recovery rate, H to H_2 conversion rate, and H_2 to H conversion rate inside the oxide layer, respectively. D_0=D_{H_2}.exp($-E_A/kT$) [6] is the diffusion coefficient of the produced H_2 species and E_A is the activation energy, k is the boltzman constant, and T is the temperature in Kelvin.

Relaxation Phase: In the relaxation phase, there is no ≡Si-H breaking. However, the H atoms/molecules diffuse back towards the interface and anneal the ≡Si- bonds. The number of interface traps that *do not* anneal by the approaching H atoms during the relaxation phase is given by [18]:

$$N_{IT}(t_o + t_r) = \frac{N_{IT}(t_o)}{1 + \sqrt{\frac{\xi \cdot t_r}{t_o + t_r}}} \quad (2)$$

where $N_{IT}(t_o)$ is the number of interface traps at the start of the relaxation, ξ is a relaxation coefficient with ξ=0.5 [18], t_o is the duration of the previous stress phase and t_r is the relaxation duration.

Threshold voltage increment: The N_{IT} oppose the gate voltage which result in a threshold voltage increment (ΔV_{th}). The relation between N_{IT} and ΔV_{th} is given by [4]:

$$\Delta V_{th} = (1 + m) \cdot q \cdot N_{IT}/C_{ox} \cdot \chi, \quad (3)$$

where m, q, and C_{ox} are the holes/mobility degradation that contribute to the V_{th} increment [16], electron charge, and oxide capacitance, respectively. χ is a BTI coefficient with a value χ=1 for NBTI and χ=0.5 for PBTI [14].

III. Analysis Framework

In this section, the analysis framework of the standard latch type sense amplifier circuit is described. Furthermore, the workloads used in performing the experiment are explained. Thereafter, the output performance metric is presented. Finally, the conducted experiments are presented.

A. Framework Flow

Figure 3 depicts a flexible and generic BTI framework for the standard latch type sense amplifier circuit. The framework evaluates the BTI impact for different designs, technologies, workload under normal conditions and considering VT (i.e., voltage, and temperature) variations. The framework consist of a MATLAB and HSPICE working environment. The MATLAB environment typically is used for pre-processing and post-processing, it prepares BTI augmented files to run in HSPICE. The results of HSPICE that simulates the BTI augmented netlist, are subsequently post-processed in MATLAB. Furthermore, the framework analysis is divided into three parts (i.e., input, processing, and output blocks) and they are explained next.

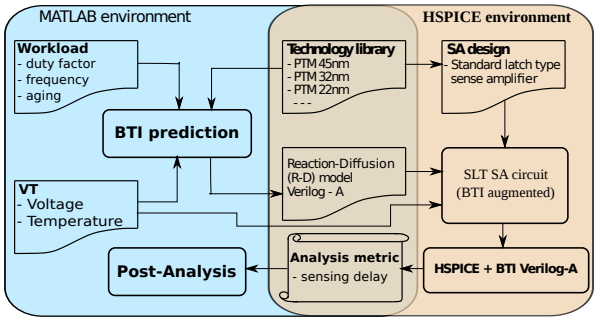

Fig. 3. Analysis framework for the standard latch sense amplifier circuit.

Input: The general input blocks of the framework are the SA design, technology library, workload, and voltage temperature (VT). They are explained as follows.

- SA design: Generally, all sense amplifier design can be used. In this paper we focus only on the standard latch type sense amplifier. The SA design is described by an HSPICE netlist.
- Technology library: Different technology nodes are considered in this work, they are 45nm, 32nm, 22nm, and 16nm and are obtained from PTM library cards [31].
- VT: This block specifies the temperatures and voltages. In this paper, we restrict ourselves to temperatures T_1 = 298K, T_2 = 348K, and T_3 = 398K and supply voltages V_1 = -10%V_{dd}, V_2 = V_{dd}, and V_3 = +10%V_{dd}. Note that each technology has its own nominal voltage.
- Workload: The shift in threshold voltage is a function of stress and relaxation durations of the transistors. This implies that BTI degradation depends on the amount of ON and OFF (idle) states of the input patterns which translates to workload. To perform this analysis, we assume that today's application consists of 10% - 90% memory instructions and the percentage of read instructions is typically 50% - 90%. Furthermore, we derive from this the following cases: best case with stress period of 0.1 * 0.1 = 0.01, worst case with 0.9 * 0.9 = 0.81, and mid case: 0.5 * 0.5 = 0.25. They lead to the following workload sequences: $S1$: $R0I^{99}$, $S2$: $R0R1I^{198}$, $S3$: $R0^4I^1$, $S4$: $(R0R1)^4I^2$, $S5$: $(R0)I^{24}$, $S6$: $(R0R1)I^{24}$, $S7$: $(R0)I^{50}$, and $S8$: $(R0R1)I^{50}$. In these sequences, $R0$ stands for read 0, $R1$ stands for read 1, I for idle operation (which includes memory write operations). For example, $S1$: $R0I^{99}$ is workload where read 0 is followed by 99 idle operations. The best and worst case will be analyzed in most detail.

The workload inputs are typically characterized by their duty factor, frequency, and aging (or stress time). The BTI impact sensitivity is highly dependent on the input stimulus clock cycle (i.e., frequency), its aging and duty factor (DC stress or AC stress) w.r.t., the affected device or circuitry.

i **Frequency** The BTI induced degradation depends on the signal frequency to the sense amplifier design. In this experiment, the frequencies considered for the SA design are 1.32GHz, 1.89GHz, 2.70GHz, and 3.86GHz for 45nm,

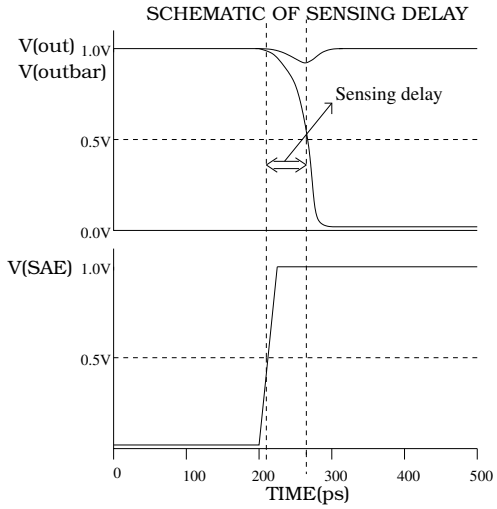

Fig. 4. Metric diagram of Sensing delay.

32nm, 22nm, and 16nm technology nodes, respectively.

ii **Aging** The BTI induced degradation depends strongly on the stress time. The stress time defines how long the workload sequence is being applied. A workload sequence is assumed to be repeated until the age time is reached.

iii **Duty Factor** The input signal is a function of the duty factor that affects the BTI induced degradation of the sense amplifier design. The duty factor of the input SA enable signal (see Figure 4.) is approximately 0.48. This applies only to read operations. During write or idle operations, SAenable signal is disabled. From the waveform analysis, we extract for all transistors individually their stress and relaxation cycles; thereby is able to obtain accurate duty cycles for each transistor. This enhances the accuracy of our simulation results. Based on the duty factor and age time, interface traps (Eqns. 1 and 2) or threshold voltage increments (Eqn. 3) can be attributed to all transistors in an accurate manner.

Processing: There are two processing blocks, the BTI predictor and the HSPICE simulation unit. The long term BTI predictor uses the duty factor, frequency, and aging to predict the interface traps/ threshold voltage increment of each device in the sense amplifier. In addition to workload inputs, inputs are required from the reaction-diffusion model (such as K_f, K_r, D_H, etc.), technology parameters, and voltage temperature (VT). Once the BTI induced V_{TH} increments are calculated per transistor, the original BTI free netlist will be updated. This new netlist is simulated in HSPICE/Verilog-A.
Output: Finally, post-analysis of the results are performed for varying voltages and temperatures in MATLAB environment.

B. Output Analysis Metrics

In this section, the sensing delay metric used for analyzing BTI impact on sense amplifier is described.

Sensing delay: The sensing delay metric is determined when the trigger signal (i.e., sense amplifier enable input signal) reaches 50% of the supply voltage and the target (i.e., either out or outbar falling output signal) reaches 50% of the supply voltage. The difference between the target and the trigger

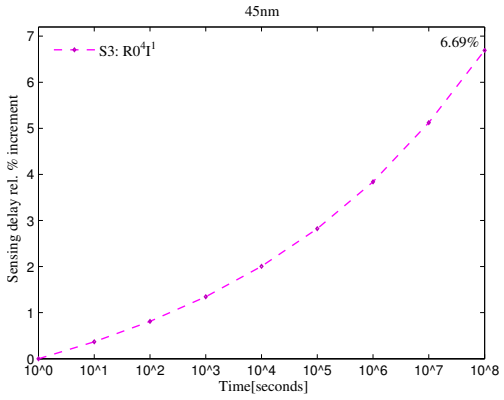

Fig. 5. BTI impact on Sensing delay.

results in sensing delay as shown in Fig. 4. Furthermore, the relative variation of the sensing delay due to BTI is the difference between the measured sensing delay when BTI is added and referenced sensing delay when BTI is not added.

C. Experiments Performed

In this paper, four sets of experiments are performed to analyze BTI impacts. These experiments are described below:

1 **BTI Impact Experiments:** BTI impact on sensing delay of the SRAM sense amplifier is investigated.
2 **Workload Dependent Experiments:** BTI impact on the sensing delay of the SRAM sense amplifier for different workloads on different technology nodes is investigated.
3 **Technology Dependent Experiments:** BTI impact on sensing delay using different technology nodes is investigated.
4 **Supply Voltage and Temperature Dependent Experiments:** BTI impact on sensing delay of the SRAM sense amplifier for varying supply voltages (i.e., $-10\%V_{dd}$, V_{dd} and $+10\%$ V_{dd}) and temperatures (i.e., $298K$, $348K$ and $398K$) for different technology nodes are explored.

IV. EXPERIMENTAL RESULTS

In this section, we present the analysis results of the experiments mentioned in the previous section.

A. Temporal BTI Impact

The BTI in MOS transistors affect the sensing delay of the sense amplifier, i.e., the time required to amplify the input from BL and BLBar to outputs Out and Outbar (see Figure 2). In order to quantify this delay, we simulate the initial BTI-free SA design, for each technology node and take their sensing delays as references. To obtain proper sensing delays, appropriate values of BL and BLBar should be selected. For 45nm, we assume the differential input to be 100mV (V_{dd}) [30]. Subsequently, we modify this differential voltage in such a way to meet up with the frequencies of the lower technology nodes. Note that the transistors are scaled with each technology.
Figure 5 shows the relative increment of the sensing delay w.r.t., the stress time (aging) for workload $S3$ using 45nm technology. The figure shows a quadratic delay increment with respect to the stress time. For example, after 10^8sec the delay increments equals 6.69% due to BTI.

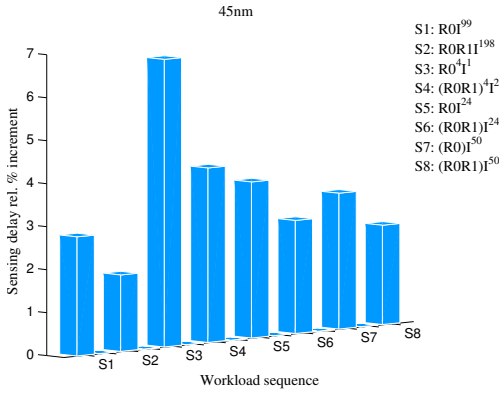

Fig. 6. Workload dependent Sensing delay.

B. Workload Dependency

The BTI induced degradation is sensitive to the workload. Hence, this workload-dependent behaviour is one of the main contributions of this study. A better understanding of this behaviour will strongly help to select the proper mitigation schemes and to reduce the cost for highly dynamic cost-sensitive embedded systems. The workload defines when and how long each transistor is stressed. Figure 6 shows the relative BTI induced sensing delay for sequences $S1$, $S2$, $S3$, $S4$, $S5$, $S6$, $S7$, and $S8$ respectively. There is a significant variation in the relative sensing delay increment. For instance, workload sequence, $S2$ ($R0R1I^{198}$) has a lower impact as it is activated (stressed) only 1% of the signal duration than the other workloads, whereas workload sequence, $S3$ ($R0^4I^1$) has the highest impact as it is activated (stressed) 80% of the signal duration. The remaining workloads result in a delay increment between the extreme cases $S2$ and $S3$. The same trends are observed for the other technology nodes.

C. Technology Dependency

CMOS technology scaling results in an apparent oxide field increment which speeds up the BTI covalent bond breaking phenomenon and thus the BTI induces threshold voltage. Therefore, it is essential to evaluate the reliability of different technology nodes. Experiments are performed at nominal supply voltage and temperature (T_1 = 298K) for different technology nodes with their corresponding supply voltages 1.0V, 0.9V, 0.8V, and 0.7V for 45nm, 32nm, 22nm, and 16nm, respectively. Here, we focus only on the best and worst case workloads $S2$ and $S3$ respectively. Experiments are performed to investigate the impact of BTI on sensing delay for different technologies for worst and best case workloads, i.e., workloads S3 and S2, respectively. Figure 6 depicts the sensing delay of these experiments for a stress time of 10^8s. The figure shows for both the worst case and best case workloads that the relative delay increment increases with advanced technology nodes. However, this increment is larger for the worst case workload. For instance, the variation for the worst case workload increases from 6.7% for 45nm to 12.0% for 16nm, while for the best case the increment is 1.8% for 45nm and 3.6% for 16nm only.

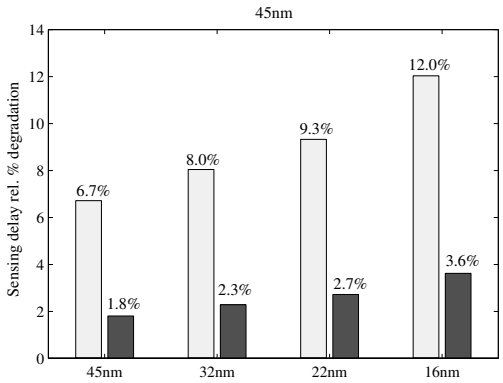

Fig. 7. BTI impact on Sensing delay for all technology nodes.

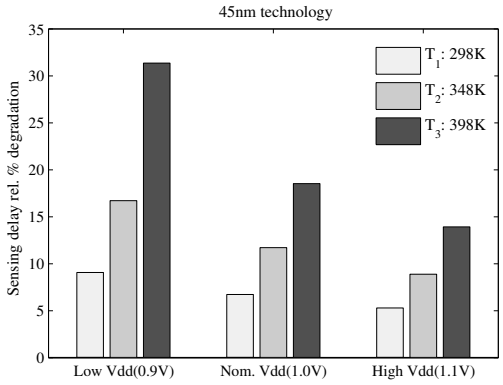

Fig. 8. Worst case sensing delay for supply voltage and temperature variations.

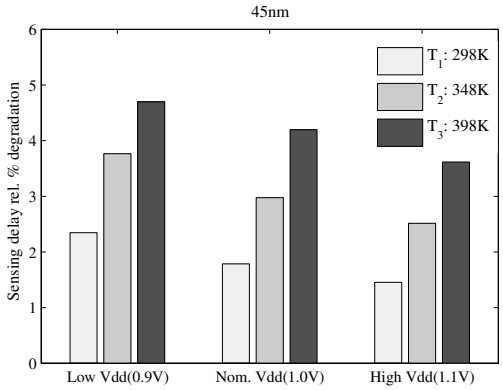

Fig. 9. Best case sensing delay for supply voltage and temperature variations.

D. Supply Voltage and Temperature Dependency

Conventionally, supply voltage and temperature fluctuations impact the operating condition of MOS transistors. Supply voltage variations in a transistor can impact the sensing delay significantly as it impacts the operational speed. In addition, variation in supply voltage also affects the oxide field (capacitance) and subsequently the BTI impact (C_{ox} in Eqn. 3). The analysis of the supply voltage variation is performed on two workloads, (i.e., worst-case (S3) and best-case (S2)) for 45nm technology. The supply voltage is varied between -10% and +10% of nominal V_{dd}, i.e., between 0.9V and 1.1V. Figures 8 and 9 depict the BTI induced sensing delay for various supply voltages and temperatures for the worst-case and best-case workloads, respectively. The figures show for different voltages, i.e., low V_{dd} (Low V_{dd} = 0.9V), nominal V_{dd} (Nom. V_{dd} = 1.0V), and high V_{dd} (High V_{dd} = 0.9V) and

temperatures (i.e., T_1 = 298K, T_2 = 348K, and T_3 = 398K) the impact on the sensing delay (vertical axis). From the figures we conclude the following:

- Increasing the temperature leads to a higher BTI induced degradation. For example, in Figure 8, for a fixed supply voltage, e.g., V_{dd} = 1.1V, the BTI induce degradation is 5.3% for T_1, and while 8.9% and 13.9% for T_2 and T_3, respectively. In addition to that, the same trend is observed at V_{dd} = 1.0V and V_{dd} = 0.9V. In Figure 9, for considering V_{dd} = 1.1V as a fixed reference, the relative sensing delay degradation becomes 1.5% for T_1 while 2.5% and 3.6% for T_2 and T_3, respectively.
- Increasing the supply voltage reduces the sensing delay degradation. For instance, in Figure 8, for a fixed temperature, e.g., T_1, the BTI induced degradation on the sensing delay at 10^8s is 9.0% for low V_{dd}, while 6.7%, and 5.3% for nominal V_{dd} and high V_{dd}, respectively. Moreover, the same trend is observed at T_2 and T_3. In Figure 9, for fixed T_1, the relative sensing delay degradation is 2.3% for V_{dd} = 0.9V, while 1.8% and 1.5% for V_{dd} = 1.0V and V_{dd} = 1.1V, respectively.
- The performance degradation is much higher for the worst-case workload (S3) as compared to the best-case workload (S2). For instance, in Figure 8, at low V_{dd} and T_3 = 398K, the sensing degradation is 31.3% while in Figure 9, for the same voltage and temperature, the BTI induced degradation is only 4.7%.

In conclusion, based on the experiments, it is extremely important for designers to include proper design margins to guarantee the life-time operation of the considered SA circuitry under given operating conditions (such as voltage and temperature). In order to design a reliable memory system, designers need to understand the degradation of each sub-component. Based on such information, monitoring and mitigation schemes might be considered for SAs. For example, a sensing delay monitoring circuit could be used as sensor to adaptively control the supply voltage. Another approach could focus on redesigning more robust SA, by increasing the drive strength (or device width) of critical transistors [29].

V. Conclusion

This paper investigated the combined impact of Bias Temperature Instability (BTI), voltage and temperature variation and different workloads on the standard latch type memory sense amplifier for different technologies. The results show that the sensing delay degradation is strongly workload dependent and reaches up to 12.8%. Both the scaling and increase in temperature severely impact the BTI degradation. Increasing the supply voltage reduces the BTI induced degradation leading to more reliable and robust sense amplifiers, but at the cost of a higher power consumption. Optimizing a reliable memory system requires the consideration of all its sub-parts, i.e., their degradation rate depends on the application (e.g. workload, temperature, etc); for instance, the aging rate of the sense amplifier may differ from that of the memory array and other peripheral circuits.

References

[1] ITRS, "International Technology Roadmap for Semiconductor 2004" "www.itrs.net/common/2004 update/2004update.htm.".

[2] S. Borkar, et al "Micro architecture and Design Challenges for Giga scale Integration", *Pro. of Intl. Sympos. Micro architecture*, 2004.

[3] S. Hamdioui et al, "Reliability Challenges of Real-Time Systems in Forthcoming Technology Nodes", *DATE*, 2013.

[4] B.C. Paul et al, "Impact of NBTI on the Temporal Performance Degradation of Digital Circuits", *IEEE Electron Device Letter*, Vol. 26, No.8, Aug. 2005.

[5] M. A. Alam et al, "A Comprehensive Model of PMOS NBTI Degradation", *Microelectronics Reliability* , Vol:45, 2005.

[6] D. Varghese, et al, "On the Dispersive versus Arrhenius Temperature Activation of NBTI Time Evolution in Plasma Nitrided Gate Oxides: Measurements, Theory, and Implications", *IEDM*, Dec. 2005, pp. 1-4.

[7] K. Kang, et al, "Estimation of Statistical Variation in Temporal NBTI Degradation and Its Impact on Lifetime Circuit Performance", *ICCD*, 2005, pp. 730-734.

[8] R. Wang, et al., Threshold Voltage Variation with Temperature in MOS Transistors, *IEEE Transaction on Electron Devices*, pp: 386- 388, 1971.

[9] S. Sapatnekar, et al., Overcoming Variatins in Nano-scale Technologies, IEEE Transaction on Emerging and Selected Topics in Circuits and Systems, pp: 5-18, 2011.

[10] B. Kackzar, et al., "Disorder-Controlled-Kinetics Model NBTI and its Experimental Verification", *IPRS* , pp: 381-387, 2005.

[11] S. Zafar, et al, "A comparative study of NBTI and PBTI in SiO2/HfO2 stacks with FUSI, TiN gates", *Pro. of VLSI Technology symp.*, 2006.

[12] P. Pouyan, et al, "Process Variability-Aware Proactive Reconfiguration Technique for Mitigating Aging effects in Nano Scale SRAM lifetime", *IEEE 30th VLSI Test Symposium.*, 2012.

[13] D. Rodopoulos, et al, "Time and Workload Dependent Device Variability in Circuit Simulations" *Proc. Intl. Conf on IC Design and Technology*, pp: 1-4, 2011.

[14] M. T. Luque, et al, "From Mean Values to Distribution of BTI Lifetime of Deeply scaled FETs through Atomistic Understanding of the Degradation" *Sym. on VLSI Technology*, pp: 152-153, 2011.

[15] T. Sakurai et al, "Alpha-Power law MOSFET model and its applications to CMOS delay and other formulas", *IEEE JSSC*, Vol.25, No.2, April 1990,

[16] A. T. Krishnan, et al, "NBTI impact on transistor and circuit: Models, mechanisms and scaling effects", *IEDM*, 2003.

[17] B. Cheng, A. R. Brown, "Impact of NBTI/PBTI on SRAM Stability Degradation", *IEEE ELECTRON DEVICES LETTERS*, 2011.

[18] S. Kumar et al, "Impact of NBTI on SRAM Read Stability and Design for Reliability", *ISQED*, pp: 212-128, 2006.

[19] A. Carlson, "Mechanism of Increase in SRAM VMIN Due to Negative-Bias Temperature Instability", *IEEE TDMR*, 2007.

[20] A. Bansal et al, "Impact of NBTI and PBTI on SRAM static/dynamic noise margins and cell failure probability", *JMR*, 2009.

[21] S. Khan, et al, "Impact of Partial Resistive Defects and Bias Temperature Defects and Bias Temperature Instability on SRAM Decoder Reliability", *Pro. of 7th IDT*, 2012.

[22] D. Rodopoulos, et al, "Atomistic Pseudo-Transient BTI Simulation with Inherent Workload Memory", *IEEE TDMR*, June 2014.

[23] S. Khan, et al, "Bias Temperature Instability Analysis of FinFET based SRAM cells", *DATE*, 2014.

[24] R. Menchaca et al, "Impact of Transistor Aging Effects on Sense Amplifier Reliability in Nano-Scale CMOS", *13th ISQED*, 2012.

[25] I. Agbo et al, "BTI Impact on SRAM Sense Amplifier", *8th IDT*, 16-18 Dec. 2013.

[26] H. Kukner et al, "Comparison of Reaction-Diffusion and Atomistic Trap-based Models for Logic Gates", *IEEE TDMR*, 2013.

[27] V. Chandra, R. Aitken, "Impact of Voltage Scaling on Nanoscale SRAM Reliability", *DATE*, 2009.

[28] S. Hamdioui, "Testing Static Random Access Memories: Defects, Fault Models and Test Patterns", *Kluwer Academic Press Publishers, The Netherlands*, 2004.

[29] H. Kukner et al, "BTI reliability from Planar to FinFET nodes: Will the next node be more or less reliable", *MEDIAN*, 2014.

[30] S. Cosemans, "Variability-aware design of low power SRAM memories", *Ph.D Thesis Katholieke Universiteit Leuven*, 2009.

[31] Predictive Technology Model "http://ptm.asu.edu/".