Alternative Architectures Toward Reliable Memristive Crossbar Memories

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***Abstract*— Resistive random access memory (ReRAM), referred to as memristor, is an emerging memory technology to potentially replace conventional memories, which will soon be facing serious design challenges related to continued scaling. Memristor-based crossbar architecture has been shown to be the best implementation for ReRAM. However, it faces a major challenge related to the sneak current (current sneak paths) flowing through unselected memory cells, which significantly reduces the voltage read margins. In this paper, five alternative architectures (topologies) are applied to minimize the impact of sneak current; the architectures are based on the introduction of insulating junctions within the crossbar. Simulations that were performed while considering different memory accessing aspects, such as bit reading versus word reading, stored data background distribution, crossbar dimensions, etc., showed that read margins can be increased significantly (up to 4×) as compared with standard crossbar architectures. In addition, the proposed architectures eliminate the requirement for extra select devices at each cross point and have no operational complexity overhead.**

***Index Terms*— Crossbar, current sneak paths, memory technologies, memristors, nanoelectronics, resistive random access memory (ReRAM).**

I. Introduction

NONVOLATILE resistive random access memory (ReRAM) is nowadays considered one of the promising alternatives to conventional memory technologies facing serious design challenges related to their continued scaling down [1]–[4]; ReRAMs provide many advantages such as scalability, energy efficiency, density, CMOS compatibility, and so on. Table I, taken from [5], illustrates a brief comparison between both conventional and emerging memories; it clearly shows that ReRAM with scalability down to sub-10 nm, comparable read/write times with today's memories and good retention time, is promising to advance the state of the art.

At the architectural level, crossbar memory cell array structure is considered one of the best ways to implement ReRAMs [6]. Crossbar architectures offer several benefits including pattern regularity, manufacturing flexibility, defect tolerance, CMOS compatibility, and the highest possible device density [7], [8]. Moreover, passive nanocrossbar arrays comprising bipolar switchable resistors at their junctions (hereinafter simply referred to as memristors [9]–[11]) have been proposed as convenient geometries to achieve higher density and performance [12]–[14]; they even provide the possibility of having multiple array layers stacked on top of each other to further augment density and bandwidth [15].

However, a typical passive crossbar memory, where no rectifying devices are used to isolate the cells being written or read [16], [17], suffers from a large amount of leakage current flowing through unselected cells called current sneak paths; this reduces both the size and the reliability (noise margin) of the device [18]–[20]. Many solutions have been proposed to overcome or diminish this drawback. They can be classified into three classes.

1) *Select devices*, which are separate devices, such as diodes or transistors, that are connected to the ReRAM cells [18], [21]–[23].
2) *Bias schemes*, where the voltages applied to nonaccessed word lines and bit lines are set to values different than those applied to accessed word lines and bit lines; examples are multistage reading [18] and using an ac signal instead of a dc signal for sensing the stored data in the desired cells [24].
3) *Switching device modifications*, where the resistive devices are modified; examples are serially connecting two memristive elements (bipolar switches) with opposite polarities, resulting into a complementary resis-

TABLE I
TRADITIONAL AND EMERGING MEMORY TECHNOLOGIES

	Current Baseline Technologies			Emerging Technologies		
	DRAM	**SRAM**	**Flash NAND**	**PCM**	**STT MRAM**	**Re RAM**
Feature Size	36-65 nm	45 nm	16 nm	45 nm	65 nm	5 nm
Cell Area	6-30 F^2	140 F^2	4 F^2	4 F^2	20 F^2	4 F^2
Read Time	2-10 ns	0.2 ns	0.1 ms	12 ns	35 ns	<10 ns
Write Time	2-10 ns	0.2 ns	0.1–1.0 ms	100 ns	35 ns	<1.0 ns
Retention	4-64 ms	N/A	10 years	> 10 years	> 10 years	> 10 years

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tive switch able to block the current at low voltage irrespective of the state of the devices [25]–[28], and the employment of a highly nonlinear memristor device (due to current-controlled negative differential resistance) to overcome sneak path [29].

Although the above mentioned solutions contribute to the reduction/removal of the current sneak paths, they also suffer from some limitations. For instance, using an *access* transistor or diode reduces the density; *bias schemes* and *device modifications* require complex reading schemes, thus impact both hardware area and performance.

This paper presents five alternative architectures for passive crossbar ReRAM as means to deal with the sneak path problem; it is built upon [30]. The architectures are based on the introduction of a certain percentage of insulating nodes spread out inside the array according to specific distribution patterns. The simulations were performed while considering different memory accessing aspects such as bit reading versus word reading, stored data background distribution, array dimensions, and so on. The simulation results showed that read voltage margins (hence reliability) can be increased significantly (up to 4×) as compared with standard crossbar architectures. Compared with the previous related work, our approach proves advantageous in terms of simplified fabrication processes of large memory arrays; it eliminates the requirement for extra select devices at each array cross point and has no operational complexity overhead.

The rest of this paper is organized as follows. Section II briefly presents memristive cross-point device modeling details, memristor-based crossbar memory, and highlights the serious negative impact of the current sneak paths. Section III presents the five alternative crossbar topologies to minimize the sneak path impact. Section IV provides a simulation-based validation of the proposed topologies. Section V discusses the obtained results and comments on the possibility to be used in 3-D ReRAM. Finally, Section VI concludes this paper.

II. Sneak Path Challenge in Memristive Crossbar-Based Memory

Memristive device modeling is a necessary step before the analysis of memristive crossbar-based memories. Therefore, this section starts with a brief description of the memristive cross-point device model before the crossbar-based memory architectures are presented. Thereafter, the impact of the sneak path on the read margin as function of the memory size is estimated. Finally, some simulation results are given for different cases to get more insight into the correlation between the read margins and the memory size.

A. Memristive Cross-Point Device Modeling

For our study, we use a memristor device model to represent the behavior of a memristive crossbar junction [31]. The equivalent circuit schematic of the device model is shown in Fig. 1(a) and consists of an ohmic resistor and a tunneling variable resistor coupled together. It generally concerns a threshold-type switching voltage-controlled memristor

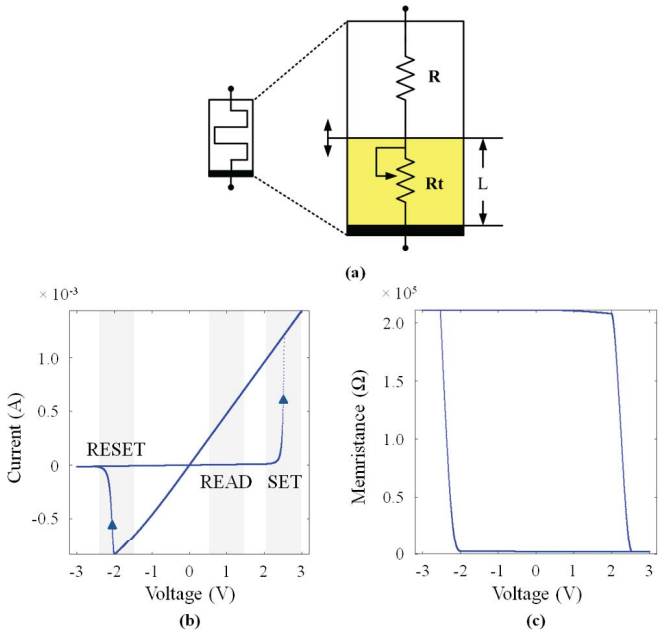

Fig. 1. (a) Equivalent circuit of the used memristor model [31]. (b) I–V and (c) R_t–V characteristics of a simulated memristor under triangular applied voltage.

whose behavior is described by the following nonlinear constitutive relation:

$$I_M(t) = G(L,t)V_M(t). \tag{1}$$

The model primarily attributes the resistance switching effect to an effective tunneling distance modulation. Parameter L is the state variable, which denotes the tunnel barrier width. G is the conductance of the device, whereas I_M and V_M represent the flowing current and the applied voltage, respectively. The equivalent circuit of Fig. 1(a) is inspired form the original circuit model proposed by Hewlett Packard (HP) for TiO_2-based devices [32]. R represents the resistance of the doped dioxide layer, and R_t represents the tunneling resistance of the undoped layer of the device. Since the doped layer acts as a conductor and the undoped layer is a pure insulator, there is a large difference between the actual values of their resistances, with $R_t \gg R$. This is why this model concentrates mainly on R_t, which is described by the equation

$$Rt(L_{V_M}) = f_0 \cdot \frac{e^{2L_{V_M}}}{L_{V_M}}. \tag{2}$$

Equation (2) contains a model-fitting constant parameter f_0 and generally gives the resistance (memristance) of the device for a certain value range of the state variable L. A heuristic equation that qualitatively gives the expected response of L as a function of the applied voltage V_M is given as follows:

$$L_{V_M} = L_0 \cdot \left(1 - \frac{m}{r_{V_M}}\right). \tag{3}$$

Parameter L_0 is the maximum value that L can attain. The term in the parenthesis of (3) contains a voltage-dependent parameter r and a fitting constant parameter m, which both determine the boundaries of the barrier width. Parameter r

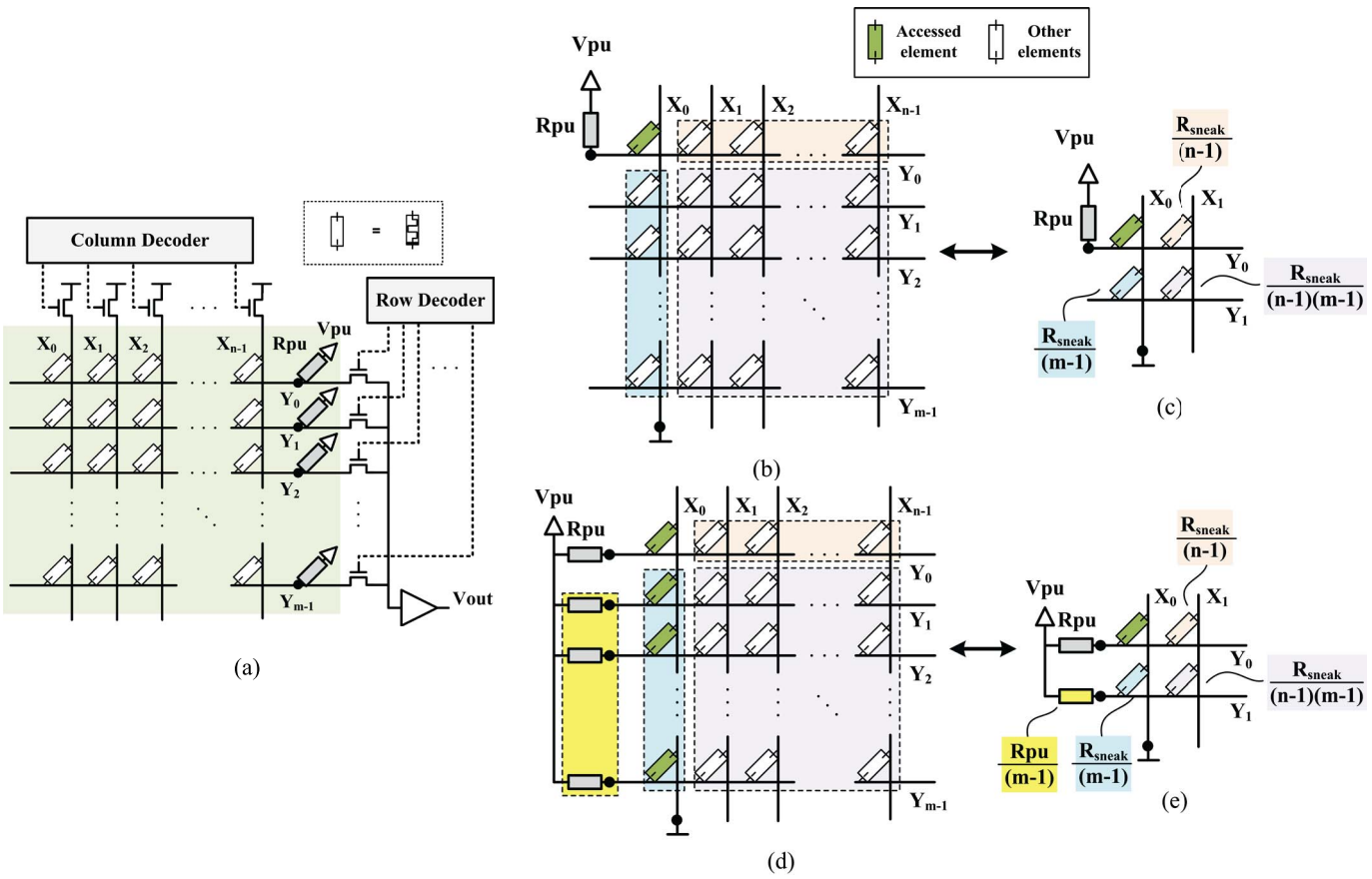

Fig. 2. (a) Basic setup of a nano/CMOS crossbar memory system. (b)–(e) Read operation setup and the equivalent circuit of a passive crossbar with one bit line/all bit lines pulled up, when all other cells are set to the same resistive state given as R_{sneak}.

also defines the current state of the device; its value is monitored and maintained within a valid range $r_{\text{MIN}} \leq r \leq r_{\text{MAX}}$. As a consequence, the memristance is correspondingly set to the most (R_{ON}) or the least (R_{OFF}) conductive state according to (2). Furthermore, the switching rate of L is small (fast) below (above) a threshold voltage (V_{SET} or V_{RESET}). This assumption is encapsulated in the time derivative of parameter r which is slow or fast depending on the applied voltage, as shown below:

$$\dot{r}_{V_M} = \begin{cases} a_{\text{RESET}} \cdot \dfrac{V_M + V_{\text{RESET}}}{c + |V_M + V_{\text{RESET}}|}, & V_M < V_{\text{RESET}} \\ b \cdot V_M, & V_{\text{RESET}} \leq V_M \leq V_{\text{SET}} \\ a_{\text{SET}} \cdot \dfrac{V_M - V_{\text{SET}}}{c + |V_M - V_{\text{SET}}|}, & V_M > V_{\text{SET}}. \end{cases} \tag{4}$$

Parameters a_{RESET}, a_{SET}, b, and c of (4) are fitting constants that are used to shape the intensity of the state variable dynamics. Throughout this paper, in all simulations, we set $\{a_x, b, c, m, f_0, L_0, r_{\text{MIN}}, r_{\text{MAX}}, V_{\text{SET}}, V_{\text{RESET}}\} = \{5 \times 10^3, 10, 0.1, 82, 310, 5, 100, 390, 2\text{ V}, -2\text{ V}\}$, and the resulting memristance range is $[R_{\text{ON}}, R_{\text{OFF}}] \approx [2, 200]$ KΩ. Such value set defines a memristor that switches steeply as soon as the applied voltage exceeds either of its thresholds. Fig. 1(b) and (c) shows the simulation results for a memristor under triangular applied voltage. Current is piecewise linear with the applied voltage, i.e., the memristor has linear ON and OFF states [27], [33].

B. Memristive Crossbar-Based Memory

The crossbar geometry is one of the most common and most mature architectures toward high-density nanoelectronics. Passive crossbar-based memristive memory systems use memristors with nonlinear I–V characteristics as cross-point elements. They do not rely on any kinds of devices (diodes or transistors) that are normally used to isolate the cell being accessed in conventional memories. Fig. 2(a) shows the basic setup of nano/CMOS crossbar memory architecture; here, a crossbar setup with n word lines and m bit lines is assumed. Column and row decoders drive the necessary selection switches to form a voltage divider circuit with the corresponding pull-up (sense) resistor and the resistance of the accessed node. Typically, the pull-up resistors are implemented in a CMOS layer or in a form of nanowire resistors [34]. The output of the voltage divider is then driven to a CMOS sense amplifier, and the state of the device is distinguished by comparing this voltage with a reference value. The simplest circuit approach for reading information from the memristor-based crossbar is by applying a certain read voltage across a junction and transforming the current flow into a voltage.

C. Estimation of Read Margins

To perform correct read operations, the voltage swing at the output of the crossbar read circuit [between reading a high-impedance state (R_{OFF}) and a low-impedance state (R_{ON})] should be large enough to distinguish the two states.

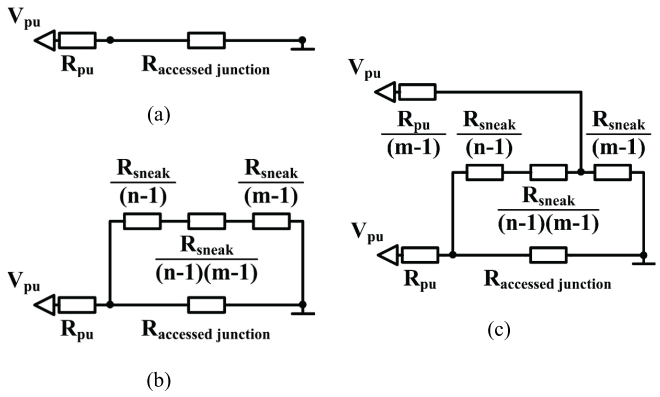

Fig. 3. Read operation equivalent circuits in passive crossbar [27], [28]. (a) Ideal reading case for a single accessed memristor. More realistic case with the inevitable parasitic resistance when accessing (b) single memristor, or (c) entire word line of memristors.

Two different approaches can be used to access the crossbar memory: 1) single cell: select one word line, pull up one bit line, and leave the other bit lines floating or 2) entire word: select one word line and pull up all bit lines simultaneously [4]. The circuit setup corresponding to the read operation of a single cell and an entire word line is shown in Fig. 2(b) and (d), respectively. Based on the equivalent circuits shown in Fig. 2(c) and (e), the respective parasitic worst case resistance can be computed.

In the ideal reading case, where no current sneak paths are present, the equivalent circuit for the read operation is a simple voltage divider formed by a pull-up resistor $R_{\rm PU}$ and the accessed memristor, as shown in Fig. 3(a). For a given $R_{\rm OFF}/R_{\rm ON}$ ratio, the achieved voltage swing ΔV for a certain applied pull-up voltage $V_{\rm PU}$ is calculated as follows:

$$\frac{\Delta V}{V_{\rm PU}} = \frac{V_{\rm OFF} - V_{\rm ON}}{V_{\rm PU}} = \frac{R_{\rm OFF}}{R_{\rm OFF} + R_{\rm PU}} - \frac{R_{\rm ON}}{R_{\rm ON} + R_{\rm PU}}. \quad (5)$$

This normalized detection margin of the two possible states of a memory cell is maximized if the pull-up resistor $R_{\rm PU}$ is optimally chosen to be the geometric mean of the two bistable resistances of the memristors [4]. However, for large $R_{\rm OFF}/R_{\rm ON}$ ratios, the optimal $R_{\rm PU}$ is close to $R_{\rm ON}$. In reality, when a read operation is performed in the presence of parasitic current paths parallel to the accessed memristor, the effective $R_{\rm OFF}/R_{\rm ON}$ ratio substantially reduces.

Fig. 3(b) and (c) show the equivalent circuits for the read operation of a single cell and an entire word line, respectively, in the presence of parasitic resistance; different accessing approaches result in different parasitic resistances. The worst case reading scenario in case the accessed memristor is in $R_{\rm OFF}$ ($R_{\rm ON}$) occurs when the parasitic resistance is as small (high) as possible. This is when all nonaccessed memristors ($R_{\rm sneak}$) are set to $R_{\rm ON}$ ($R_{\rm OFF}$). According to Fig. 3(b), the parasitic worst case resistance is given by the following:

$$R_{P,{\rm OFF(ON)}} = \frac{R_{\rm ON(OFF)}}{(m-1)} + \frac{R_{\rm ON(OFF)}}{(n-1)} + \frac{R_{\rm ON(OFF)}}{(m-1)(n-1)} = R_{\rm ON(OFF)} \frac{m+n-1}{(m-1)(n-1)}. \quad (6)$$

This resistance is found in parallel with the accessed memristance, and as a result, the maximum achievable read voltage margin gets significantly smaller with increasing crossbar size. Similarly, when having all bit lines pulled up, the parasitic worst case resistance for any of the accessed elements (of the same word-line) can be computed based on the equivalent circuit shown in Fig. 3(c). Following a similar modeling approach to that of [28], after applying typical $Y-\Delta$ transform, it is found that the equivalent read circuit corresponds to a voltage divider between the *effective* pull-up resistance given by

$$R_{\rm PU,eff} = \frac{R_{\rm sneak\_b} \cdot R_{\rm PU}}{R_{\rm sneak\_b} + R_{\rm PU}} \quad (7)$$

and the effective *sensed* memristance for either stored binary values, given by the following:

$$R_{\rm OFF(ON),sensed} = \frac{R_{\rm sneak\_a} \cdot R_{\rm OFF(ON)}}{R_{\rm sneak\_a} + R_{\rm OFF(ON)}} \quad (8)$$

where the auxiliary variables $R_{\rm sneak\_a}$ and $R_{\rm sneak\_b}$ are calculated as follows:

$$R_{\rm sneak\_a} = \frac{\left(\frac{R_{\rm ON}}{n-1} + \frac{R_{\rm ON}}{(n-1)(m-1)}\right) \cdot \frac{R_{\rm ON}}{m-1} + \frac{R_{\rm PU}}{m-1} \cdot \frac{R_{\rm ON}}{m-1}}{\left(\frac{R_{\rm PU}}{m-1}\right)} + \frac{\left(\frac{R_{\rm ON}}{n-1} + \frac{R_{\rm ON}}{(n-1)(m-1)}\right) \cdot \frac{R_{\rm PU}}{m-1}}{\left(\frac{R_{\rm PU}}{m-1}\right)} \quad (9)$$

$$R_{\rm sneak\_b} = \frac{\left(\frac{R_{\rm ON}}{n-1} + \frac{R_{\rm ON}}{(n-1)(m-1)}\right) \cdot \frac{R_{\rm ON}}{m-1} + \frac{R_{\rm PU}}{m-1} \cdot \frac{R_{\rm ON}}{m-1}}{\left(\frac{R_{\rm ON}}{m-1}\right)} + \frac{\left(\frac{R_{\rm ON}}{n-1} + \frac{R_{\rm ON}}{(n-1)(m-1)}\right) \cdot \frac{R_{\rm PU}}{m-1}}{\left(\frac{R_{\rm ON}}{m-1}\right)}. \quad (10)$$

Finally, the measurable normalized read voltage margin in this case is

$$\frac{\Delta V}{V_{\rm PU}} = \frac{R_{\rm OFF,sensed}}{R_{\rm OFF,sensed} + R_{\rm PU,eff}} - \frac{R_{\rm ON,sensed}}{R_{\rm ON,sensed} + R_{\rm PU,eff}}. \quad (11)$$

D. Sneak Path Negative Impact on Readout Performance

For evaluation and comparison purposes, readout performances of several sets of crossbar memory designs are compared in this section. Simulations are based on the memristor device model presented in Section II-A [31]. The applied readout voltage $V_{\rm PU}$ is selected equal to 1 V so as to be below the device switching thresholds, as shown in Fig. 1(b). Nodal analysis is performed, and all differential equations are numerically solved using a fourth-order Runge–Kutta integration method, as it is implemented in [35]. It is assumed that all memristors inside the crossbar are identical with equal

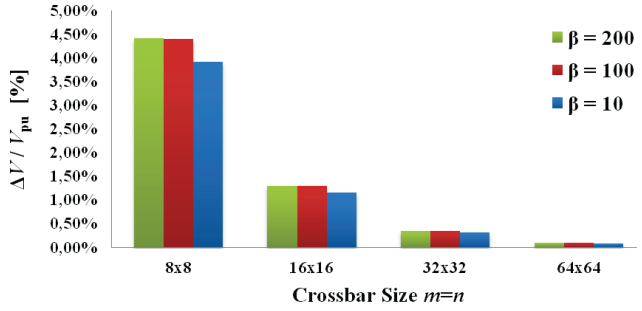

Fig. 4. Normalized read voltage margin $\Delta V/V_{\mathrm{PU}}$ versus size of an $n \times m$ memristor-based quadratic crossbar array ($n = m$) with a stored worst case pattern for different resistance ratios $\beta = R_{\mathrm{OFF}}/R_{\mathrm{ON}}$ and assumed $R_{\mathrm{PU}} = R_{\mathrm{ON}}$.

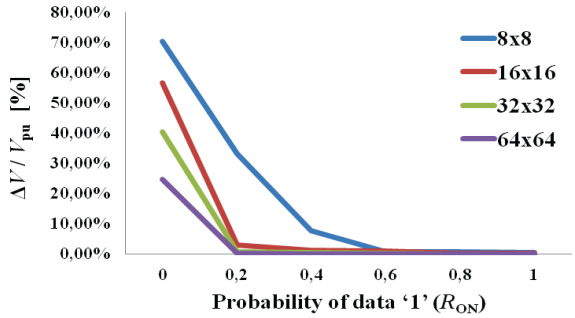

Fig. 5. Dependence of measured voltage margins on the data distribution in the crossbar grid. In the presented simulation results, it is assumed that $\beta = R_{\mathrm{OFF}}/R_{\mathrm{ON}} = 200$ and $R_{\mathrm{PU}} = R_{\mathrm{OPTIMUM}}$ for each array size.

resistance ratio $\beta = R_{\mathrm{OFF}}/R_{\mathrm{ON}}$ of two orders of magnitude. The resistance of interconnects, sensing elements, and voltage source/s is not taken into consideration for two reasons: 1) to reduce the total system's complexity and minimize simulation run time and 2) because our intension is to perform qualitative analysis and check the trends. For all design sets, the detection margins are normalized with respect to V_{PU} since their values will be always proportional to V_{PU}.

Fig. 4 shows the simulation results for a floating memristor array considering different sizes and different ratios β when accessing the leftmost cell of the first row; we choose this particular cell to perform our study following the fundamental analysis in [4]. The maximum achievable read voltage margin gets significantly smaller with increasing array size. Evidently, the noise margins almost vanish quickly as the array size gets larger, regardless of β. The effect of β is more intense when pull-up resistors of optimum values are used. However, the measured voltages strongly depend on the distribution of the stored information in the memory. The simulation results in Fig. 5 indicate how the normalized voltage margins decay fast with an increased probability of low-resistive junctions when $\beta = 200$.

Furthermore, we investigate the effect of random data distribution patterns on the measured voltages when reading entire word lines (array columns). Fig. 6 shows the simulation results for a read operation from a column located close to the middle of the grid, both for 32×32 and 64×64 array sizes. In each case, the minimum and maximum values from

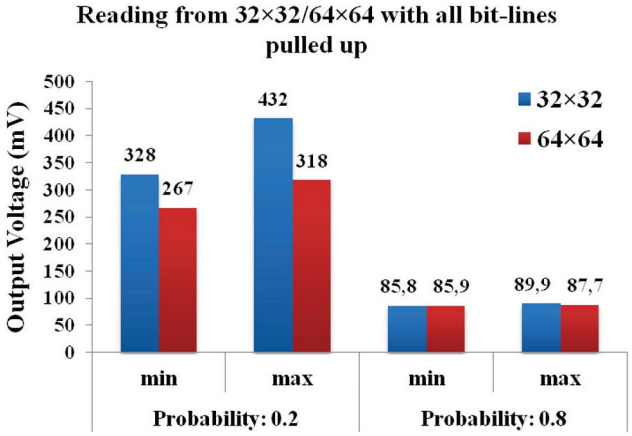

Fig. 6. Simulation results for a word-line read operation from 32×32 and 64×64 crossbar arrays considering 20% and 80% probability for the low-resistive nodes across the grid with $\beta = 200$ and $R_{\mathrm{PU}} = R_{\mathrm{OPTIMUM}}$.

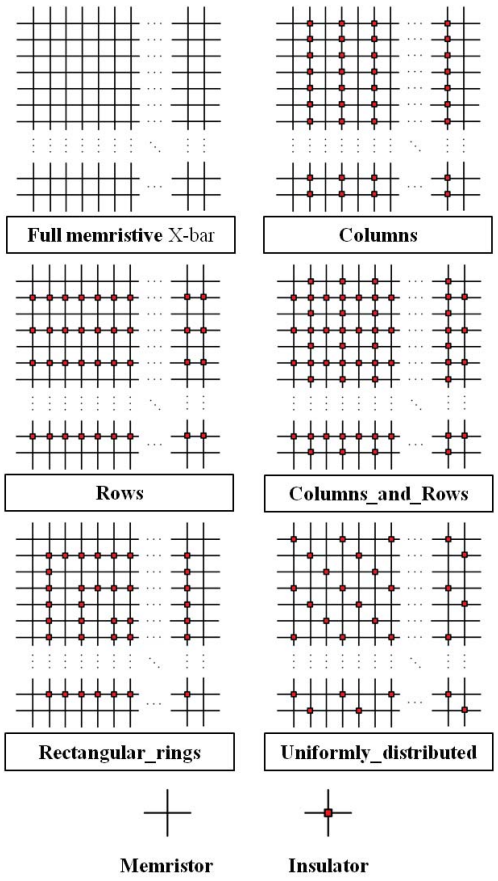

Fig. 7. Alternative crossbar architectures (topologies) compared with the full memristive crossbar (X-bar). Red dots denote insulating cross points, whereas simple wire crossings denote memristive memory cells.

the measured voltages across the selected word line are given. The larger the number of low-resistive nodes, the higher the impact on the read voltage margins regardless of the array size. We also observe that as the probability of the low-resistive nodes approaches 100%, when moving from smaller to larger arrays, the minimum output voltages almost remain unaffected, whereas the maximum measured voltages continue to decay, thus shortening the resulting ΔV.

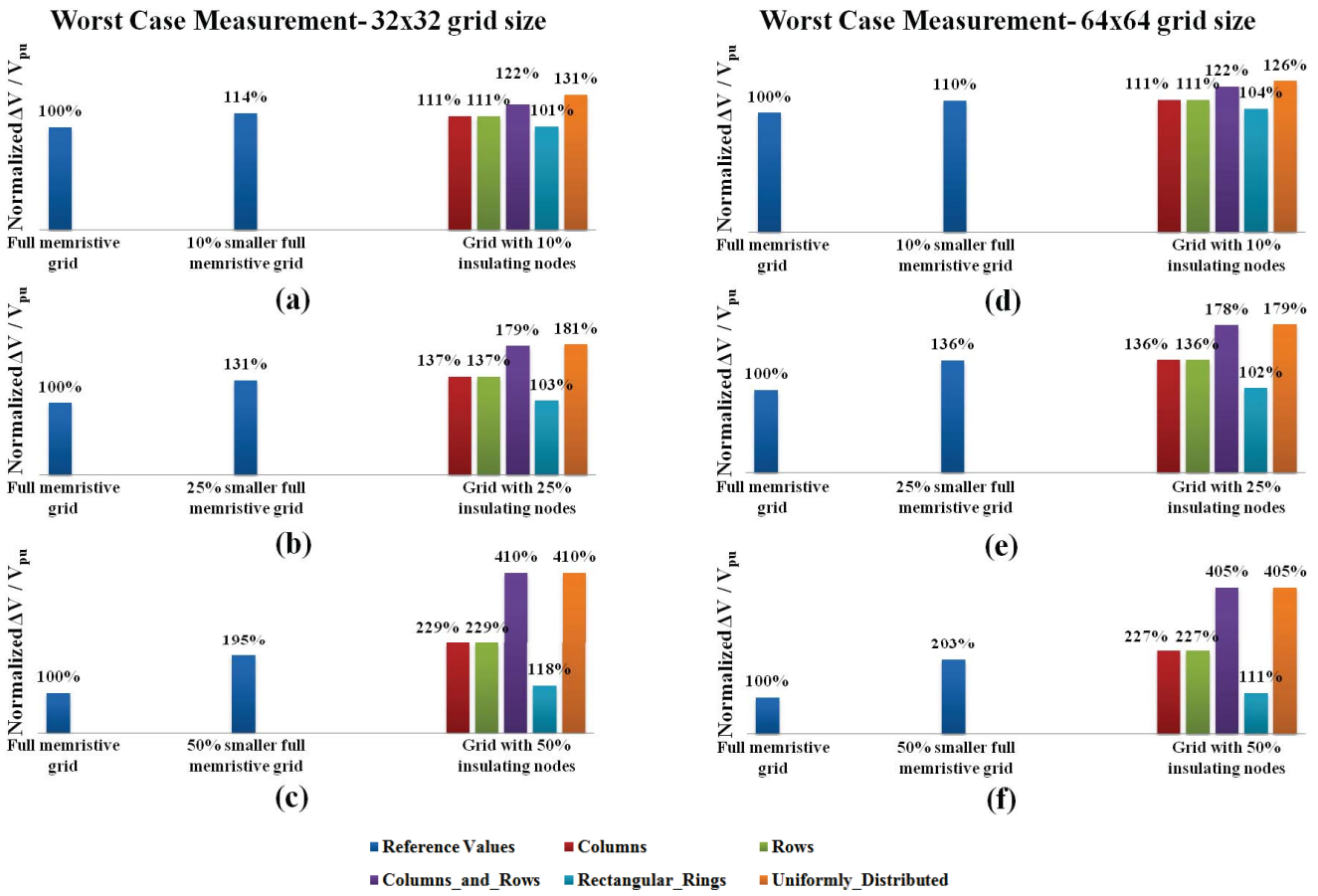

Fig. 8. Normalized read voltage margin $\Delta V/V_{PU}$ for the worst case reading scenario in (a)–(c) 32 × 32 and (d)–(f) 64 × 64 grids. The measured margins are normalized to the voltage ratio of the full memristive grid. The achieved margins of the applied patterns are also compared with the margins measured in smaller full memristive grids, which comprise a number of nodes equal to the remaining nodes of the original grid if we omit the insulators. The performance of the patterns with 10%, 25%, and 50% insulators is compared with the corresponding performance of memristive grids with 10%, 25%, or 50% less nodes. The five patterns are designated with red (columns), green (rows), purple (columns and rows), cyan (rectangular rings), and orange (uniformly distributed).

All of the provided simulation results underline that innovative techniques, which will provide us with the opportunity to enlarge importantly the measured voltage margins, thus resulting in more effective readout memory operations, constitute a key factor toward the practical realization of passive crossbar memory systems.

III. Alternative Crossbar Topologies

This section discusses alternative topologies for passive crossbar ReRAM as means to deal with the sneak-path problem [30]. In alternative topologies, a certain percentage of insulating nodes spread out inside the array according to specific distribution patterns. The motivation is to restrain current sneak paths and, thus, improve the voltage margins by replacing some memory cells. Such a practice is considered a viable solution given the huge device density that the crossbar geometry offers compared with other circuit architectures. Fig. 7 shows five alternative topological patterns together with the full memristive crossbar (denoted as X-bar).

1) *Column Pattern:* The insulating junctions are located in columns that are uniformly distributed across the array.
2) *Row Pattern:* Here the insulating junctions are placed in uniformly distributed rows.
3) *Column and Row Pattern:* This combines the previous two mentioned patterns.
4) *Rectangular Ring Pattern:* The inserted insulating nodes are placed in rectangular rings that are distributed across the grid starting from the central rectangle, which is formed by the four innermost nodes.
5) *Uniformly Distributed Pattern:* The insulating nodes are uniformly distributed both horizontally and vertically inside the grid. For each insulator, the closest neighboring insulating nodes are always found at equal horizontal and vertical distances.

Each of the above patterns aims to uniformly cover as much as possible the entire grid area; the grid is considered a torus to facilitate the distribution.

IV. Evaluation of Alternative Topologies

To investigate the impact of such topologies, several simulations were performed for different grid sizes and by considering different populations for the total introduced insulators. Simulation of the new architectures was based on the memristor model, which was summarized in Section II-A, where

$\beta = 200$ and the sense resistor R_{PU} was set to the optimum value to yield the highest possible output signal-to-noise ratio. The presented patterns were tested for both 32×32 and 64×64 arrays, and their performance was compared with that of the full memristive crossbar, while considering three different distributions characterizing the total number of insulators in the grid; these are 10%, 25%, or 50% of the total number of nodes. Once all the data were programmed in the array, the read operation was always performed by applying a 1 V readout voltage pulse V_{PU} across the target cross-point cells, as explained above. Then, the resulting voltage margin was calculated.

A. Reading One Memory Cell: Worst Case Scenario

Fig. 8 shows the read voltage margin for the worst case reading scenario; in each subfigure, the voltage margin ($\Delta V/V_{PU}$) is normalized to the reference value, which is always the performance of the full memristive crossbar (i.e., the array with 100% memristive nodes). In addition, the voltage margins of smaller arrays, resulting by removing the insulating junctions from the simulated grid, are also included; for example, Fig. 8(a) shows that the read voltage of the simulated initial full memristive 32×32 grid is improved by 14% when its size is reduced by 10%. However, maintaining the same grid size while replacing 10% of the nodes with insulators increases the voltage margin up to 31% depending on the architecture. All architectures yield improved voltage margin, which is never equal to the margin corresponding to the smaller memristive grid that comprises the same total number of memory cells. Depending on the applied architecture, on the percentage of insulating nodes, as well as on the percentage of low-resistive cross-point cells, the exact values of the improved read margins for the examined array-sizes fall within the range 2–440 mV. Overall, inspecting Fig. 8 reveals the following.

1) All of the five architectures improve the read margins, although the strength of the improvement is strongly architecture dependent. The improvement trends for the architectures are the same irrespective of the simulated grid sizes and the considered percentages of inserted insulators.
2) Column and row pattern-based architectures result in similar improvements for all simulated cases. Combining these two patterns results in a better improvement; the higher the percentage of inserted insulators, the higher the improvement. However, this improvement difference seems to be grid-size independent.
3) Rectangular ring-based architecture performs the worst, while the uniformly distributed-based architecture scores the best, irrespective of the simulated case. This can be easily explained. Having insulators is essentially like having R_{OFF} cells (with larger R_{OFF} though); hence, the more uniformly distributed these are, the less the sneak current, which in turn results in better read margins.

Moreover, we tested the performance trend of the alternative architecture which yielded better results in bit-reading mode also in large crossbar arrays with up to 2048×2048 elements.

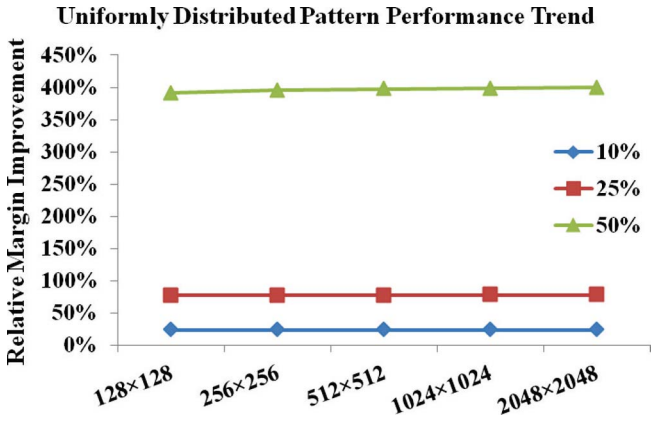

Fig. 9. Relative read margin improvement trend for the pattern with the best performance in bit-reading mode considering 10%, 25%, and 50% insulators.

The relative readout margin improvement is shown in Fig. 9. Apparently, the uniformly distributed pattern holds its relative performance regardless of the array size; this confirms our initial observation about the overall patterns' performance.

In addition to the above analysis, we studied the sneak current distribution during random read operations performed to a 32×32 array whose nodes were all found at the low-resistive state except the node being accessed; a total of 2000 read operations were performed. Each time we measured the sneak current at all nonaccessed nodes. The total accumulated currents were finally computed and normalized to the maximum noticed value. Fig. 10(a) shows the normalized sneak current distribution, whereas Fig. 10(b) shows the readout event distribution in the array. It can be observed that the majority of the sneak current is uniformly distributed in the grid (nodes marked with purple color). Consequently, the architectures that spread as much as possible the insulating nodes rightfully more effectively suppress the sneak currents.

B. Reading Entire Word Lines: Random Stored Data Distribution

To evaluate the performance of the five architectures when reading the entire word line, 30 read accesses were performed, each with 30 different (random) memory initializations resulting in 900 memory accesses. For each memory initialization, the maximum and the minimum of the read voltage difference between: 1) the read voltage of R_{OFF}-read operation (V_{OFF}) and 2) the read voltage of R_{ON}-read operation (V_{ON}) were calculated as follows:

$$\Delta V_{MIN} = V_{OFF,MIN} - V_{ON,MAX}$$
$$\Delta V_{MAX} = V_{OFF,MAX} - V_{ON,MIN}.$$

Thereafter, the average of the 30 values of ΔV_{MIN} and ΔV_{MAX} was determined. While accessing the memory, the insulating junctions of the targeted word line were always omitted; read operation was instead performed to an adjacent word line whenever necessary to broaden the sample of measurements.

Figs. 11 and 12 show the simulation results for 32×32 and 64×64 memory arrays, respectively; the change of the voltage margin is normalized to the reference value, which represents

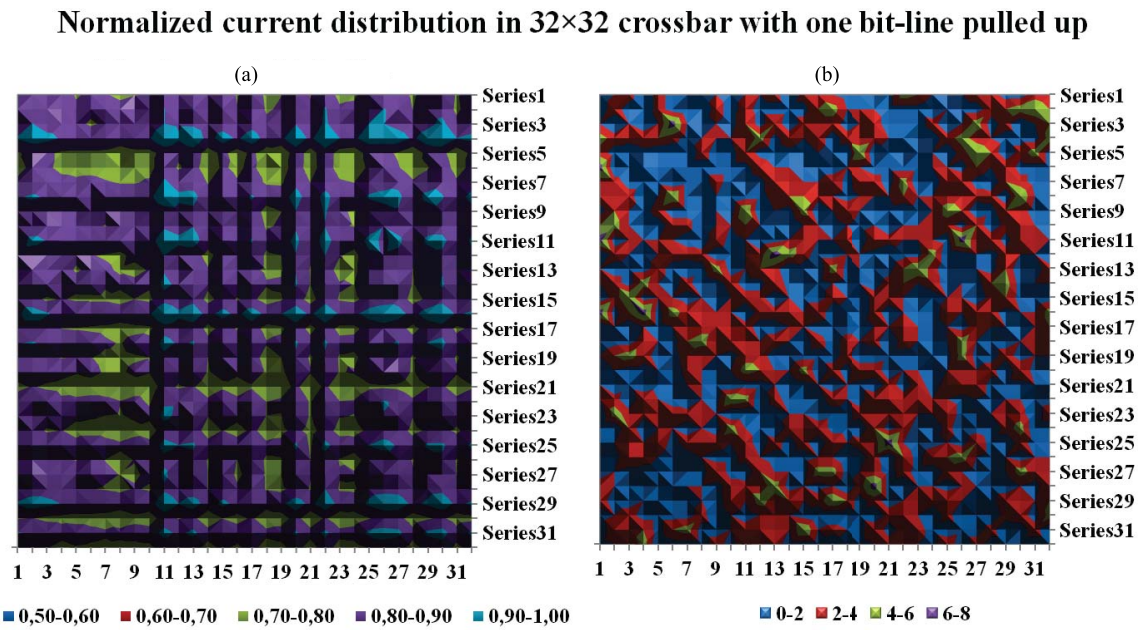

Fig. 10. Simulation results for the sneak-current distribution analysis of the worst case scenario when accessing 1 bit per memory operation in a crossbar with all of its nodes initialized at R_{ON} except for the node being accessed. (a) Accumulated sneak current at each node normalized to the maximum measured value. The five distribution classes are given in blue (0.5–0.6), red (0.6–0.7), green (0.7–0.8), purple (0.8–0.9), and cyan (0.9–1.0) colors, respectively. (b) Distribution of the readout events in the grid, which were randomly performed based on the uniform distribution. The four distribution classes are given in blue (0–2), red (2–4), green (4–6), and purple (6–8) colors, respectively. To maximize the output, we assume $R_{\mathrm{PU}} = R_{\mathrm{OPTIMUM}}$ and set $\beta = 200$.

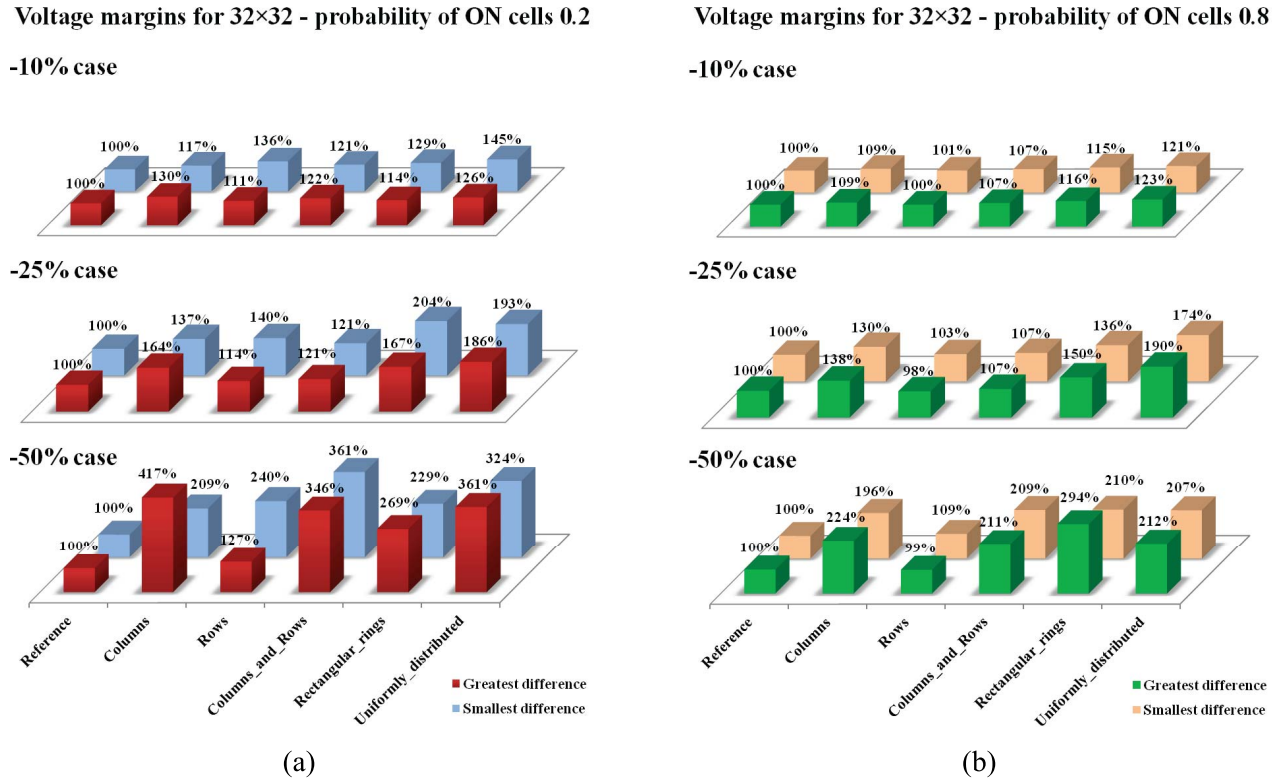

Fig. 11. 32×32 grid size: evaluation of the average patterns' performance on the greatest and smallest measured ΔV over a series of 30 different read operations. The considered probabilities for the stored low-resistive states across the grid are (a) 20% and (b) 80%, respectively. To maximize the output voltages, we again assume $R_{\mathrm{PU}} = R_{\mathrm{OPTIMUM}}$ and set $\beta = 200$.

the case where no insulating junctions are inserted in the array. Overall, we observe the following.

1) All of the five architectures improve the read margins irrespective of the array size and the occurrence probability of low-resistance nodes in the array, except for the row-based architecture in some cases, i.e., when the occurrence probability of low-resistance nodes is 80% and the percentage of inserted insulators in the grid is 25% or 50%. However, such results are attributed to the sample of measurements because for high percentage

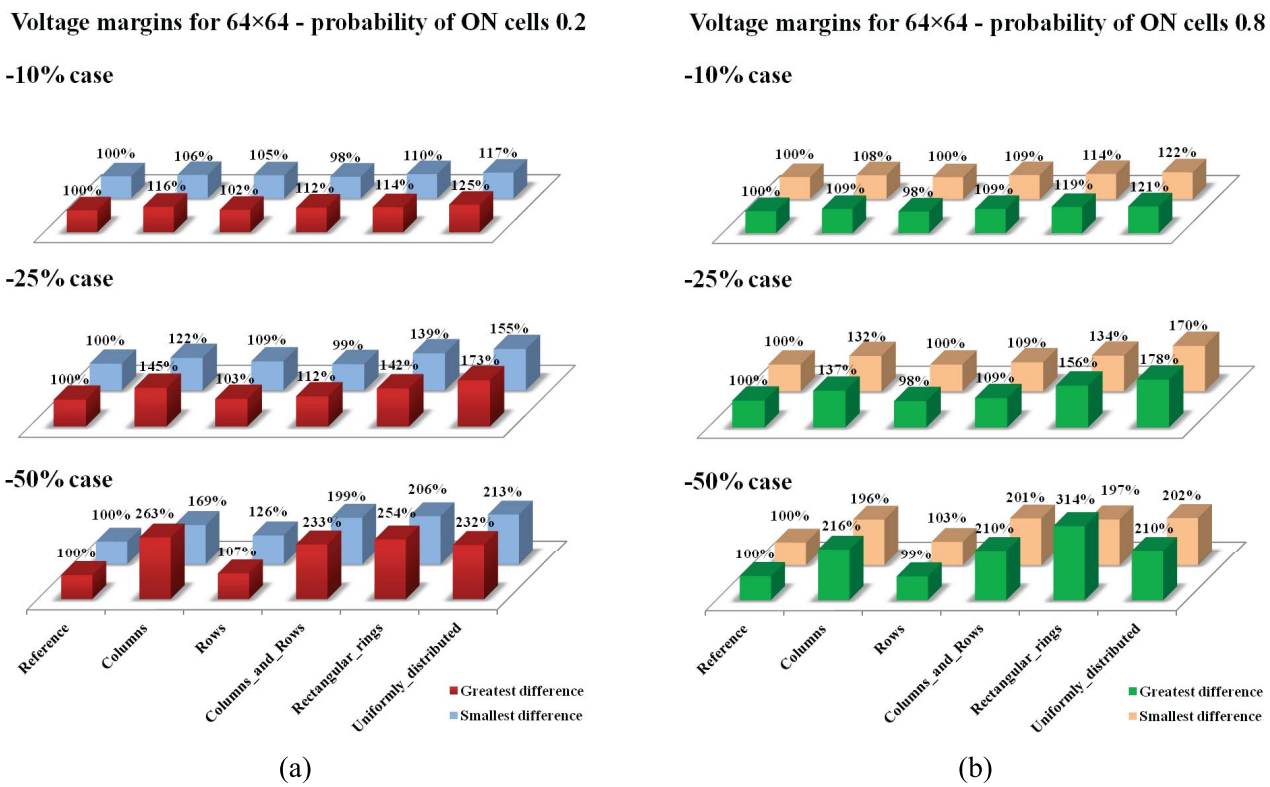

Fig. 12. 64×64 grid size: evaluation of the average patterns' performance on the greatest and smallest measured ΔV over a series of 30 different reading operations. The considered probabilities for the stored low-resistive states across the grid are (a) 20% and (b) 80%, respectively. To maximize the output voltages, we again assume $R_{\text{PU}} = R_{\text{OPTIMUM}}$ and set $\beta = 200$.

of inserted insulators, there were only few remaining memristive nodes to read.

2) The strength of the improvement is not only strongly architecture dependent but also strongly dependent on the metrics (greatest versus smallest) and the percentage of inserted insulators. However, the dependence on the array size seems very marginal.
3) The worst architecture when considering ΔV_{MAX} metric (greatest difference) is the row-based for all simulated cases. However, when considering ΔV_{MIN} metric (smallest difference), it becomes case dependent; it is the row-based architecture for large occurrence probability of low-resistance nodes and can be row- or combined row–column-based architecture for low occurrence probability of low-resistance nodes.
4) The best architecture is uniform-based for most of the simulated cases. However, in some cases, column- and rectangular ring-based architectures perform (slightly) better.

In addition, we performed similar experiments as in the previous section to analyze the sneak current distribution during random read operations. Fig. 13 shows the simulation results; the most congested nodes of the grid are found along specific rows located close to the center and the borders of the array. Such distribution is more evident when the probability of the low-resistance nodes increases [Fig. 13(b)]. Therefore, the architectures that position the insulators along the columns of the array are more likely to replace critical (congested) nodes and, consequently, contribute more to the lowering of sneak currents. This is very much in line with the simulation results shown in Figs. 11 and 12, which clearly show that the column-based architecture overall performs very well.

V. Discussion

Although some assumptions were made to facilitate and accelerate the simulation (e.g., neglecting the resistance of interconnects), the results clearly show that considering the injection of insulator patterns in the crossbar is a valid and interesting approach to be considered for reducing the impact of the sneak path problem. This comes at the price of additional area overhead. However, given the fact that: 1) crossbar architecture typically will target huge data storage; 2) nanodevices integrated in the crossbar are extremely small (size $4F^2$, where the feature size $F < 10$ nm [5]); and 3) the regularity of the structure (easy to manufacture), it is very justifiable to trade additional array area for better reliability and robustness; keep in mind that the proposed approach eliminates the requirement for select devices at each cross point as well. It is worth noting that reliability is one of the major bottlenecks that technology scaling is facing, leading to lower yield, thus preventing cost per die from further scaling.

The provided simulation results indicate that the choice of the best architecture will strongly depend on the memory size, the memory addressing mode, and the impact of the access circuitry (decoders, sense amplifiers, etc.). However, obviously the architectures that spread the insulating nodes uniformly across the array perform steadily well and can yield good improvements for either bit- or word-reading modes.

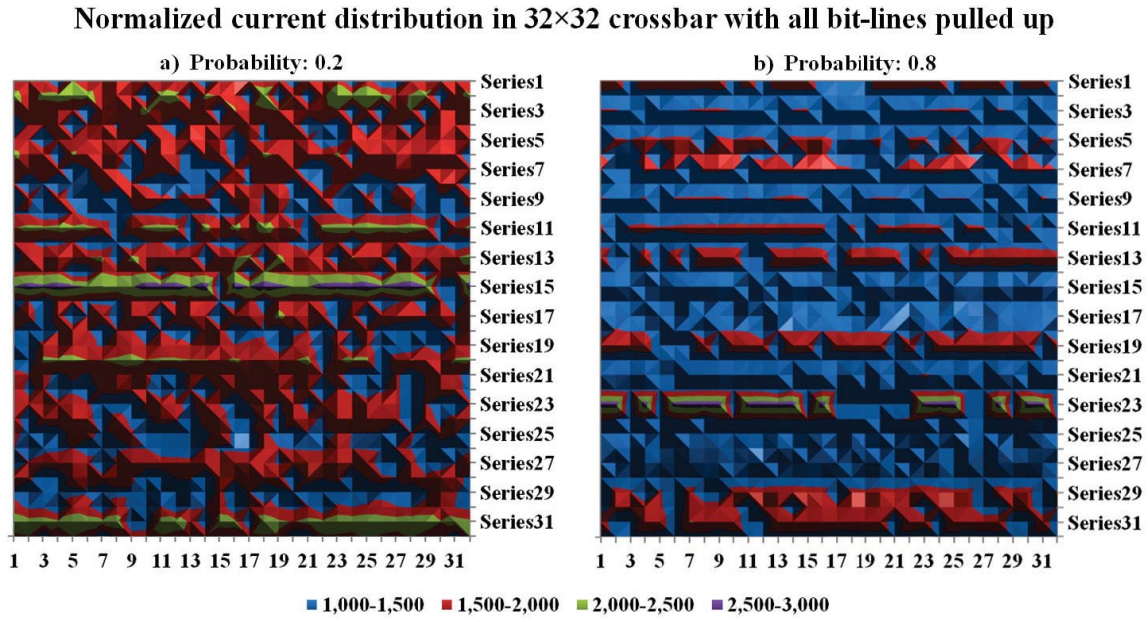

Fig. 13. Simulation results of the sneak-current distribution analysis when accessing one word line per memory operation on a 32×32 crossbar initialized randomly with (a) 20% or (b) 80% of its nodes at R_{ON}. After initialization, we read all columns and calculate the mean value of the amount of parasitic current corresponding to each node. (a) Accumulated sneak current at each node normalized to the minimum mean value when taking into consideration only the nodes found at R_{OFF}. (b) Mean values are normalized to the minimum mean value when taking into consideration only the nodes found at R_{ON}. The four distribution classes are given in blue (1.0–1.5), red (1.5–2.0), green (2.0–2.5), and purple (2.5–3.0) colors, respectively. To maximize the output voltages, we again assume $R_{\mathrm{PU}} = R_{\mathrm{OPTIMUM}}$ and set $\beta = 200$.

Moreover, it is worth noting that the proposed architectures could be useful in large hierarchical memory organizations where a memory lattice is divided into a number of smaller sized subarrays to maintain sufficient voltage margins; the necessary subarrays will be less in number and larger in size, thus reducing the overhead of extra peripheral circuits.

As already explained, the provided architectures require the injection of insulator patterns in the crossbar. From the manufacturing point of view, this will require additional steps in the fabrication process and modification of the masks. Nevertheless, the regularity of the insulator patterns will make it easier to be integrated both in the masks and in the fabrication process; moreover, this will make it impression resistant.

As mentioned before, the current mainstream in nonvolatile memories is flash memory. 2-D NAND-type flash has already scaled to 16-nm node, whereas scaling to near 10 nm seems possible [5]. Further density scaling, though, may require a different memory technology and/or a 3-D architecture, and 3-D NAND flash is currently being developed [36]. Current projections for the achievable packing density (bits/cm^2) of ReRAM remain substantially lower than those for 3-D NAND flash, unless 3-D ReRAM is fabricated [37]. However, compact bipolar cell selection devices with scalability below 10 nm, high ON/OFF ratio, and high endurance are highly required to cut off the leakage paths in the z-plane of 3-D ReRAM. Indeed, the higher the number and the size of the stacked 2-D layers, the higher ON/OFF ratio is needed. Even though the presented architectures were not tested for multiple stacked 2-D arrays, they are expected to somehow relax the aforementioned tight requirements for the 3-D selection devices by mitigating the leakage paths at each 2-D stacked layer separately.

VI. Conclusion

In this paper, the concept of using insulator patterns in crossbar architecture to solve the sneak path problem is proposed. A set of five architectures was developed and simulated. The results reveal that significant improvements of the sensed voltages can be realized, irrespective of the array size. Sneak-current distribution analysis was performed to verify the overall performance of the alternative architectures while considering bit-/word-reading approaches and different stored data backgrounds. The proposed architectures simplify the array fabrication process since they eliminate the requirement for select devices at each cross point; hence, they are well suited for future data storage applications. Circuit-level simulations of large-scale arrays based on new models that consider resistive and capacitive loads of word/bit lines, thus unmasking their impact on read/write operation and power dissipation, will be part of our future work.

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