Comparative BTI Impact for SRAM Cell and Sense Amplifier Designs

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***Abstract*—Bias Temperature Instability (BTI) in transistors has become a major reliability challenge with the continuous downscaling of CMOS technologies. This paper presents the impact of BTI on SRAM cells and sense amplifiers (SA) while considering both high performance (HP) and low power (LP) designs in 45nm technology node. The results show that the HP designs degrades more than $2\times$ faster than LP designs. Moreover, in terms of absolute numbers, the HP SA seems to be the design with maximum degradation and LP SRAM cell with marginal degradation.**

***Index Terms*—BTI, NBTI, PBTI, SRAM sense amplifier**

I. Introduction

In recent decades, CMOS technology has been sustained with aggressive downscaling that severely impacts the reliability of devices [1–3]. These trends are a consequence of advancements in the fabrication technology, introduction of novel materials and evolution of architecture designs. Bias Temperature Instability (BTI) (i.e., Negative BTI in PMOS transistors and Positive BTI in NMOS transistors) is a reliability failure mechanism which affects the performance of MOS transistors by increasing their threshold voltage and reducing their drain current (I_d) over the operational lifetime [4,5]. However, studies of such individual devices or small composites do not allow extrapolation of these effects on larger circuits like SRAMs.

Static Random-Access Memories (SRAM) occupy a large fraction of semiconductor chip and play a major role in the silicon area, performance, and critical robustness [6]. An SRAM system consists of an array of cells, its peripherals circuits such as row and column address decoders, control circuits, write drivers, and sense amplifiers.

Many publications analyzed the BTI impact on SRAM cell array and few on the peripheral circuitry, while very limited work is published on the relative analysis between the SRAM cell and sense amplifier designs. For instance, Binjie *et al.* [7] investigated NBTI impact on Static Noise Margin (SNM) and Write Noise Margin (WNM) degradation of 6T SRAM cell. Kumar *et al.* [8] Analyzed the impact of NBTI on the read stability and SNM of SRAM cells. On the other hand, few authors have focused on reliability analysis of the SRAM peripheral circuit. Khan *et al* [9] anlyzed the impact of partial resistive defects and bias temperature instability on SRAM decoder reliability. Agbo *et al.* [10] investigated BTI impact on SRAM drain-input latch type sense amplifier design implemented on 90nm, 65nm, and 45nm for different supply voltages by using sensing delay and voltage metrics. Agbo *et al.* [11] investigated the integral impact of BTI and voltage temperature variation on SRAM sense amplifier using sensing delay as reliability metric. Agbo *et al.* [12] explored the BTI analysis for high performance and low power SRAM sense amplifier designs using sensing delay and dynamic energy as reliability metrics without taking the cell into account. In the past, BTI analysis was only on SA designs and not mutual comparative study of the memory sub-circuits (i.e., cell and SA, etc.). However, comparative analysis of BTI impact of different memory sub-circuits (including 6T SRAM cell and sense amplifiers) while considering HP and LP designs for worst-case workload is still to be explored. It is worth noting that understanding and quantifying the aging rate of each memory part is needed for optimal reliable memory design; this is because the different parts may degrade with different rates depending e.g. on the workload (application).

This paper focuses on 6T SRAM cell and two different SRAM sense amplifiers each targeted for a different application. The 6T cell is selected for its extensive application, while the standard latch-type sense amplifier design is selected for its superior performance [13] for HP, and double tail latch type SA due to its low power properties [13] for LP. The BTI impact for each design is analyzed using worst-case workload. The main contributions of the paper are as follows:

- Investigation of BTI impact on the 6T SRAM cell and sense amplifier swing and sensing delay; two different target application are considered.
- Thorough quantitative analysis of the BTI impact using two applications.
- Comparison between SRAM cell and sense amplifier designs for high performance and low power application.

The rest of the paper is organized as follows: Section II introduces bias temperature instability model, and the architectures of the 6T SRAM cell and sense amplifier designs, i.e.; standard latch type and double-tail latch type sense amplifier. Section III provides our analysis framework, it presents also the performed experiments. Section IV analyzes the result for different designs, and applications. Finally, Section V concludes the paper.

II. Background

This section presents the bias temperature instability model analyzed in this paper. Thereafter, it explains the working

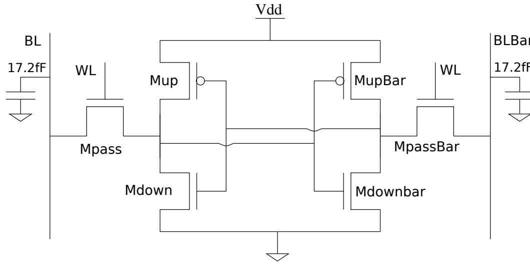

Fig. 1. 6T SRAM cell.

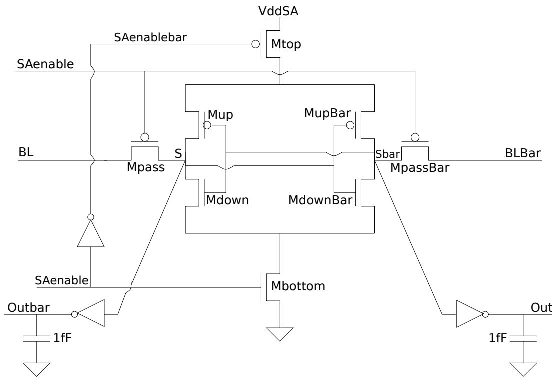

Fig. 2. Standard latch-type sense amplifier.

principles of the targeted 6T SRAM cell and sense amplifiers.

A. Atomistic Model

Kaczer *et al*. proposed the atomistic model in [14,15]. It is based on the capture and emission of single traps during stress and relaxation phases of NBTI/PBTI, respectively. The threshold voltage shift of the device ΔV_{th} is the accumulated result of all the capture and emission of carriers in gate oxide defect traps. The probabilities of the defect occupancy in case of capture P_C and emission P_E are defined by [16]

$$P_C(t_{STRESS}) = \frac{\tau_e}{\tau_c + \tau_e}\left\{1 - exp\left[-(\frac{1}{\tau_e} + \frac{1}{\tau_c})t_{STRESS}\right]\right\} \quad (1)$$

$$P_E(t_{RELAX}) = \frac{\tau_c}{\tau_c + \tau_e}\left\{1 - exp\left[-(\frac{1}{\tau_e} + \frac{1}{\tau_c})t_{RELAX}\right]\right\} \quad (2)$$

where τ_c and τ_e are the mean capture and emission time constants, and t_{STRESS} and t_{RELAX} are the stress and relaxation periods, respectively. Furthermore, BTI induced V_{th} is an integral function of capture emission time (CET) map, workloads, duty factor and transistor dimensions, which gives the mean number of available traps in each device [17].

B. Memory systems

A memory systems comprise memory cell array, row and column address decoders, read/write circuitry, input/output data registers and control logic as depicted in [11]. However, the main focus of this paper is 6T SRAM cell and two sense amplifiers designs. In this section, first the 6T SRAM cell will be described and later the standard latch-type SRAM strobed sense amplifier will be addressed which is representative for HP industrial SA designs [13]. Thereafter, the LP double-tail latch type sense amplifier is described [13].

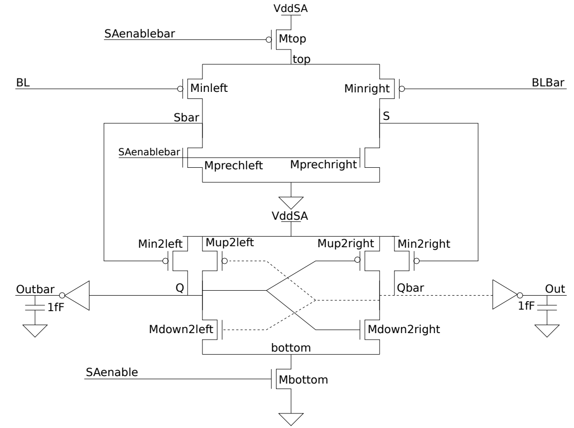

Fig. 3. The double tail latch type sense amplifier

6T SRAM cell

Fig. 1 depicts the diagram of a 6T SRAM cell. The 6T cell comprises of two cross coupled inverters that retain the data and two pass transistors. The word line (WL) is high when the cell is accessed and low when the cell is not accessed.

Standard Latch-Type Sense Amplifier (SLT SA)

The structure of the Standard latch-type Sense Amplifier is depicted in Fig. 2. The operation of the sense amplifier consists of two phases. In the first phase, when SAenable is low, the access transistors Mpass and MpassBar connect to the BL (BLBar) with the internal nodes S (Sbar). In this phase, Mtop and Mbottom transistors are switched off. In the second phase, when SAenable is high, the pass transistors disconnect the BL (BLBar) input from the internal nodes. The cross coupled inverters get their current from Mtop and Mbottom and subsequently amplify the difference between S and Sbar and produce digital outputs on Out and Outbar. S (Sbar) node is actively pulled down when Sbar (S) exceeds the threshold voltage of Mdown. The positive feedback loop ensures low amplification time and produces the read value at its output. Moreover, all current paths are disabled when S (Sbar) is at 0V and S (Sbar) is at $V_{dd\mathrm{SA}}$ or vice versa. This process is repeated for each read operation.

Double-tail latch-type Sense Amplifier (DTLT SA)

Fig. 3 introduces the double-tail latch-type SA. It uses two tails, one for capturing the input and the other for amplification and latching. Initially, when SAenable = 0V, Mtop and Mbottom are disabled. Nevertheless, S and Sbar are pulled to ground by Mprechleft and Mprechright, respectively. Subsequently, Q and Qbar are pulled up. Thereafter, when SAenable = 1V, the capturing tail will charge up nodes S and Sbar; their charge time depends on the inputs BL and BLBar. The ΔS creates a voltage difference at Q and Qbar through transistors Min2left and Min2right. Finally, the amplification and latching tail will amplify this voltage difference.

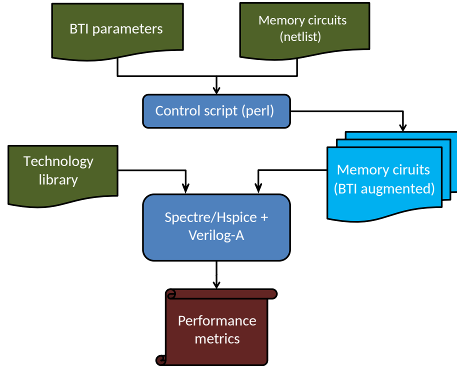

Fig. 4. Analysis framework.

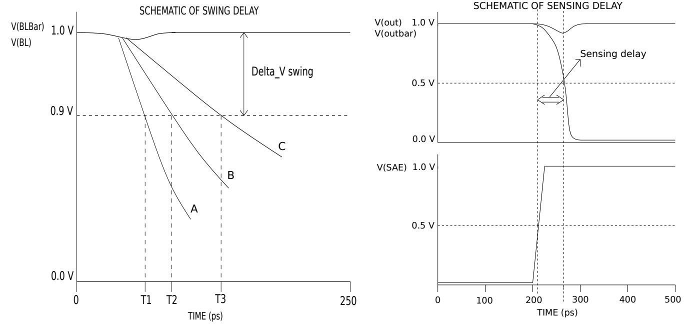

Fig. 5. Metric diagram of (a) Swing delay and (b) Sensing delay.

III. Analysis Framework

A. Framework Flow

Fig. 4 depicts our generic framework to evaluate the BTI impact on the memory ciruits i.e., 6T SRAM cell and sense amplifier circuits. Next, its inputs, processing and output blocks are described.

Input: The general input blocks of the framework are the technology library, Sense Amplifier design, and BTI input parameters. They are explained as follows. In this section, the analysis framework and the conducted experiments are presented.

- Technology library: In this work we only use the 45nm PTM library [18]. For the LP 6T SRAM cell and SA we use the LP library, while for HP 6T SRAM cell and SA the HP library. Note that in general any library card can be used.
- Memory ciruit design: Generally, all SRAM cell and sense amplifier design can be used. In this paper we focus only on 6T SRAM cell, the standard latch-type SA and double-tail latch-type SA. The 6T SRAM cell and SA designs are described by a SPICE netlist.
- BTI parameters: The BTI induced degradation depends strongly on the stress time duration. The stress time defines how long the workload sequence is being applied. The workload sequence is assumed to be repeated until the age time is reached. To perform realistic workload analysis, we assume that today's applications consist of 10% - 90% memory instructions and the percentage of read instructions is typically 50% - 90%. We derive from these assumptions the following cases: *best-case* with stress period of 0.1 * 0.1 = 0.01, *worst-case* with 0.9 * 0.9 = 0.81, and *mid-case* with 0.5 * 0.5 = 0.25. They lead to the following workload sequences: best-case: $R0R1I^{198}$, worst-case: $R0^4I^1$ and mid-case: $R0I^{24}$. In these sequences, $R0$ stands for read 0, $R1$ stands for read 1, I for idle operation (which includes memory write operations).

Processing: Based on the transistor dimensions and the other specified inputs, the Control script (perl) generates several instances of BTI augmented SRAM sense amplifier circuits. Every generated instance has a distinct number of traps (with their unique timing constants) in each transistor, and are incorporated in a Verilog-A module of the SA netlist. The module responds to the every individual trap, and alters the transistors concerned parameters such as V_{th}. After inserting BTI in every transistor of the SA design, a Monte Carlo (MC) is performed at different time steps (100 runs at each time step) where circuit simulator (HSPICE/Spectre) is used to investigate the BTI impact. Only the mean of this distribution is quantified in this paper due to limited space.

B. Output Metrics

In this section, the swing and sensing delay metrics used for analyzing BTI impact on SRAM cell and sense amplifier designs are described.

Swing delay: The swing delay is the required time for one of the node of the cell to be discharged till the pre-defined voltage swing between the BLs is reached. For example, $T1$ is the swing delay for case A while $T2$ and $T3$ are the swing delays for cases B and C, respectively as shown in Fig. 5(a).

Sensing delay: The sensing delay metric is determined when the trigger signal (i.e., sense amplifier enable input signal) reaches 50% of the supply voltage and the target (i.e., either Out or Outbar falling output signal) reaches 50% of the supply voltage. The difference between the target and the trigger results in sensing delay as shown in Fig. 5(b).

C. Experiments Performed

In this paper, two sets of experiments are performed to analyze BTI impacts. These experiments are described below:

1 **BTI Impact Experiments:** BTI impact on swing and sensing delay for SRAM cell and SA design for High Performance application at nominal voltage and temperature is investigated.

2 **Design Dependent Experiments:** BTI impact on the swing and sensing delay of the SRAM cell and sense amplifier is investigated for both applications.

IV. Experimental Results

In this section, we present the analysis results of the experiments mentioned in the previous section.

A. BTI Impact Experiments

The BTI in MOS transistors affects the swing delay and the sensing delay of the 6T SRAM cell and the sense amplifier

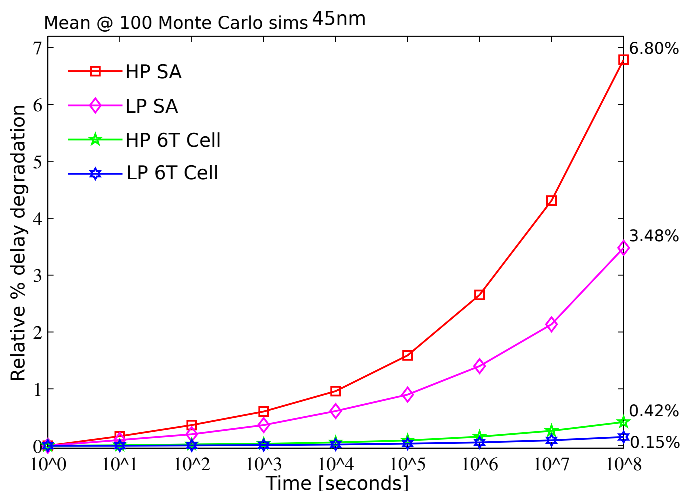

Fig. 6. BTI impact on relative % delay degradation.

designs, respectively. Moreover, the time needed for the predefined bit line swing voltage to degrade for a period of three years (see Fig. 1) and the time required to amplify the input from BL and BLBar to outputs Out and Outbar (see Fig. 2, 3). In order to quantify this relative % delay, i.e., swing delay for the cell and sensing delay for the SA, we simulate the initial BTI-free for both Cell and SA design, for 45nm technology node and take the relative % delay as references. To obtain proper relative % delay, appropriate values of BL and BLBar should be selected. For 45nm, we calibrated the differential input to be 89.4mV for HP and 99.5mV for LP applications [13]. Fig. 6 shows the relative increment of the delay w.r.t. the stress time (aging) for worst-case workload. The figure shows a quadratic type of delay increment w.r.t., the stress time. For instance, after an operation of 10^8sec, the delay increments equals 6.80% for HP SA and approaches 0.42% for HP 6T cell, respectively while in absolute numbers HP SA degrades more than the HP 6T cell design.

B. Design Dependent Experiments

The BTI induced degradation impacts differently for various parts of the memory systems, i.e., cell and SA designs and for different applications, i.e., HP and LP for the worst-case workload. The workload defines when and how long each transistor is stressed. Fig. 6 shows the BTI impact for relative % delay for both Cell's swing delay and SA's sensing delay, i.e., for HP and LP applications, respectively. For the HP application, i.e., HP designs, the relative % delay increases to 6.80% for the HP SA; while it is 0.42% for HP 6T Cell for worst-case workload. Furthermore, for the LP application, i.e., LP designs, the relative % delay increases to 3.48% for the LP SA; while it is 0.15% for LP 6T Cell for worst-case workload. Furthermore, in absolute numbers at 10^8s, the LP memory cell seems to be the design with marginal degradation while HP SA with maximum degradation.

C. Discussion

Understanding and quantifying the aging rate for different parts of memory system design is crucial for reliable and optimal SRAM systems. The current analysis focused on 6T SRAM cell, LP SA, and HP SA designs for the nominal supply voltage and room temperature. The relative % delay degrades faster for HP and LP SA while marginally for HP and LP 6T SRAM cell designs. We observed an increase in the absolute numbers for HP SA than for LP 6T cell design. This implies that BTI impact for 6T SRAM cell is of less concern for the 45nm technology node and could be a challenge as the technology scales down up to 16nm technology node.

V. Conclusion

This paper investigated the impact of Bias Temperature Instability (BTI) on swing and sensing delay for different memory parts (i.e., 6T SRAM cell (both LP and HP application) and on the standard latch type (SLT) (HP) and double-tail latch type (DTLT) (LP) memory sense amplifiers). In this paper, we have shown that the delay degradation is more impacted by HP applications for both Cell and SA designs for worst-case workload. We observed for both the HP and LP 6T SRAM Cell a marginal increment in relative % delay when BTI is considered. Therefore, it is crucial for designers to analyze BTI impact at the early design stages for different memory parts to understand which part to be focused on for optimal reliable design.

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