BTI Analysis of SRAM Write Driver

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***Abstract*—Bias Temperature Instability (BTI) has become a major reliability challenge for nano-scaled devices. This paper presents BTI analysis for the SRAM write driver. Its evaluation metric, the write delay (WD), is analyzed for various supply voltages and temperatures for three technology nodes, i.e., 45nm, 32nm, and 22nm. The results show that as technology scales down, BTI impact on write delay (i.e., its average and $+/-3\sigma$ variations) increases; the 22nm design can degrade up to $1.9\times$ more than the 45nm design at nominal operation conditions. In addition, the result shows that an increment in supply voltage (i.e., from $-10\%V_{dd}$ to $+10\%V_{dd}$) increases the relative write delay during the operational lifetime. Furthermore, the results show that a temperature increment accelerates the BTI induced write delay significantly; while at 298K the degradation is up to 4.7%, it increases to 41.4% at 398K for the 22nm technology node.**

***Index Terms*—BTI, NBTI, PBTI, SRAM write driver**

I. Introduction

In recent decades, CMOS technology has witnessed relentless downscaling [1]. Forces behind the trend are advancements in the fabrication technology, introduction of novel materials and evolution of architecture designs. However, for circuits based on the current CMOS technology, reliability failures have become a major bottleneck [1]–[3]. Bias Temperature Instability (BTI) (i.e., Negative BTI in PMOS transistors and Positive BTI in NMOS transistors) is a reliability failure mechanism which affects the strength of MOS transistors by increasing their threshold voltages and reducing their drain current (I_d) over the operational lifetime [4]–[6].

Static Random-Access Memories (SRAM) occupy a large part of semiconductor systems and play a major role in the silicon area, performance, and critical robustness [7]. An SRAM system consists of cells array, and its peripherals circuits such as column and row address decoders, control circuits, sense amplifiers and write drivers. Many previous work focused on the BTI SRAM cell array [8] and only a few on the SRAM peripheral circuitry. For example, Binjie *et al.* [9] investigated the NBTI impact on the degradation of Static Noise Margin (SNM) and Write Noise Margin (WNM) for the 6T SRAM cell. Kumar *et al.* [10] analyzed the impact of NBTI on the read stability and SNM of SRAM cells. Bansal *et al.* [11] analyzed the stability of an SRAM cell for worst-case conditions and in the presence of NBTI and PBTI, both individually and combined. Weckx *et al.* [12] investigated a novel statistical based approach for workload dependent circuit lifetime projections which focused on the degradation of SNM metric for 6T SRAM cell. On the other hand, few authors have focused on the reliability analysis of the periheral circuits. Khan *et al.* [13] investigated the combined impact of partial opens and BTI in SRAM address decoder. Menchaca *et al.* [14] analyzed the BTI impact on different sense amplifier designs implemented in 32nm technology node by using failure probability (i.e., flipping a wrong value) as a reliability metric. Agbo *et al.* [15] investigated the BTI impact on SRAM drain-input latch type sense amplifier. In [16] the same authors investigated the integral impact of BTI and voltage temperature variations on SRAM Sense Amplifier. However, to our best knowledge, no previous work focused on the BTI impact on the write driver.

This paper focuses on the write driver design as it has the vital role to ensure correct data is written to the cell [17]. Although, it is obvious that BTI increases delay and reduces memory reliability, the actual BTI impact on the write driver still needs to be characterized. In this regard, the main contributions of the paper are:

- Investigation of BTI impact on the write driver's mean write delay and its distribution.
- Analysis of BTI impact on the write driver at nominal supply voltage for various technology nodes i.e., 45nm, 32nm, and 22nm, respectively; both nominal and high temperature (i.e., 398K) are considered.
- Investigation of BTI impact for varying supply voltages for the write driver design.
- Exploring BTI impact for varying temperatures for the write driver's write delay.

The results depict that with the downscaling of CMOS technology, BTI impact on the write delay causes a significant increment. Moreover, a temperature increase may lead to alarming write delay increment; the impact must be properly investigated to ensure robust and reliable write drivers.

The rest of the paper is organized as follows. Section II introduces the BTI model and memory write driver. Section III provides our analysis and simulation framework, and presents the performed experiments. Section IV analyzes the result for different technology nodes and various supply voltages and temperatures. Finally, Section V concludes the paper

II. Background

This section explains first the BTI mechanism. Afterwards, it explains the functional model of an SRAM system. Finally, it presents the behavior of the precharge circuit, SRAM 6T

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cell, and the analyzed write driver; the precharge and 6T cell are part of the write operation.

A. Bias Temperature Instability

The Bias Temperature Instability (BTI) mechanism takes place inside the MOS transistors and causes a threshold voltage shift that impacts the delay negatively; its mechanism is described below.

BTI Mechanism

BTI increases the absolute V_{th} value in MOS transistors. For the PMOS, the negative V_{th} decreases while for the NMOS the V_{th} increases. The increment in V_{th} in a PMOS transistor that occurs under *negative* gate stress is referred to as NBTI, and the decrement that occurs in an NMOS transistor under *positive* gate stress is known as PBTI. For both MOS transistors, there are two BTI phases, i.e., the stress phase and the relaxation phase.
Recently, exhaustive efforts have been put to understand NBTI [4], [5], [13], [18]. Kaczer *et al.* in [18] have analyzed NBTI using an atomistic model. Alam *et al.* [4] have modeled NBTI and presented the overall dynamics of NBTI as a reaction diffusion process. The model is usable at a higher level such as circuit level. In Kukner *et al.* in [17], both the atomistic and RD models have been compared. In this work, we use the atomistic model as its BTI predictions are more accurate than these from the RD model [17]. We will briefly describe the atomistic model next.

Atomistic Model

Kaczer et al. proposed the atomistic model in [19]. It is based on the capture and emission of single traps during stress and relaxation phases of NBTI/PBTI respectively. The threshold voltage shift of the device ΔV_{th} is the accumulated results of all the capture and emission of carriers in gate oxide defect traps. The probabilities of the defect occupancy in case of capture P_C and emission P_E are defined by

$$P_C(t_{STRESS}) = \frac{\tau_e}{\tau_c + \tau_e}\left\{1 - exp\left[-(\frac{1}{\tau_e} + \frac{1}{\tau_c})t_{STRESS}\right]\right\} \quad (1)$$

$$P_E(t_{RELAX}) = \frac{\tau_c}{\tau_c + \tau_e}\left\{1 - exp\left[-(\frac{1}{\tau_e} + \frac{1}{\tau_c})t_{RELAX}\right]\right\} \quad (2)$$

where τ_c and τ_e are the mean capture and emission time constants, and t_{STRESS} and t_{RELAX} are the stress and relaxation periods, respectively. Furthermore, BTI induced V_{th} is an integral function of Capture/Emission Time CET map [20], workloads, duty factor and transistor dimensions, which gives the mean number of available traps in each device.

B. Memory model

A memory system comprises memory cell array, row and column address decoders, read/write circuitry, input/output data registers and control logic as depicted in functional model of SRAM system in Fig. 1. [21]. The main focus of this paper is the SRAM write driver; in addition, the precharge and SRAM circuit will be also explained as they effect the write operation.

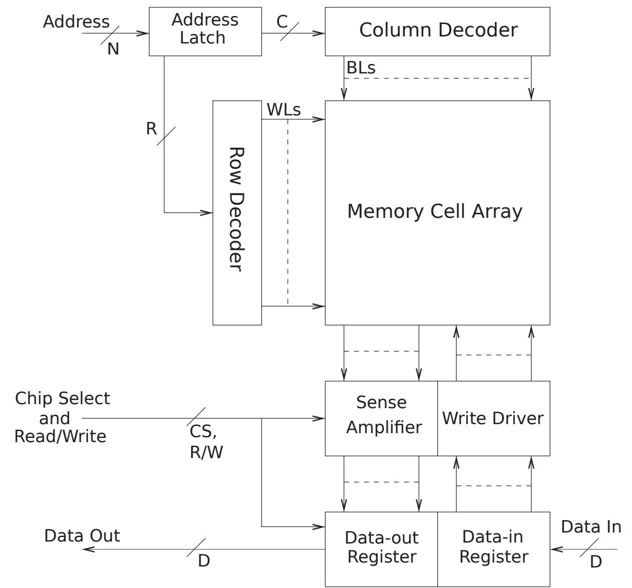

Fig. 1. Functional model of SRAM system

Figure 2 shows the simulation model which is divided into three parts (i.e., precharge circuitry, 6T cell, and the write driver). These parts will be explained below. To be able to read correct data (i.e., either a one or zero) from a memory cell, first valid data must be written into the cell. The circuit that is responsible for correct writing of data into the memory cell is called the write driver. A possible implementation of the write driver is shown in the bottom of Fig. 2. The write operation starts with the precharge circuit that precharges both bit-lines (i.e., *Bl* and *BLBar*). Subsequently, the write driver forces one of the bit-lines to zero, while maintaining the precharged value on the other bit-line. After sometime, when the word line of the cell is activated, the cell's internal state takes over the written values on BL and BLBar.

Precharge circuit

The precharge consists of three PMOS transistors connected to the bit lines (i.e., *BL* and *BLBar*). The differential bit lines are connected to the cell and these bit lines are precharged to high state in typical high-performance memory.

SRAM 6T cell

The SRAM 6T cell consists of six transistors (i.e., two pull-up (PMOS), two pull-down (NMOS), and two pass (NMOS) transistors) which is the basic building block of any memory cell. An SRAM cell has a bistable circuit characteristics which implies that it can be driven into one of the two states and still retains its state as the power goes on.

Write driver

The write driver [21] consists of two pass transistors (i.e., NMOS) and two inverter circuitry. The pass transistors are the transfer device of an SRAM cell, which effectively drives a logic zero but not a logic one. The write operation is realized by writing a zero into either BL or $BLBar$. Thereafter, the

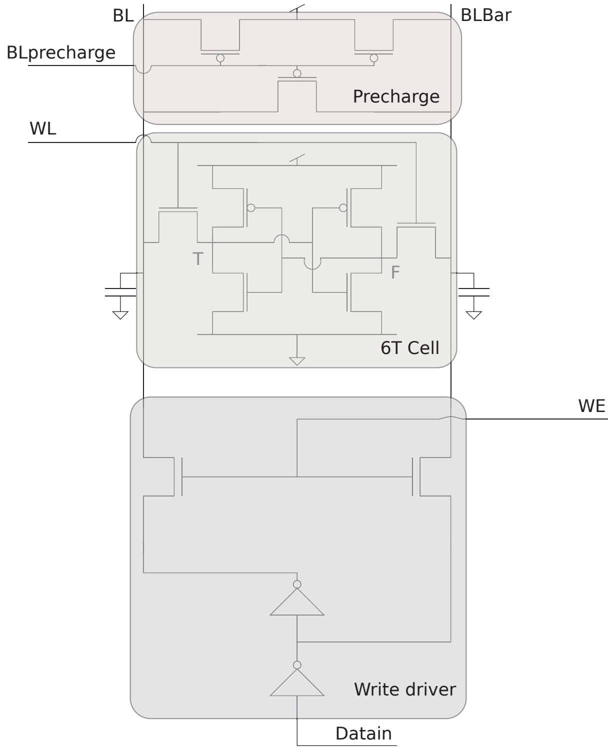

Fig. 2. Simulation setup.

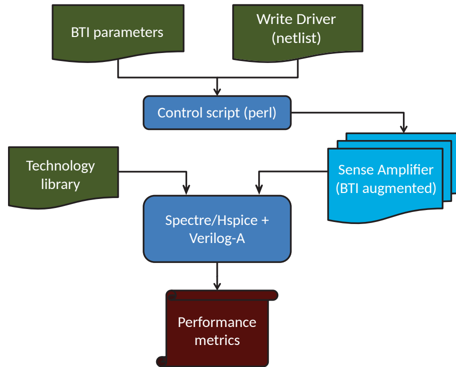

Fig. 3. Analysis framework.

cross-coupled inverters of the cell change the logic zero to a logic one at the other storage node. Then, when the write enable (i.e., WE) signal is activated, the data is transfered to the BLs. Since, forcing a strong zero into one of the BLs is the main target, the PMOS and NMOS devices may be equally sized.

III. Analysis Framework

In this section, the analysis framework and the conducted experiments are presented.

A. Framework Flow

Figure 3 depicts our generic framework to evaluate the BTI impact on the considered memory write driver circuitry. Next, its inputs, processing and output blocks are described.

Input: The general input blocks of the framework are the technology library, memory write driver design, and BTI input parameters. They are explained as follows.

- Technology library: In this work we use three technology nodes; they are 45nm, 32nm, and 22nm PTM library [22]. Note that in general any library card can be used.
- WD design: Generally, all write driver design can be used. In this paper we focus only on the typical write driver (WD) shown in fig. 2. and is described by a SPICE netlist.
- BTI parameters: The BTI induced degradation depends strongly on the stress time duration. The stress time defines how long the workload sequence is being applied. The workload sequence is assumed to be replicated until the age time is reached. The workload assumed in this experiment is based on a 50% duty factor for each transistor of the WD.
- TV: This block specifies the temperature and voltage; each is explained next.

A. Temperature

Temperature variation is an important factor in BTI induced degradation of SRAM write drivers write delay. For instance, MOS transistors threshold voltage reduces as temperature increases. In this paper, we restrict ourselves to temperatures Nominal T_1 = 298K, T_2 = 348K, and T_3 = 398K.

B. Voltage

Supply voltage variations can impact the write delay significantly as it impacts the operational speed. In addition, variation in supply voltage also affects the oxide field (capacitance) inside the transistors and subsequently the BTI impact. In this paper, we restrict ourselves to three supply voltages: V_1 = -10%V_{dd}, V_2 = Nominal V_{dd}, and V_3 = = +10%V_{dd}. Note that the nominal V_{dd} for 45nm is 1.0V while 0.9V for 32nm and 0.8V for 22nm technology.

Processing:

Based on the transistor dimensions and the other specified inputs, the Control script (perl) generates several instances of the BTI augmented SRAM write driver. Every generated instance has a distinct number of traps (with their unique timing constants) in each transistor, and are incorporated in a Verilog-A module of the WD netlist. The module responds to the every individual trap, and alters the transistors concerned parameters such as Vth. After inserting BTI in every transistor of the WD design, a Monte Carlo (MC) is performed at different time steps (100 runs at each time step) where circuit simulator (HSPICE/Spectre) is used to measure the BTI impact. In this paper, our analysis focus on both the mean write delay (denoted by diamond marker in the figure) and its distribution (i.e., +/-3σ denoted by the edges of the vertical lines in the figure).

Output: Finally, statistical post-analysis of the results are performed for varying supply voltages and temperatures in MATLAB environment. The raw outputs are measured directly

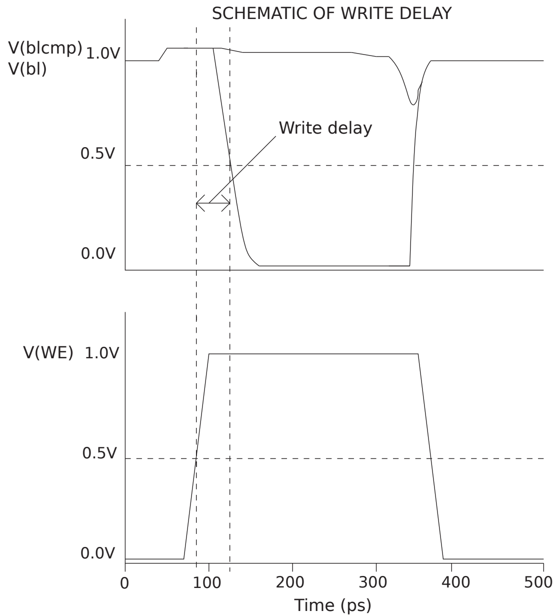

Fig. 4. Metric diagram of Write delay.

from HSPICE/Spectre and measure the write delay. The write delay metric is determined when the trigger signal (i.e., write enable input signal) reaches 50% of the supply voltage and the target (i.e., either *bl* or *blcmp* falling output signal) reaches 50% of the supply voltage while the initial conditions of the cell flips to the correct state of the Bit lines. The difference between the target and the trigger results in write delay as shown in Fig. 4. Furthermore, the impact of the BTI degradation is measured relatively to the case where no BTI is present.

B. Experiments Performed

In this paper, four sets of experiments are performed. These experiments are described below:

1. BTI Impact Experiments: The BTI impact on the write delay is investigated for different lifetime.

2. Technology Dependent Experiments: The BTI impact on the write delay for three technology nodes at nominal voltage (i.e., 22nm, 32nm, and 45nm) is investigated. This is performed at nominal and high temperature (i.e., 398K).

3. Supply voltage Dependent Experiments: The BTI impact on the write delay for various supply voltages (i.e., from -10% to +10% V_{dd}) is explored.

4. Temperature Dependent Experiments: The BTI impact on the write delay for various temperatures (i.e., 298K, 348K and 398K) is investigated.

IV. EXPERIMENTAL RESULTS

In this section, we present the analysis results of the experiments mentioned in the previous section.

A. BTI Impact Experiments

Figure 5 shows the absolute mean write delay (denoted by diamond markers) and its distribution, i.e., $+/-3\sigma$ (denoted by the edges of the vertical lines) w.r.t. aging up to 3 years degradation (10^8s) for the write driver.

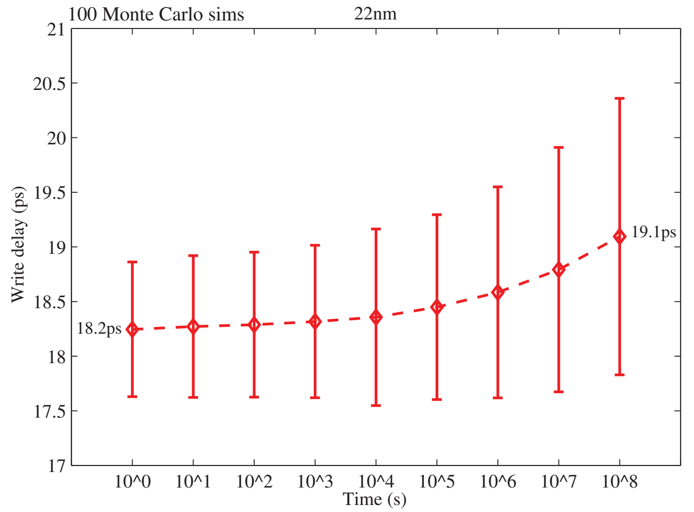

Fig. 5. BTI impact on Write delay for 22nm technology.

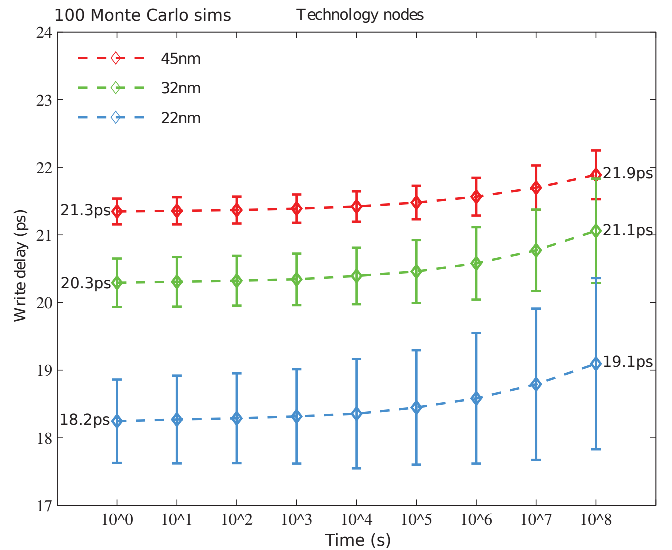

Fig. 6. BTI impact on Write delay for various technology nodes.

The figure shows that the write delay increases over time. For example, the delay increases up to 4.7% in 3 years. The figure also shows that the degradation of the distribution widens over time. For example, the write delay $+3\sigma$ variation increases from 0.6ps to 1.3ps in 3 years.

B. Technology Dependent Experiments

Figure 6 depicts the absolute BTI induced write delay (i.e., its mean and distribution) for the three technology nodes (i.e., 45nm, 32nm, and 22nm) at 298K. The figure shows that all the technology nodes follow the same trends. The smaller the technology node, the higher the relative impact and the wider the $+3\sigma$ variation. For example, after 3 years operational lifetime, the BTI induced relative degradation is 2.82% for 45nm while 3.94% for 32nm node and only 4.95% for 22nm node. In addition, the figure shows that the write delay after 10^8s for 22nm is the fastest when compared to 32nm and

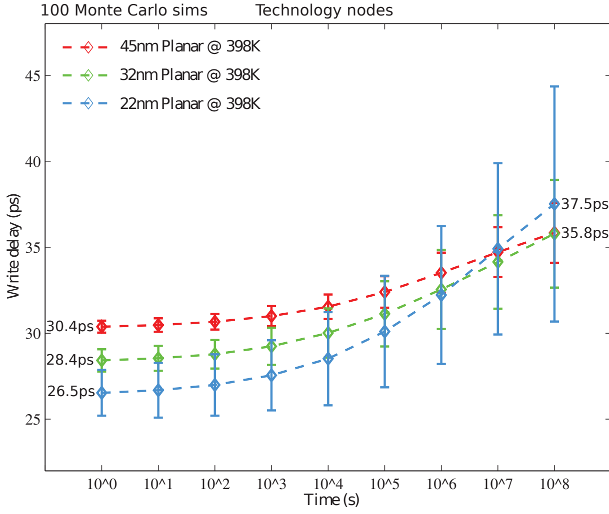

Fig. 7. BTI impact on Write delay for various technology nodes at 398K.

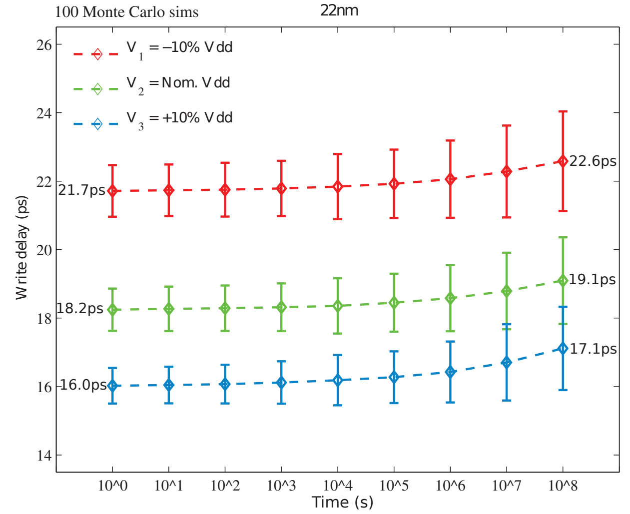

Fig. 8. BTI impact on write delay for varying supply voltages.

45nm nodes. For example, after 3 years, the absolute delay degradation for 22nm is up to 1.11× faster than 32nm and only 1.15× faster than 45nm. The figure also shows that the distribution of the degradation is the widest for the lower nodes irrespective of the operational time. For example, after an operation of 10^8s, the BTI induced distribution (i.e., +3σ variation) is 1.3ps for 22nm while 0.8ps and 0.4ps for 32nm and 45nm, respectively. More importantly, the figure shows that after 10^7s the worst case, 22nm drivers (i.e., the slowest ones) become even slower than the worst case drivers of 32nm and 45nm.

Figure 7 shows the BTI induced degradation for different technology nodes at 398K. The figure also shows that the mean BTI induced write delay for 22nm nodes overlaps 32nm and 45nm nodes after an operation of 10^6s to 10^7s; the mean write delay is 5% higher for 22nm at 10^8s over 32nm and 45nm. In addition, the same trend is observed for write delay distribution (i.e., +3σ variation) at 398K. Hence, the degradation distribution is the widest for lower node (i.e., 22nm) at higher temperature.

C. Supply Voltage Dependent Experiments

Figure 8 shows the absolute BTI induced write delay (i.e., average and +/-3σ distribution) for various supply voltages for the write driver design. At 10^0s, when the devices are still fresh, the write driver operates faster at higher V_{dd}. For example, after an operation of 10^0s the absolute write delay is 16.0ps for +10% V_{dd}, and 18.2ps for nominal V_{dd} while 21.7ps for -10% V_{dd}. The figure also shows that the BTI induced write delay increases irrespective of supply voltage considered. For example, after an operation of 10^0s, the degradation is 21.7ps and 22.6ps at 10^8s for -10% V_{dd}, while for 10^0s is 18.2ps and 19.1ps at 10^8s for nominal V_{dd}, and only 16.0ps at 10^0s and 17.1ps at 10^8s for +10% V_{dd}, which shows % increment of 4.0% for -10%V_{dd}, while 4.7% and only 6.8% for nominal V_{dd} and +10%V_{dd}, respectively. It is worth noting that the

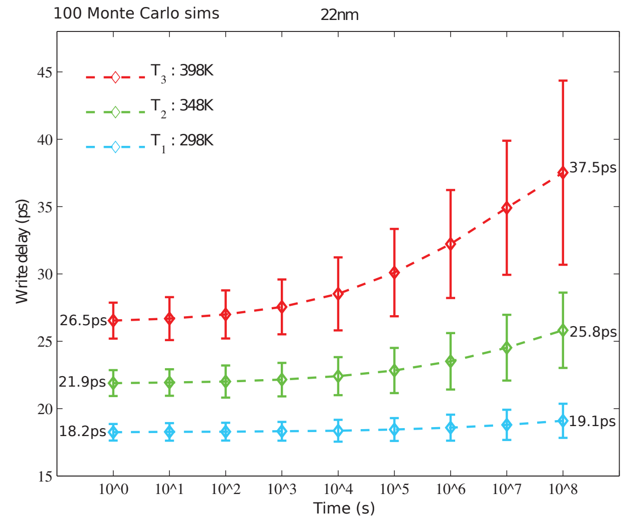

Fig. 9. BTI impact on write delay for varying temperatures.

increase in supply voltage reduces the BTI induced write delay in absolute terms while increases the degradation in relative terms.

The figure also shows that the distribution of the degradation (i.e., +3σ variation) widens as the supply voltage reduces from +10% V_{dd} to -10% V_{dd}. For example, after an operation of 10^8s the +3σ spread equals 1.5ps for +10%V_{dd} and 1.3ps for nominal V_{dd} while 1.2ps for -10%V_{dd}; at +10% V_{dd} this is 1.25× higher than at -10% V_{dd}, while at nominal V_{dd} is 1.08× higher than at -10% V_{dd}.

D. Temperature Dependent Experiments

Figure 9 shows the absolute BTI induced degradation (i.e., average and +/-3σ distribution) for three temperatures (i.e., T_1 = 298K, T_2 = 348K, and T_3 = 398K) for the write driver design. The figure shows that an increase in temperature increases the BTI induced write delay. For example, after an operation of 10^0s the absolute write delay degradation

is 18.2ps for 298K and 21.9ps for 348K while 26.5ps for 398K. Furthermore, after an operation of 10^8s the BTI induced degradation is 19.1ps for 298K and 25.8ps for 348K while 37.5ps for 398K which is about 4.7% for 298K and 17.9% for 348K while 41.4% for 398K.

The figure also shows that the degradation distribution (i.e., +3σ) widens as the temperature increases from 298K to 398K. For example, after an operation of 10^8s the +3σ spread equals 1.2ps for 298K and 2.1ps for 348K, while 3.6ps for 398K; at 398K this is 3× higher than at 298K and at 348K only 1.75× higher than at 298K.

E. Discussion

Memory write driver robustness and reliability are very vital for the overall design of memory systems. The presented analysis show that the BTI induced write delay and its distribution of the write driver design is a function of technology, supply voltage, and temperature etc. Evaluating the simulation results with respect to degradation and its variations (i.e., +/-3σ) we conclude the following:

- At lower nodes (i.e., 22nm) the write delay degradation is the worst when compared to other technologies reported in this work; this indicates that BTI may be a serious concern and it may lead to read failures at a lower technology nodes. Moreover, the degradation variation at both corners (i.e., $+/-3\sigma$) of the Planar node is the widest for the 22nm irrespective of the operational lifetime considered, when compared with higher technology nodes. This variation is very crucial and require urgent mitigation technique to address it.
- The degradation increases with decrease in power supply in absolute terms irrespective of the operational lifetime and the distribution follows the same path as the degradation; this implies that at higher power supply, the degradation reduces in absolute terms. However, the mean degradation follows an opposite path in relative terms while the distribution remains the same.
- The degradation and its distribution are worst at a higher temperature (i.e., 398K); this is applied to both absolute and relative terms. The degradation is up to 37.5ps while its distribution is up to 6.8ps at 10^8s operational time.
- The degradation analysis of the memory sub-circuits (i.e., cell, sense amplifier (SA), write driver, etc.) show that SA degrades the most i.e., up to 2.72× more than the write driver while 16.2× more than the cell using various delay metrics i.e., sensing delay for SA, and swing delay for the cell [23]; while write delay for the write driver presented in this work.
- The analysis of BTI on write driver design necessitate understanding and quantifying the aging rate for different parts of memory systems for optimal and reliable SRAM systems.

V. Conclusion

This paper investigates the impact of Bias Temperature Instability (BTI) for memory write driver for different technologies while considering various supply voltages and temperatures. First, BTI impact increases the write delay and its distributions as the technology nodes scales down causing the memory write driver to be less reliable and robust. Second, increase in supply voltage per technology node compensate the write delay and its variation in absolute terms causing the write driver to be more robust and reliable while this is not the case when viewed from the relative terms point of view. Third, increase in temperature increases the degradation and widens its distribution. These results are validated with HSPICE/Spectre.

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