Comparative BTI Analysis for Various Sense Amplifier Designs

Innocent Agbo Mottaqiallah Taouil Said Hamdioui
Delft University of Technology
Faculty of Electrical Engineering, Mathematics and CS
Mekelweg 4, 2628 CD Delft, The Netherlands
{I.O.Agbo, M.Taouil, S.Hamdioui}@tudelft.nl

Pieter Weckx[1,2] Stefan Cosemans[1] Praveen Raghavan[1] and Francky Catthoor[1,2]
[1]imec vzw., Kapeldreef 75, B-3001, Leuven, Belgium
[2]Katholieke Universiteit Leuven, ESAT, Belgium
{Pieter.Weckx, stefan.cosemans, Ragha, Francky.catthoor}@imec.be

***Abstract*—With the continuous downscaling of CMOS technologies, ICs become more vulnerable to transistor aging mainly due to Bias Temperature Instability (BTI). This paper presents a comparative study of the BTI impact while considering varying supply voltages and temperatures for three memory sense amplifier (SA) designs: low power (LP), mid power/performance (MP), and high performance (HP). As an evaluation metric, the sensing delay (SD) of the three designs is analyzed for various workloads using 45nm technology. The results show that HP SA degrades faster than MP SA and LP SA irrespective of the workload, supply voltage, and temperature. At nominal supply voltage and temperature, HP degrades up to $1.62\times$ faster than MP, and up to $1.94\times$ faster than LP designs for the worst case workload. In addition, the results show that an increase of 10% in power supply has a marginal impact on the relative degradation. In contrast, the results show that a temperature increment significantly worsens the BTI impact. Finally, the results show that for 16nm technology, BTI impact becomes worse and even causes read failures. This clearly indicates that designing for reliability is not only strongly application dependent, but also technology node dependent. Hence, one has to carefully consider the targeted application, design, and technology node in order to provide appropriate solutions.**

***Index Terms*—BTI, NBTI, PBTI, SRAM sense amplifier**

I. Introduction

In recent decades, CMOS technology has been sustained with aggressive downscaling that severely impacts the variability and reliability of devices [1–3], originating from manufacturing (i.e., time-zero) and run-time operation, (i.e., from temperature, voltage, aging), respectively. [1]. Bias Temperature Instability (BTI) (i.e., Negative BTI in PMOS transistors and Positive BTI in NMOS transistors) is an aging reliability failure mechanism which affects the performance of MOS transistors by increasing their threshold voltage and reducing their drain current (I_d) over the operational lifetime [4,5]. However, studies of such individual devices or small composites do not allow extrapolation of these effects on larger circuits like Static Random-Access Memories (SRAMs). SRAMs, which are an integral part of any SoC today and occupy a large fraction of today's chips, play a major role in performance, and are critical for system robustness [6]; an SRAM system consists of an array of cells, and peripheral circuitry facilitates the read and write access to the cells; examples are row and column address decoders, control circuits, write drivers, and sense amplifiers. In this work we focus on the SRAM sense amplifier which is a key component that ensures that data is correctly read from the cell array.

Limited work has been published in the area of SA degradation. The authors in [7] analyzed the time zero variability of SRAM sense amplifier systems to determine the offset specification for LP designs. However, they did not take the run-time variability into account. In [8], the authors presented a scheme to determine the signal margins for DRAM SAs based on offset distribution measurements. Also for runtime variability limited work has been published. For example, Menchaca *et al.* [9] analyzed the BTI impact on different SA designs (i.e., current and voltage mode SA) implemented in 32nm technology node using failure probability (i.e., flipping a wrong value) as a reliability metric. Agbo *et al.* [10] investigated the BTI impact on LP drain-input latch type sense amplifier design implemented in 90nm, 65nm, and 45nm for different supply voltages by using sensing delay and sensing voltage as reliability metrics. The same authors [11] investigated the integral impact of BTI and voltage temperature variation on HP standard latch type SA using sensing delay as reliability metric. From the above, we conclude that no prior work discussed the run-time variability of different types of sense amplifiers (i.e., HP, MP, and LP).

This paper focuses on the aging analysis of three different SRAM sense amplifier designs using the realistic atomistic model calibrated with representative test data. The method in [7] is adopted to determine the SA offset specification of all SAs. Subsequently, the BTI impact for each design is analyzed using different workloads, temperatures, voltages, and technology nodes. The results are analyzed and compared relatively to each others.

The rest of the paper is organized as follows. Section II introduces the BTI mechanism, its model, and the architectures of the sense amplifier designs. Section III provides our analysis and simulation framework, and presents also the performed experiments. Section IV analyzes the result for different sense amplifier designs, varying supply voltages, temperatures and technology nodes. Finally, Section V concludes this paper.

II. Background

This section briefly discusses bias temperature instability mechanism and its model which is used in this work. Thereafter, it presents the three targeted sense amplifiers.

A. Bias Temperature Instability

The Bias Temperature Instability (BTI) mechanism takes place inside MOS transistors and increases the absolute V_{th}

978-1-5090-2466-7/16/$31.00 ©2016 IEEE

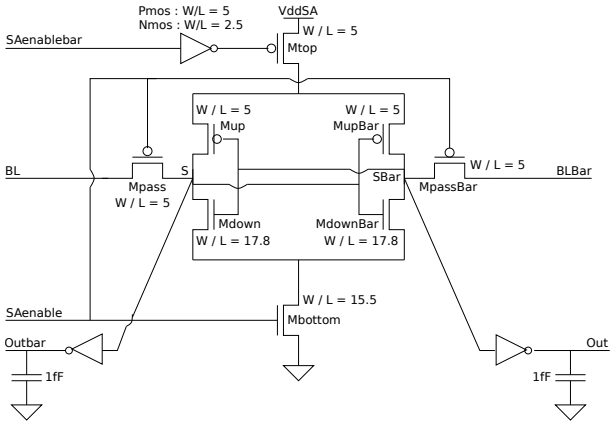

Fig. 1. Standard latch-type Sense Amplifier

value of the transistors [4,12]. The $V_{\rm th}$ increment in a PMOS transistor occurs under *negative* gate *stress* and is referred to as NBTI, while in an NMOS transistor this occurs under *positive* gate *stress*, and is known as PBTI. Note that for a MOS transistor, there are two BTI phases, i.e., the stress phase and the relaxation phase.

Recently, exhaustive efforts have been put to understand NBTI [4,5,12]. Kaczer *et al.* in [12,14] have analyzed NBTI using an atomistic model. Alam *et al.* [4] have modeled NBTI and presented the overall dynamics of NBTI as a reaction diffusion process. In this work, we use the atomistic model as it produces more accurate results than the RD model [13]. The atomistic model is based on the capture and emission of single traps during stress and relaxation phases of NBTI/PBTI respectively. The threshold voltage shift of the device ΔV_{th} is the accumulated results of all the capture and emission of carriers in gate oxide defect traps. The probabilities of the defect occupancy in case of capture P_C and emission P_E are defined by [13]:

$$P_C(t_{STRESS}) = \frac{\tau_e}{\tau_c+\tau_e}\left\{1-exp\left[-(\frac{1}{\tau_e}+\frac{1}{\tau_c})t_{STRESS}\right]\right\} \quad (1)$$

$$P_E(t_{RELAX}) = \frac{\tau_c}{\tau_c+\tau_e}\left\{1-exp\left[-(\frac{1}{\tau_e}+\frac{1}{\tau_c})t_{RELAX}\right]\right\} \quad (2)$$

where τ_c and τ_e are the mean capture and emission time constants, and t_{STRESS} and t_{RELAX} are the stress and relaxation periods, respectively. Furthermore, BTI induced V_{th} is an integral function of Capture Emission Time (CET) map [15], workloads, duty factor and transistor dimensions, which gives the mean number of available traps in each device.

B. Sense Amplifiers

In this paper, we select three sense amplifier designs: standard latch-type sense amplifier is representattive for HP industrial SA designs [7], look-ahead type sense amplifier [16], and double-tail latch-type sense amplifier [17]. They target high performance, inter-mediate performance/power and low power respectively.

Figure 1 depicts the standard latch-type sense amplifier [7], it amplifies a small voltage difference between BL and BLBar

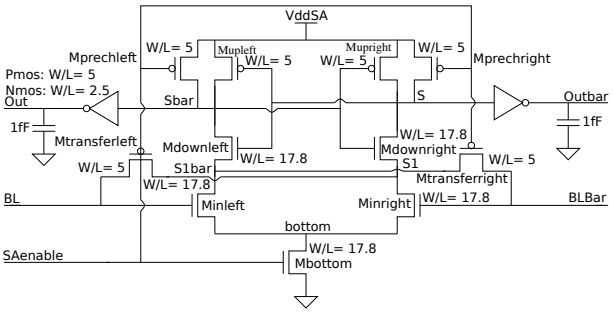

Fig. 2. The Look ahead type Sense Amplifier

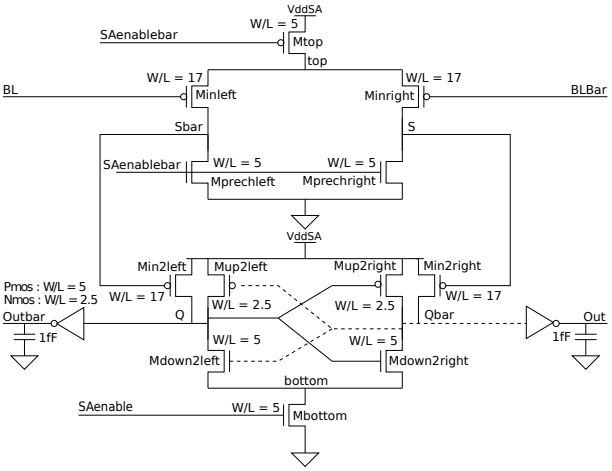

Fig. 3. The Double tail latch type Sense Amplifier

during read operations, and produces them at the output (i.e., *Out* and *Outbar*). The positive feedback loop (created by cross-coupled inverters) ensures low amplification time and produces the read value at its output.

Figure 2 depicts the Look-ahead type SA [16] which consists of two stages. In the first stage, when SAenable=0V, S and Sbar are charged up and the inputs BL and BLBar are passed to nodes S1 and S1bar, respectively. In the second stage, the cross-coupled inverters will start the amplification process.

Figure 3 introduces the double-tail latch-type SA [17]. It uses two tails, one for capturing the input and one for amplification and latching. Initially, when SAenable=0V, Mtop and Mbottom are disabled. Thereafter, when SAenable=1V, the capturing tail will charge up nodes S and Sbar; their charge time depends on the inputs BL and BLBar. The ΔS=$V_S - V_{Sbar}$ creates a voltage difference at Q and Qbar through transistors Min2left and Min2right. The amplification and latch tail will amplify this voltage difference.

III. Analysis Framework

In this section, the analysis framework, the sense amplifier offset specification and the conducted experiments are presented.

A. Framework Flow

Figure 4 depicts our generic simulation framework to evaluate the BTI impact on the three considered sense

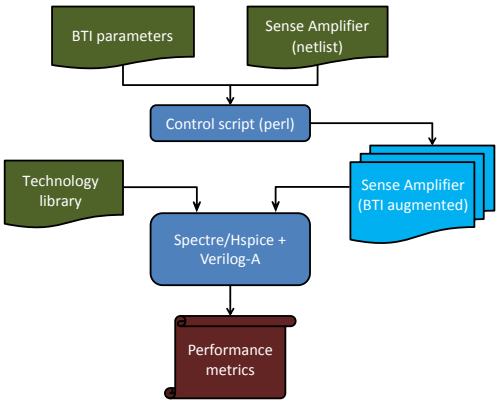

Fig. 4. Analysis framework.

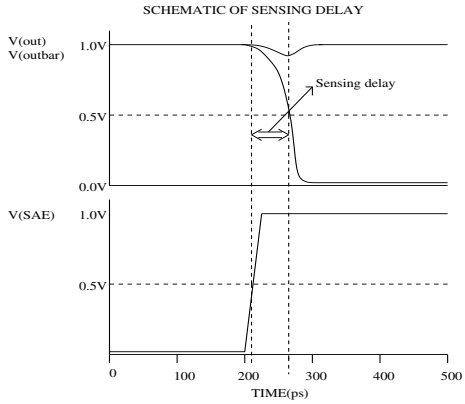

Fig. 5. Metric diagram of Sensing delay.

amplifier designs. It uses HSPICE/Spectre simulator and has the following components.

Input: The general input blocks of the framework are the technology library, Sense Amplifier design, and BTI input parameters. They are explained as follows.

- Technology library: Two technology nodes are considered in this work, they are 16nm and 45nm obtained from PTM library cards [19]. For the LP SA we use the LP library, while for the MP SA and HP SA the HP library. Note that in general any library card can be used.
- SA design: Generally, any sense amplifier design can be used. In this paper we focus only on the standard latch-type SA, look-ahead type SA, and double-tail latch-type SA. The SA designs are described by a SPICE netlist.
- BTI parameters: The BTI induced degradation depends strongly on the stress time duration. The stress time defines how long the workload sequence is being applied. The workload sequence is assumed to be replicated once completed until the age time is reached. To perform realistic workload analysis, we assume that today's application consists of $10\%-90\%$ memory instructions and the percentage of read instructions is typically 50%-90%. Furthermore, we derive from these the two extreme workload cases: worst case: $0.9*0.9=81\%$ and best case: $0.1*0.1=1\%$. In addition, we define a mid case workload. This leads to the following workload sequences: $R0^4I^1$ for worst-case, $R0R1I^{198}$ for best-case, and $(R0)I^{24}$ for mid-case, where, $R0$ stands for read 0, $R1$ stands for read 1, I for idle operation (which includes memory write operations). For example, $R0R1I^{198}$ is a workload describing a read 0 and a read 1 performed after each 198 idle operations. For each transistor, we extract its individual duty factor based on the workload and waveform analysis. This enhances the accuracy of our simulation results. This block also specifies the temperatures and voltages.

Processing: Based on the transistor dimensions and other specified inputs, a Control script (perl) generates several instances of BTI augmented SRAM sense amplifier designs. Every generated instance has a distinct number of traps (with their unique timing constants) in each transistor, and are incorporated in a Verilog-A module of the SA netlist [20]. The module responds to the every individual trap, and alters the transistors concerned parameters such as Vth. After inserting BTI in every transistor of the SA design, a Monte Carlo (MC) simulation is performed at different time steps (100 runs at each time step) where circuit simulator (HSPICE/Spectre) is used to investigate the BTI impact.

Output: Finally, statistical post-analysis of the results are performed for varying supply voltages, temperatures and technology nodes in MATLAB environment. The raw outputs are measured directly from HSPICE/Spectre and used to determine the sensing delay. The sensing delay metric is determined when the *trigger* signal (i.e., sense amplifier enable input signal) reaches 50% of the supply voltage and the *target* (i.e., either out or outbar falling output signal) reaches 50% of the supply voltage. The difference between the *target* and the *trigger* signals is the sensing delay as shown in Fig. 5. Furthermore, the impact of the BTI degradation is measured as the relative difference between the sensing delay with and without BTI.

B. SA offset specification

SA offset voltage is crucial for the correct operation of any SA design. In this work, three SA designs are considered and each of them requires a minimum offset voltage for its operation. In order to accurately determine the SA offset voltage, the impact of process variation on V_{TH} (which is the most critical) is determined, which is thereafter used to measure the impact on the SA offset voltage. The sigma of the V_{TH} distribution is given by:

$$\sigma_{V_{TH0}} = \frac{A_{\Delta V_{TH}}}{\sqrt{2WL}} \tag{3}$$

where $A_{\Delta V_{TH}}$ is the Pelgroms constant [18], W and L the transistor width and length, respectively. While taking this into consideration for each transistor, 100 Monte Carlo simulations are performed on each SA. The minimum offset voltage of a specific SA instance is the voltage difference between SA inputs (Bit lines) where the cross-coupled inverters of the SA remain in their metastable point. This offset voltage is

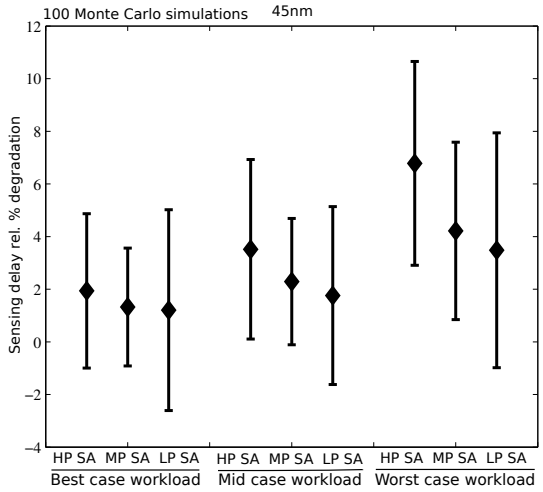

Fig. 6. BTI impact on sensing delay for three SA designs and workloads.

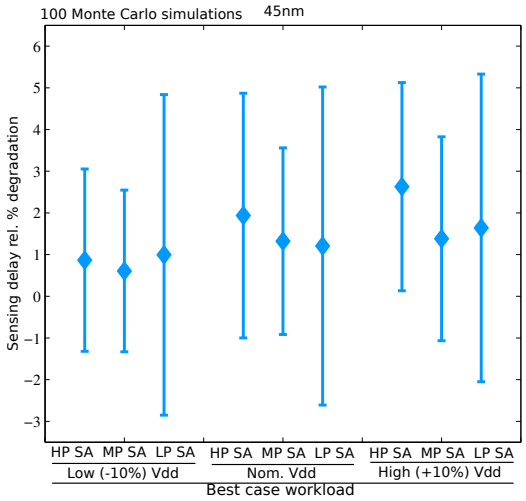

Fig. 7. Supply voltage dependent Sensing delay for best case workload.

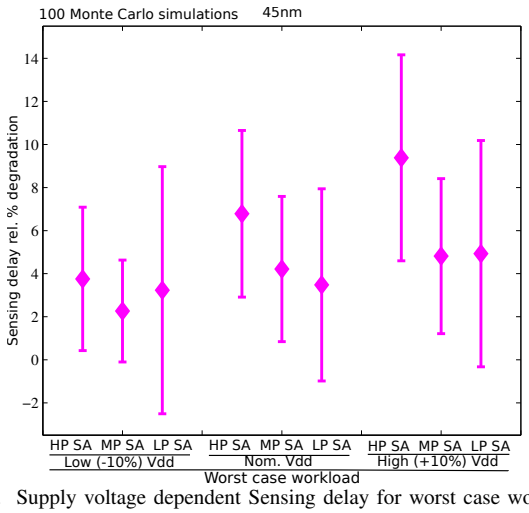

Fig. 8. Supply voltage dependent Sensing delay for worst case workload.

determined by applying a binary search on the input voltage while monitoring the SAs output. This procedure is repeated for all the Monte Carlo instantiations. Because in a good SA design, the offset voltage has nearly normal distribution, the selected SA offset voltage to achieve sufficient yield is 6σ for a 10^{-9} failure rate [7]. For our 45nm designs, we determine the offset specifications to be 89.4mV for HP SA, 104.08mV for MP SA, and 99.5mV for LP SA, while for 16nm design, the offset specification is 225.8mV for HP SA [7].

C. Experiments Performed

In this paper, four sets of experiments are performed.

1 **BTI Impact Experiments:** BTI impact on sensing delay of three SA designs and for different workloads at nominal supply voltage and nominal temperature is investigated.
2 **Supply Voltage Dependent Experiments:** BTI impact on the sensing delay for different SRAM sense amplifiers for varying supply voltages (i.e., from -10% of V_{dd} to V_{dd} and $+10\%$ of V_{dd}) and two workloads (i.e., best case and worst case) is investigated.
3 **Temperature Dependent Experiments:** BTI impact on sensing delay for different SRAM sense amplifiers for three temperatures (i.e., $298K$, $348K$ and $398K$) and two workloads (i.e., best case and worst case) is explored.
4 **Technology Dependent Experiments:** BTI impact on sensing delay for HP SA for two technology nodes (i.e., $16nm$ and $45nm$) using worst case workload is investigated.

IV. Experimental Results

This section, presents the analysis results of the experiments mentioned in the previous section.

A. BTI Impact Experiments

Figure 6 shows the relative increment of the sensing delay w.r.t. the stress time (aging), up to 3 years degradation (10^8s) for the three SA designs and the three workloads (i.e., best case, mid case and worst case). In order to quantify this delay, we simulate the initial BTI-free SA designs and use their sensing delays as references. In this paper, our analysis focus both on the average (i.e., diamond marker) sensing delay and its distribution (i.e., +/-3σ denoted by the edges of the vertical lines in the figure).

The figure shows that the degradation is strongly dependent on the design type and the workload. HP SA degrades on average faster irrespective of workloads than the MP and LP SA designs. For example after an operation of 10^8s for worst case workload, the BTI induced mean degradation is 6.8% for HP SA while 4.2% and 3.5% for MP SA and LP SA designs, respectively. In addition, the degradation is worst for worst case workload as in this case the SA is stressed most; this applies to all designs. The figure also shows that the degradation distribution maintains a distinctive behavior for each SA and workloads. LP SA degradation distribution is wider than the HP SA and MP SA for the worst case workload. For example after an operation of 10^8s for worst case workload, the BTI induced +3σ variation for LP SA is 4.5% while 3.9% and 3.4% for HP SA and MP SA designs, respectively. Besides, the same trend is observed for best case workload while for mid case workload, HP SA and LP SA BTI induced +3σ are approx. 3.4% and 2.4% for MP SA design.

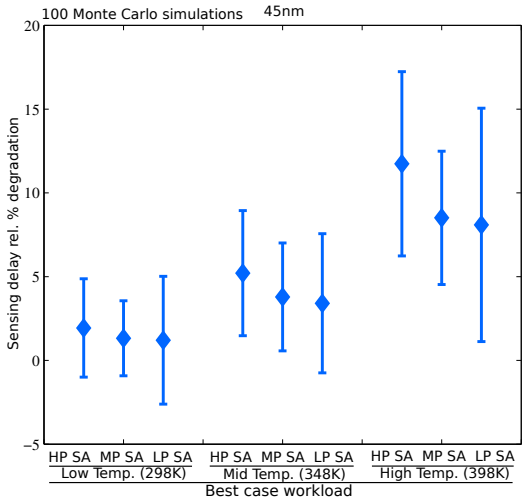

Fig. 9. Temperature dependent Sensing delay for best case workload.

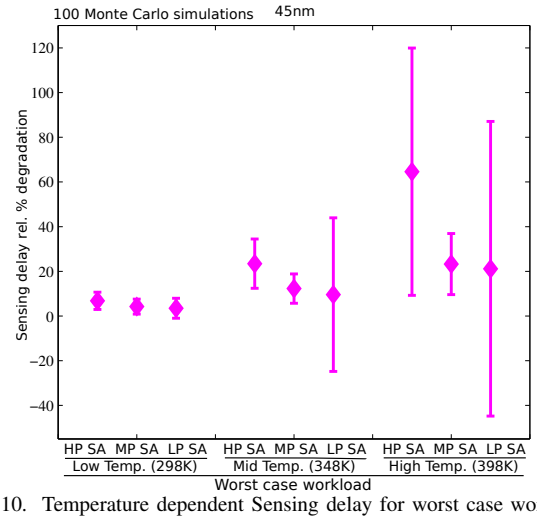

Fig. 10. Temperature dependent Sensing delay for worst case workload.

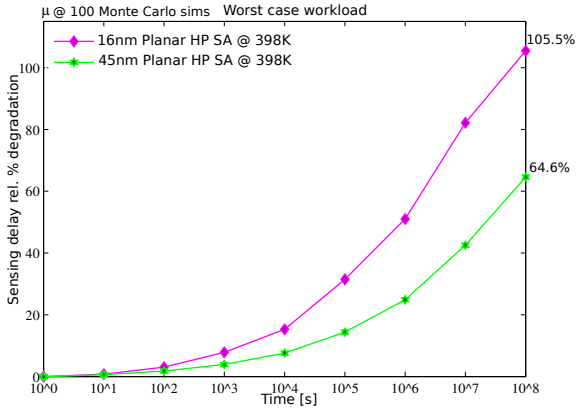

Fig. 11. BTI impact on Sensing delay for two technology nodes.

B. Supply Voltage Dependent experiments

Figures 7 and 8 depict the relative BTI induced sensing delay (i.e., average and +/-3σ variation) for the three SA designs for the various supply voltages and for the best case and worst case workloads, respectively. Note that nominal V_{dd} = 1.0V for HP SA and MP SA, while 1.1V for LP SA.

Figure 7 shows that HP SA is most sensitive to supply voltage; increasing V_{dd} from -10% to +10% leads to a 3× increase in the relative degradation. For example, after an operation of 10^8s for HP SA, the BTI induced mean degradation on sensing delay is 2.63% for +10% V_{dd}, and only 0.87% for -10% V_{dd}. However, the degradation of MP SA and LP SA are marginal. The figure also shows that the degradation distribution maintains a distinctive behavior for each SA and supply voltages. LP SA degradation distribution is the widest irrespective of the supply voltages considered, and the relative delay increment at +3σ equals (w.r.t. to average) 3.8% for 10^8s at nominal V_{dd}.
Figure 8, shows for worst case workload, similar trends as Figure 7 for the relative sensing degradation. However, the degradation is much faster (up to 4.33× faster at -10% V_{dd} to 3.57× at +10% V_{dd} for HP SA, while this is only 3.73× to 3.49× and 3.25× to 3.01× for MP SA and LP SA designs, respectively). In addition the degradation distribution is also wider (up to 1.92× wider at +10% V_{dd} to 1.52× at -10% V_{dd} for HP SA, while this is 1.47× to 1.22× and 1.42× to 1.49× for MP SA and LP SA designs, respectively).

C. Temperature Dependent experiments

Figures 9 and 10 depict the relative BTI induced sensing delay (i.e., average and +/-3σ variation) for the various SA designs and for different temperatures using the best case and worst case workloads, respectively.

Figure 9 shows that the BTI induced relative sensing delay degradation increases with increase in temperature irrespective of the design type. Moreover, HP SA degrades faster (up to 1.4× for MP SA and 1.5× for LP SA designs) at 398K. For example after an operation of 10^8s, the BTI induced mean degradation increases from 1.94% at 298K to 11.74% at 398K for HP SA, while this is only 1.32% to 8.51% and 1.21% to 8.09% for MP SA and LP SA designs, respectively. The figure also shows that the +3σ degradation distribution widens with increase in temperature irrespective of the SA design, and that the LP SA distribution is the widest at all temperatures. For example after an operation of 10^8s at 398K, the BTI induced degradation distribution is 6.96% for LP SA, while this is 5.50% and 3.98% for HP SA and MP SA designs, respectively. Figure 10 representing the results for the worst case workload shows similar trends as Figure 9. However, the degradation is much faster (up to 5.5× at 398K for HP SA). Also the degradation distribution widens (up to 10.06× at 398K for HP SA).

D. Technology Dependent experiments

Figure 11 depicts the relative BTI induced sensing delay for two technology nodes (i.e., 16nm and 45nm) for HP SA at 398K using worst case workload. Clearly, the BTI induced relative degradation increases significantly at lower nodes, leading to read failures.

Figure 12 depicts the BTI induced read failures for 16nm node for HP SA using worst case workload at 398K; the figure

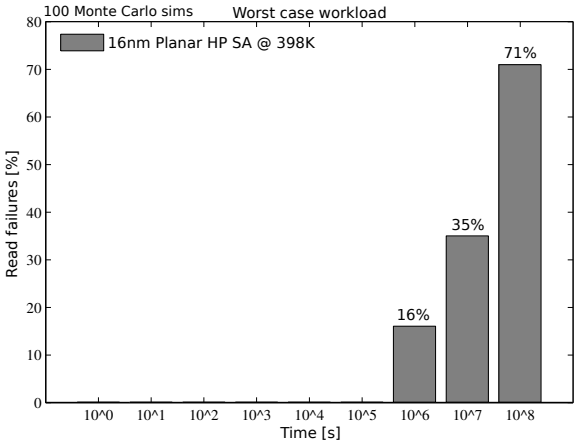

Fig. 12. BTI impact on read failures for 16nm technology node.

also shows the % of read operations that return a wrong value 1 instead of 0. Note that the sensing delay is allowed to be as much as possible. This clearly indicates that using design margin to compensate for degradation is not going to work at lower technology node. It is worth noting that no read failures were observed for 45nm node.

E. Discussion

Memory SA robustness and reliability are very crucial for the overall design of memory systems. The current analysis shows that the degradation and its distribution of each SA design is a function of supply voltage, temperature, workload and technology scaling etc. Examining the simulation results with regard to degradation and its distribution we conclude the following:

- HP SA degrades faster than other SA type regardless of the workload, supply voltage, and temperature; the degradation goes up to 65% (for the 45nm technology considered here); this indicates that BTI may be a serious concern and it may even worst for smaller technologies. Using design margin to compensate for reliability, as it is today, may not be applicable in the future any more.
- The distribution does not maintain the same trend as the degradation with regard to SA types, power, temperature, and workloads. The LP SA distribution widens more than other SA design. This implies a clear trade-off between degradation and distribution in selecting SA design that meet the reliability needs.
- The degradation worsens with scaling for HP SA which causes read failures for the worst case workload; this shows that a more effective mitigation techniques is required at lower technology node.
- The impact of aging on peripheral devices such as SA designs show that there is need to review and analyze the impact of aging on all memory parts and not only the memory cell array as it is usually the case.
- Understanding and quantifying the aging rate of the different parts of memory system is needed for reliable and optimal SRAM designs.
- Designers must be aware of both the average degradation and its distribution for all parts of a memory system (cell array, SA, decoders, write drivers, etc.) and the way they interact together to ensure correct operational life time.
- Designers urgently need to look at mitigation techniques which do take the workload, suppy voltage, temperature, and technology dependence into account.

V. Conclusion

This paper investigated the comparative study of the impact of BTI, supply voltage and temperature variation and different workloads for HP SA, MP SA, and LP SA designs for 45nm technology node. In this paper, we have shown that the sensing delay degradation is more impacted by worst case workload for the different SA design at 10^8s operational time. Increasing the supply voltage increases the BTI induced degradation in relative term while reduces in absolute terms leading to more reliable and robust sense amplifiers. Finally, an increase in temperature causes significant increase in sensing delay degradation, thereby severely impacts the reliability of the sense amplifier.

References

[1] ITRS, “International Technology Roadmap for Semiconductor 2004” ”www.itrs.net/common/2004 update/2004update.htm.”.
[2] S. Borkar, et al “Micro architecture and Design Challenges for Giga scale Integration”, *Pro. of Intl. Sympos. Micro architecture*, 2004.
[3] S. Hamdioui et al, “Reliability Challenges of Real-Time Systems in Forthcoming Technology Nodes”, *DATE*, 2013.
[4] M. A. Alam and S. Mahapatra, “A Comprehensive Model of PMOS NBTI Degradation”, *Microelectronics Reliability* , Vol:45, 2005.
[5] S. Zafar, et al, “A comparative study of NBTI and PBTI in SiO2/HfO2 stacks with FUSI, TiN gates”, *Pro. of VLSI Technology symp.*, 2006.
[6] P. Pouyan, et al, “Process Variability-Aware Proactive Reconfiguration Technique for Mitigating Aging effects in Nano Scale SRAM lifetime”, *IEEE 30th VLSI Test Symposium.*, 2012.
[7] S. Cosemans, “Variability-aware design of low power SRAM memories”, *Ph.D Thesis Katholieke Universiteit Leuven*, 2009.
[8] M. H. Abu-Rahma, et al., ”Characterization of SRAM sense amplifier input offset for yield prediction in 28nm CMOS”, *IEEE CICC*, pp.1-4, Sep. 2011.
[9] R. Menchaca, H. Mahmoodi, “Impact of Transistor Aging Effects on Sense Amplifier Reliability in Nano-Scale CMOS”, *13th Int’l Sym. on Quality Electronic Design*, 2012.
[10] I. Agbo, et al., “BTI Impact on SRAM Sense Amplifier”, *8th IDT*, 16-18 Dec. 2013.
[11] I. Agbo, et al., “Integral Impact of BTI and Voltage Temperature Variation on SRAM Sense Amplifier”, *33rd VTS*, 27-29 Apr. 2015.
[12] B. Kackzar, et al., “Disorder-Controlled-Kinetics Model NBTI and its Experimental Verification”, *IPRS* , pp: 381-387, 2005.
[13] H. Kukner et al, “Comparison of Reaction-Diffusion and Atomistic Trap-based Models for Logic Gates”, *IEEE transactions on device and materials reliability*, 2013.
[14] B. Kaczer, et al., “Origin of NBTI variability in deeply scaled pFETs”, *Reliability Physics Symposium*, 2010.
[15] S. Khan, et al, Bias Temperature Instability Analysis of FinFET based SRAM cells, *DATE*, 2014.
[16] T. Asano, et al, “Low-Power Design Approach of 11FO4 256-Kbyte Embedded SRAM for the Synergistic Processor Element of a Cell Processor”, *IEEE micro*, Oct. 2005, pp. 30-38.
[17] D. Schinkel, et al, “A Double-Tail Latch-Type Voltage Sense Amplifier with 18ps Setup+Hold Time”, *IEEE ISSCC*, 2007, pp. 314-605.
[18] M. J. M. Pelgrom, et al, “Matching properties of MOS transistors”, *IEEE J. Solid-State Circuits* , Vol. 24, no. 5, pp. 1433-1439, Oct. 1989.
[19] Predictive Technology Model ”http://ptm.asu.edu/”,
[20] B. Kaczer, et al., “Atomistic approach to variability of bias-temperature instability in circuit simulations”, *Proc. of IRPS*, April, 2011.