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Read Path Degradation Analysis in SRAM

Innocent Agbo Mottaqiallah Taouil Said Hamdioui
Delft University of Technology
Faculty of Electrical Engineering, Mathematics and CS
Mekelweg 4, 2628 CD Delft, The Netherlands
{I.O.Agbo, M.Taouil, S.Hamdioui}@tudelft.nl

Pieter Weckx[1,2] Stefan Cosemans[1] Francky Catthoor[1,2] and Wim Dehaene[2]
[1]imec vzw., Kapeldreef 75, B-3001, Leuven, Belgium
[2]Katholieke Universiteit Leuven, ESAT, Belgium
{Pieter.Weckx, stefan.cosemans, Francky.catthoor}@imec.be
wim.dehaene@esat.kuleuven.be

***Abstract*—This paper investigates the impact of aging in the read path of 32nm high performance SRAM; it combines the impact on the memory cell, on the sense amplifier, and on the way they interact. The analysis is done while considering different workloads and by inspecting both the bit-line swing (which reflect the degradation of the cell) and the sensing delay (which reflects the degradation of the sense-amplifier); the voltage swing on the bit lines has a direct impact on the proper functionality of the sense amplifier. The results show that in addition to the sense amplifier degradation, the cell degradation also contributes to the sensing delay increase; the share of this contribution depends on the cell design. Moreover, this sensing delay becomes worst at stressy workloads.**

I. Introduction

It is well recognized that technology scaling is posing major reliability challenges on electronics reliability [1–3]; e.g., it decreases their lifetime. A common practice in industry is the use of conservative guard-band and application of extra design margins to compensate for the aging impact. Accurate prediction of such impact is crucial for the realization of optimal designs. Obviously, an electronic system consists of different parts; hence, accurate aging prediction needs to consider not only *all* the different parts of the system, but also the way they *interact*, and how they all contribute to the overall degradation of the system. For instance, when it comes to SRAMs (the topic of this paper), predicting the impact of aging by only focusing on the memory array, or by only combining the individual impacts of each components, will lead to optimistic or pessimistic results.

Very limited work is published on the quantification of the degradation impact while considering all the memory components and their interactions. Li [4] analyzed the lifetime prediction of each individual transistor for the *entire* SRAM and for different reliability mechanism (i.e., HCI, TDDB, NBTI). However, this analysis did not involve the workload, which has been shown to have a large impact on the degradation rates [5]. The above clearly shows that an appropriate approach that accurately predict the impact of aging while considering all memory components, the way they interact as well as affect different workloads are required.

This paper analyzes the impact of Bias Temperature Instability (BTI) on the read path consisting of an SRAM cell and sense amplifier (SA). The analysis uses the *Atomistic Model* for aging (which is a calibrated BTI model [6–8]) and considers the *workload dependency* (as the aging variations are strongly workload dependent [5]). To measure both the impact of the cell and SA appropriate workloads are defined while using the bit-line voltage swing and SA sensing delay as metrics. The simulation model used to analyze this impact is explained next.

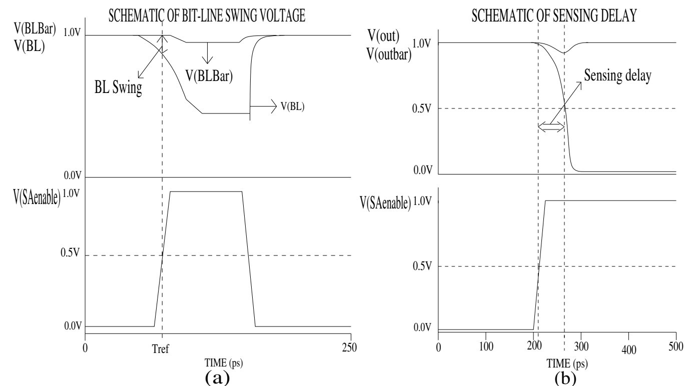

Fig. 1. Metric diagram of (a) Bit-line swing *BLS* and (b) Sensing delay *SD*.

II. Simulation model

The model comprises of precharge circuitry, 6T cell, SA precharge, and the SA. These model components *i.e., its netlists*, in addition to the BTI model *Atomistic model* explained in [6–8] are incorporated into the framework flow described in [9,10]. However, the workloads used in the model and its metrics are not described. The workloads and metrics will be explained next.

The workload sequence is assumed to be replicated until the age time is reached. To define the workloads for our analysis, we assume two extreme workloads for the cell's state: (i) 80% zero's where 80% of the cycles the cell holds a zero, and (ii) 20% zero's. Similarly, we assume two workloads for the SA: (i) 80% of the instructions are reads, and (ii) 20% of the instructions are reads. Based on this information, we derive four workload sequences for circuit simulation:

S1: denotes 20% zero's and 80% read instructions for the SA.
S2: i.e., 20% zero's and 20% read instructions for SA.
S3: i.e., 80% zero's and 80% read instructions for SA.
S4: i.e., 80% zero's and 20% read instructions for the SA.

Using the waveform of the read operation and the workload sequences, we extract duty factors for each transistors individually.

To measure the impact of BTI, the following two metrics are used.

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TABLE I
BTI IMPACT AFTER 10^8s.

Degradation component	Workload	Bit-line swing(mV)	Sensing delay(ps)
Cell-Only	20% zero	107.0	61.09
	80% zero	106.3	61.20
SA-Only	20% read instr.	111.1	61.83
	80% read instr.	111.6	65.71
Combined	S1	107.8	66.08
	S2	107.4	62.18
	S3	107.1	66.21
	S4	106.7	62.29

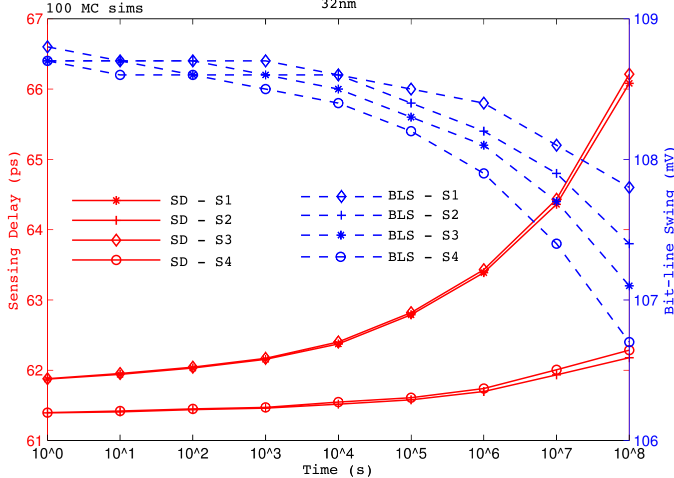

Fig. 2. BTI impact for the four workload sequences.

Bit-line swing: The bit-line swing *BLS* specifies the voltage difference between bit-lines (see Fig. 1a) at a fixed reference time T_{ref}; i.e., the time where the up transition of the sense amplifier enable signal reaches 50% of the supply voltage as shown in Fig. 1a.

Sensing delay: The sensing delay *SD* is the time required for the SA to complete its operation; it is the time between the sense enable activation (i.e., when the up transition reaches 50% of the supply voltage) and the falling output signal of the SA (i.e., when the down transition reaches 50% of V_{dd}) as depicted in Fig. 1b.

III. Experimental Results

Table I shows the results for the three cases for a stress period of 10^8s; the first column presents the simulated case. 'Cell-Only' denotes the case when only the cell is impacted by BTI, 'SA-Only' when only the SA is impacted, and 'Combined' when both the cell and SA degrade due to BTI. Note that in case of 'Cell-Only', both the bit-line swing (*BLS*) and the sensing delay (*SD*) are affected, while in the case of *SA-Only*, the *SD* is impacted (i.e., the *SD* may increase due to slow bit-line swing development or slow SA) while the *BLS* should not be affected. The table reveals the following for the different cases.

For the case Cell-Only, the BLS is marginal dependent on the workload, resulting in almost no impact on the SD. This can be explained by the fact that the pull-down transistors of the cell used for this design are very strong. We will assume SD=61.09ps as the baseline.

For the case SA-Only, the cell is not suffering from BTI; hence, it is not affected and is about 111mV. The SD, however, is affected and increases for more stressy workloads. The SD at 80% read instructions is 6% higher than at 20% reads for which the SD is just 1% more than the baseline.

For the case 'Combined', although the BLS is reduced as compared with the a-fresh cell (see SA-Only case), the dependency of BLS on the workload is marginal due to the chosen design as already mentioned. However, as can be predicted, the results show clear dependency of the SD on the workload; the SD is higher for sequences S1 and S3 which both have 80% read instructions for the SA. At 80% read instructions (S1 and S3), the SD is also 6% higher than at 20% read instructions (S2 and S4); in the latter case the SD is about 2% more than the baseline. Note that the *relative* increase due to workload is the same as for SA-Only' case.

Figure 2 shows how BLS and SD evolve over time for a duration of 3 years degradation (i.e., 10^8s) for the case 'Combined'; each point in the graph corresponds to the average of 100 Monte Carlo simulations. The figure clearly confirms the conclusions extracted from Table I, and that (although in terms of absolute number of our case study the difference are not so big), *the slowest SD* is obtained when *both* the degradation of the cell and the SA are considered. Note that the SD tends to grow very fast when the operational lifetime gets closer to 3 years (10^8s).

IV. Conclusions

In conclusion, to ensure correct operational lifetime, designers must be aware about how the different parts of the memory degrade, how their interactions contribute to the degradation, and how all of these determine the overall degradation. This will allow for better design margin optimization. Note that in our analysis zero-time variations (process variations) are not taken into account due to the model limitation.

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