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Quantification of Sense Amplifier Offset Voltage Degradation due to Zero- and Run-time Variability

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***Abstract*—Nowadays, typical (memory) designers add design margins to compensate for uncertainties; however, this may be overestimated leading to yield loss, or underestimated leading to reduced reliability designs. Accurate quantification of all uncertainties is therefore critical to provide high quality and optimal designs. These uncertainties are caused by zero-time variability (due to process variability), and by run-time variability (due to environmental variabilities such as voltage and temperature, or due to temporal variability such as aging). This paper uses an accurate methodology to predict the impact of both zero- and run-time variability on the offset voltage of sense amplifiers while considering different workloads and PVT variations for a pre-defined failure rate. The results show a marginal impact of environmental run-time variability on the offset specification when considering zero-time variability only, while this becomes significant (up to 2×) when incorporating aging run-time variability. The results can be used to quantify whether the required offset voltage is met or not for the targeted lifetime; hence, enable the designer to take appropriate measures for an efficient and optimized design, depending on the targeted application lifetime.**

***Index Terms*—Offset voltage, zero-time variability, run-time variability, SRAM sense amplifier**

I. Introduction

In recent decades, CMOS technology has been sustained with aggressive downscaling that poses major challenges on the reliability of devices [1–3]. The sources of this unreliability in todays technologies are mainly caused due to variability during manufacturing or at run-time [1]. As a result of the manufacturing process, devices will suffer from process variations, which changes the properties of the manufactured devices from the targeted ones. Hence, similar manufactured devices end up having different characteristics, referred to as *process* or *time-zero variation*. On the other hand, *run-time variations* cause the device properties to change and/or degrade during their operational lifetime. Such variations are mainly due to *environmental variations* such as supply voltage fluctuations and temperature variations, and *temporal* or *aging variations* such as *Bias Temperature Instability* [4]; both show a severe impact with CMOS scaling [1]. All these variations cause the devices to behave differently than intended, which may cause the devices (or circuits) to fail if appropriate measures are not taken. Designers usually use a conservative guardbanding and apply extra design margins [5] to ensure the correct operation for the worst-case variations during the targeted circuit lifetime. However, a pessimistic guardbanding leads to either yield or performance loss, while an optimistic guardbanding increases the test escapes and in-field failures. Therefore, an *accurate* estimation of the impact of *all kinds of* variations at circuit level (and also at the architecture level) is needed to obtain a high quality and optimal design. In this paper, we focus on the estimation of sense amplifier (SA) offset voltage using the integral impact of process and run-time variations, especially investigating the contribution of run-time variability due to aging to the overall impact as compared with zero-variability and environment variability; this guides the designers to optimize the guardbands and margins depending on the targeted product quality and application lifetime. Note that the SA delay, which is an integral part of the path delay and strongly related to the offset-voltage, plays a key role in defining memory design margins. For a fixed sensing delay, the higher the offset the more time needed for the read operation, as more time will be needed to discharge one of the cell's bitlines.

Only limited work has been presented for the characterization of the offset voltage in SAs. In [6], the authors presented a tunable SA to cope with with-in die variations; the authors estimated the offset voltage at design time based on process variations. In [7], the authors characterize the SA Input Offset by a physical circuit monitoring (implemented in real silicon) in order to estimate the yield. In [8], the authors presented a scheme to determine the signal margins for DRAM SAs based on offset distribution measurements. Prior work mainly focused on time-zero variation. Methods to estimate the SA offset voltage in the presence of both manufacturing and run-time variability at design stage are still missing.

This paper uses an *accurate* method to estimate the impact of *variability* on the SRAM sense amplifier *offset-voltage*, while considering *both process and run-time variation*. To the best knowledge of the authors, this is the first work to determine the SA offset in the presence of all kind of variability. The used method is accurate in the sense that it uses the *Atomic Model* for aging (which is a calibrated model [9,10]) and considers the *workload dependency* (as the aging variations are strongly workload dependent [11,12]). Guaranteeing a resilient SA requires not only a

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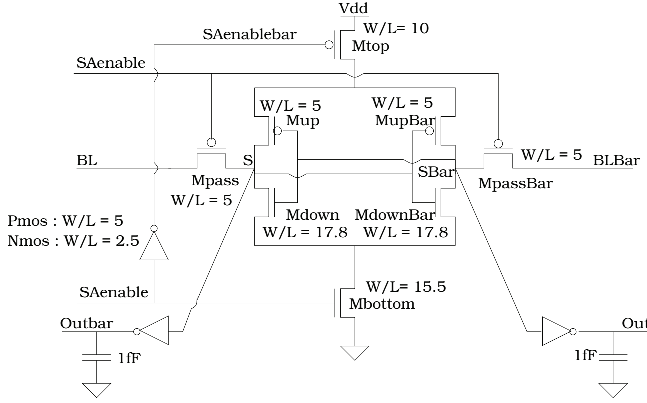


Fig. 1. Standard latch-type Sense Amplifier

correct sensing delay, but also an appropriate offset-voltage during the memory operational lifetime. The results show incorporating the run-time variability due to the aging in the estimation worsens the impact on the offset-voltage with a factor 2 at least.

The rest of the paper is organized as follows. Section II provides a background w.r.t. the targeted standard latch-type sense amplifier and variability sources. Section III provides the proposed methodology for offset voltage quantification. Section IV analyzes the results. Finally, Section V concludes the paper.

II. Background

First the standard latch-type sense amplifier is presented, and thereafter, the sources of variability considered in this paper are discussed.

A. Sense Amplifier

Figure 1 depicts the structure of the Standard latch-type Sense Amplifier; it is responsible for the amplification of a small voltage difference between BL and BLBar during read operations. The operation of the sense amplifier consists of two phases. In the first phase, when SAenable is low, the access transistors Mpass and MpassBar connect to the BL (BLBar) with the internal nodes S (Sbar). In the second phase, when SAenable is high, the pass transistors disconnect the BL (BLBar) input from the internal nodes. The cross coupled inverters get their current from Mtop and Mbottom and subsequently amplify the difference between S and Sbar and produce digital outputs on Out and Outbar. The positive feedback loop ensures low amplification time and produces the read value at its output.

B. Variation sources

The four sources of variability investigated in this paper are briefly described next.

Process variations: These affect the circuit at time $t = 0$ and consist of variations in several parameters including effective channel length (L), oxide thickness (t_{ox}), dopant concentration (N_a), and transistor width (W). There are two sources of variation, i.e., systematic and random variation. We focus only on random process variation. It can be described by a probability distribution and can be modeled by V_{th} variation. The standard deviation of the V_{th} shift is given by:

$$\sigma_{V_{TH0}} = \frac{A_{\Delta V_{TH}}}{\sqrt{2WL}} \quad (1)$$

where $A_{\Delta V_{TH}}$ is the Pelgrom's constant [14], W and L the transistor width and length, respectively.

Temperature variation: They impact the operating condition of MOS transistors. The dependence of threshold voltage and temperature is given by [24].

$$V_{th} = C_{vt} - \frac{Q_{ss}}{C_o} + \Phi_{ms} \quad (2)$$

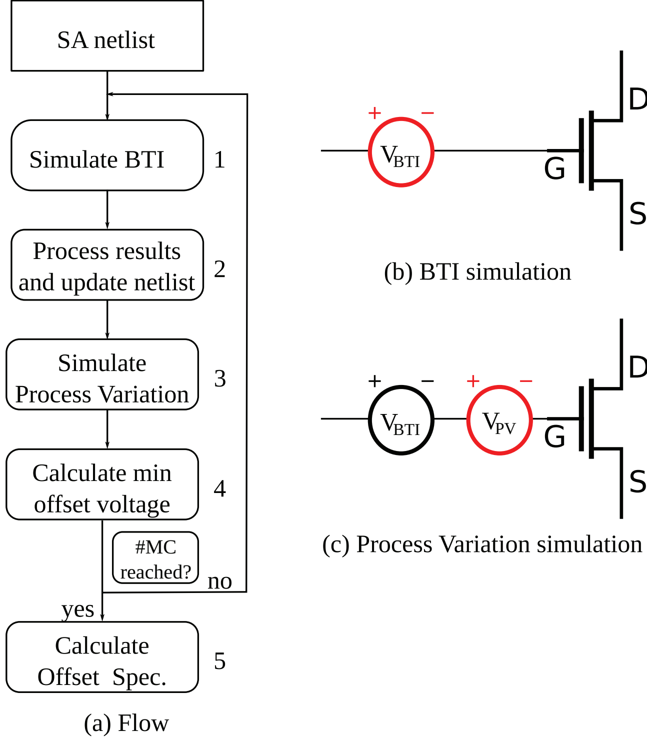
where C_{vt} is a constant that represents the fermi potential, surface charge Q_{ss} at the Si-SiO_2 interface, gate oxide capacitance C_o and work function difference Φ_{ms} is a function of the temperature [24].

$$\Phi_{ms} = -0.61 - \Phi_F(T) \quad (3)$$

Here Φ_F(T) is Fermi potential. Expression (3) shows that work function difference reduces with respect to increase in temperature and therefore leads to a threshold voltage decrement.

Supply voltage variation: Supply voltage fluctuations affect the operating speed of MOS transistors. The variation in switching activity across the die/circuitry leads to an uneven power/current demand and may lead to logic failures [13]. Furthermore, transistor subthreshold leakage variations impact the uneven distribution of supply voltage across the circuitry as well [13]. Hence, reducing the supply voltage degrades the performance of the circuit/transistors and raising supply voltage compensates/enhances the performance and significantly reduces circuit failure rates as a result of variability [13].

Aging Variations: There are different aging mechanisms such as Bias Temperature Instability (BTI) [4], Hot Carrier Injection [15], and Time Dependent Dielectric Breakdown [16]; BTI is considered to be the most important of them; therefore it is the focus of this paper. BTI has two main components i.e., Negative (BTI) and Positive (BTI). Atomistic model is proposed to accurately model BTI [9]; it induces threshold voltage variation for time $t > 0$ and is based on the capture and emission of single traps during stress and relaxation phases of NBTI/PBTI, respectively. The threshold voltage shift of the device ΔV_{th} is the accumulated result of all the capture and emission of carriers in gate oxide defect traps. The probabilities of the defect occupancy in case of capture P_C and emission P_E are defined by [18] as:



(a) Flow

(b) BTI simulation

(c) Process Variation simulation

Fig. 2. Offset voltage specification flow.

$$P_C(t_{STRESS}) = \frac{\tau_e}{\tau_c+\tau_e}\left\{1 - exp\left[-(\frac{1}{\tau_e}+\frac{1}{\tau_c})t_{STRESS}\right]\right\} \quad (4)$$

$$P_E(t_{RELAX}) = \frac{\tau_c}{\tau_c+\tau_e}\left\{1 - exp\left[-(\frac{1}{\tau_e}+\frac{1}{\tau_c})t_{RELAX}\right]\right\} \quad (5)$$

where τ_c and τ_e are the mean capture and emission time constants, and t_{STRESS} and t_{RELAX} are the stress and relaxation periods, respectively. Furthermore, BTI induced V_{th} is an integral function of capture emission time map, workloads, duty factor and transistor dimensions, which gives the mean number of available traps in each device [11]; the model also incorporates the temperature impact [9,10].

III. Proposed Methodology

Figure 2(a) depicts a generic flow to determine the offset voltage specification. It consists of five steps. The first four steps are based on 400 Monte Carlo simulations and are repeated for each experiment. Step 5, the offset specification is based on the entire population. Each of the steps is described next in more details.

1. Simulate BTI: We use the approach in [19] to perform the BTI simulations; they are based on the model described in Section II. The simulations are controlled by a Perl script that generates an initial instance of the BTI augmented SRAM sense amplifier design, based on transistor dimensions, stress time, duty factor and frequency. Every generated instance has a distinct number of traps (with their unique timing constants) in each transistor, and are incorporated in a Verilog-A module of the SA netlist. The module responds to the every individual trap, and alters the transistors concerned parameters. All these parameters can be effectively modeled by a voltage source (the so called BTI-induced threshold voltage) as shown in Figure 2(b). The severity of the BTI impact depends on the workload, temperature, etc. The workload sequence is assumed to be replicated once completed until the age time is reached. Based on the workload, we extract individual duty factors for each transistor based on the waveforms and workload sequence. This enhances the accuracy of our simulation results.

2. Process results and update netlist: In this step, the BTI induced V_{th} shifts of each individual transistor are extracted from the previous step and injected as a voltage source to the netlist. Note that due to the stochastic nature of BTI, each instantiation will have different threshold voltage shifts.

3. Simulate process variations: The next step simulates the process variations as shown in Figure 2(c). Here we follow the same approach as in [6] where the time zero V_{th} variations are modeled by voltage sources. We use the build-in Monte Carlo simulations in Spectre [20] to create a normal distribution for each transistor with a zero mean and a sigma expressed by Equation 1.

4. Calculate minimum offset voltage: The SA offset voltage is crucial for the correct operation of any SA design. The minimum offset voltage of a specific SA instance is the voltage difference between SA inputs (Bit lines) where the cross-coupled inverters of the SA remain in their metastable point. This minimum offset voltage is determined by applying a binary search on the input voltage and is affected by process, temperature, voltage and aging variations.

5. Calculate offset specification: The offset specification of the SA is calculated based on 400 Monte Carlo samples and depends on the desired failure rate or yield. In a good SA design, the offset voltage has a nearly normal distribution and therefore the relation between this distribution and failure rate can be summarized as:

$$\int_{V_{in}=-V_{Offset}}^{V_{Offset}} \mathcal{N}(\mu_{MC}, \sigma_{MC}) = 1 - f_r \quad (6)$$

In this equation, V_{in} presents the input voltage of the SA, V_{offset} the offset voltage specification, $\mathcal{N}$ a normal distribution of the offset voltages obtained from step 4, μ_{MC} and σ_{MC} their mean and standard deviation, and f_r the failure rate. The equation states that all SA instantiations that require an offset outside the range [-V_{offset} , +V_{offset}] result in failures. The objective is to find the SA offset specification V_{Offset}. At time t=0, this equation can be solved as follows [21]:

$$V_{Offset} = |normvinv(\tfrac{f_r}{2}, \mu_{MC} = 0, \sigma_{MC})| = f(f_r) \cdot \sigma_{MC} \quad (7)$$

In this equation, $norminv$ presents the normal inverse cumulative distribution function which provides the offset voltage for a given f_r, μ_{MC}=0 and σ_{MC}. The equation can be simplified as shown at right-hand side; here f is a function that presents a constant depending on f_r. In this work we assume a constant failure f_r=10^{-9} leading to $f(f_r)$=6.1; therefore, for time t=0 we obtain $V_{Offset} = 6.1 \cdot \sigma_{MC}$. The right-hand side of Equation 7 is only valid when $\mu_{MC} = 0$. However, depending on the workload for time t>0 aging can shift this distribution (i.e., have a non-zero mean); this invalidates Equation 7. As a consequence, we determine V_{Offset} directly from Equation 6 by solving this equation numerically.

IV. SIMULATION RESULTS

In this section, we present the performed experiment, and the obtained results.

A. Experiments Performed

In order to investigate the impact of both zero-time variability and run-time variability, we performed two sets of experiments.

- **Process variation (PV):** In this experiment the impact of process variation is analyzed, while considering first the voltage variations (i.e., -10% V_{dd}, nom. V_{dd}=1.0V, and +10% V_{dd}) and thereafter the temperature variations (i.e., 298K, 348K, and 398K).
- **Process and aging variation:** In this experiment, we analyzed the combined effect of both time-zero and aging variability; also here the experiments are performed for different voltages and temperatures. Moreover, all these experiment are done while considering three different workloads in order to show the dependency on the run-time applications. We assume that 80% of the executed instructions (e.g., by a CPU) are read instructions (which activate the SA). In addition, we define three sequences to present the 80% of the reads: {r0} (all the reads are 0), {r1} (all the reads are 1) and {r0r1} (50% {r0} and 50% {r1}). Note that the aging variability is workload dependent, while PV is not.

B. Simulation Results

Process variability: The results of the process variation for different voltages and temperatures are explained next.

- **Voltage Dependency:** Figure 3 shows the offset voltage distribution for the three supply voltages at nominal temperature at time-zero. The figure shows that the offset distributions are similar and that the impact of voltage variations is *marginal* (less than 5%). For example, w.r.t. nominal V_{dd} a reduction of 4.2% is observed for +10% V_{dd}, while an increase of 2.5% for -10% V_{dd}.
- **Temperature Dependency:** Figure 4 shows the offset voltage distribution for the three temperatures at nominal voltage at time-zero. The figure shows that the offset voltage distributions are nearly the same; hence the impact of temperature variations on the voltage offset is *marginal*. For instance, the offset specification is 90.2mV at 298K while 93.6mV at 398K (an increase of only 3.8%). Note that the mean in Figs. 3 and 4 should ideally be zero; a small error (worst case of 0.19mV) occurs due to the Monte Carlo simulations.

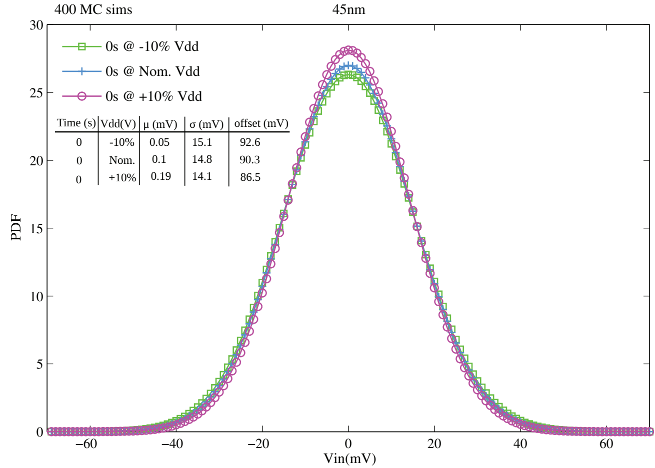


Fig. 3. Supply voltage impact at time-zero.

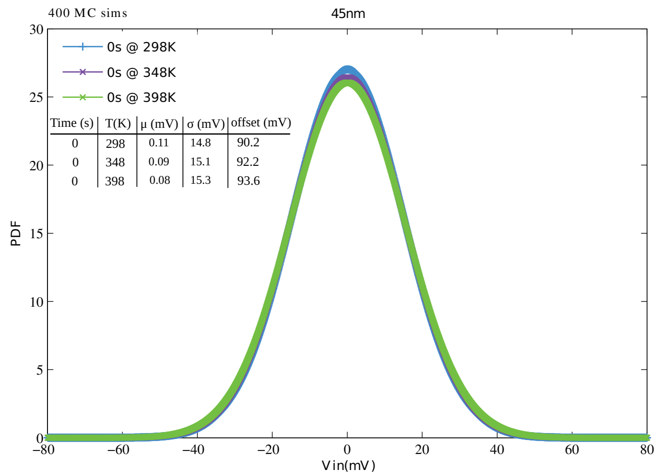


Fig. 4. Temperature impact at time-zero.

Process and aging variability: The results of the voltage and temperature experiments done for both process and aging variations are provided next.

- **Voltage Dependency:** Fig. 5 shows the voltage dependency of the offset voltage for different workloads at 298K. In addition to the baseline plot (time-zero variability), the figure depicts 6 plots: 2V_{dd}'s (-10% and +10%) × 3 workloads; the plots for nominal V_{dd} are not included for clarity. However they are added to Table I, which presents the information of Fig. 5 in another format; the

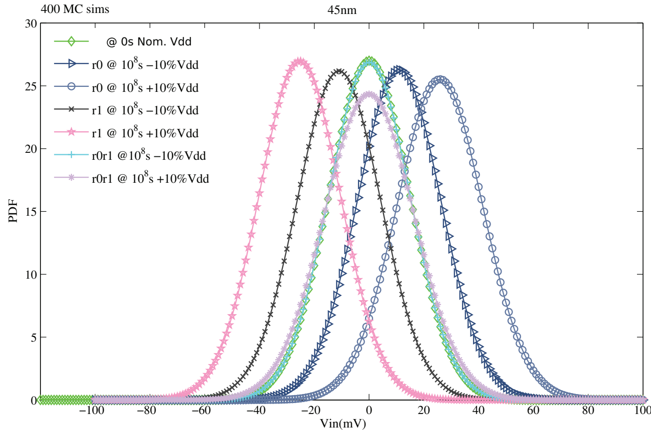


Fig. 5. Voltage impact at run-time.

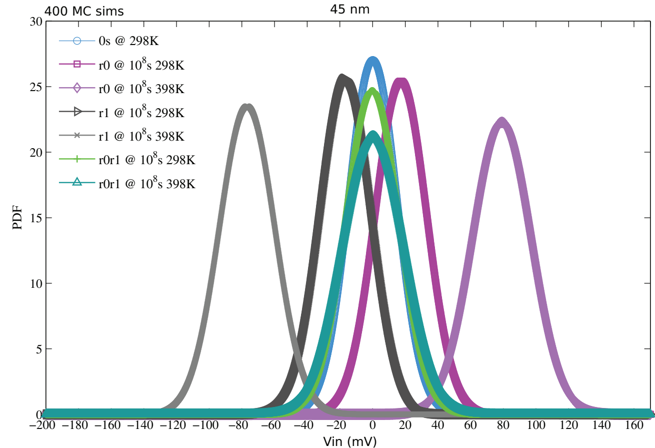


Fig. 6. Temperature variation at run-time.

TABLE I
VOLTAGE IMPACT AT RUN-TIME.

Aging(s)	Workload	Vdd. (V)	μ (mV)	σ (mV)	offset (mV)
0	–	Nom.	0.1	14.8	90.3
10^8	{r0}	−10%	11	15.2	102.0
10^8	{r0}	Nom.	17.3	15.7	111.6
10^8	{r0}	+10%	25.8	15.6	119.5
10^8	{r1}	−10%	-11	15.2	102.4
10^8	{r1}	Nom.	-17.2	15.6	110.6
10^8	{r1}	+10%	-25.3	14.8	114.0
10^8	{r0r1}	−10%	-0.09	14.8	90.6
10^8	{r0r1}	Nom.	-0.2	16.2	98.8
10^8	{r0r1}	+10%	-0.001	16.4	100.0

TABLE II
TEMPERATURE VARIATION AT RUN-TIME.

Aging(s)	Workload	Temp. (K)	μ (mV)	σ (mV)	offset (mV)
0	–	298	0.1	14.8	90.3
10^8	{r0}	298	17.3	15.7	111.5
10^8	{r0}	348	45.0	16.8	145.6
10^8	{r0}	398	79.1	17.9	186.5
10^8	{r1}	298	-17.2	15.6	110.6
10^8	{r1}	348	-44.2	16.3	142.0
10^8	{r1}	398	-76.8	17.0	178.6
10^8	{r0r1}	298	-0.2	16.2	98.8
10^8	{r0r1}	348	-0.02	17.5	107.1
10^8	{r0r1}	398	0.2	18.8	114.8

μ, σ and the offset voltage are also included. Note that the offset voltage distribution for {r0r1} at -10%V_{dd} is almost the same as the baseline, hence they are coincident. The figure shows that depending on the workload, the offset distribution may shift to the left or right; workload {r1} causes a shift to the left, {r0} to the right, while {r0r1} has a nearly zero mean (slight error due to Monte Carlo simulations). This can be explained by the way the workload stresses the SA devices (see Fig. 1); e.g., {r0} stress the transistors Mdown and MupBar of the cross-coupled inverters all the time, {r1} stresses the other devices of the inverters, while {r0r1} balances the stress on all devices.

Moreover, the figure shows that a voltage increase severes the shift as it accelerates the BTI mechanism. Note that although at time 0 the voltage impact is marginal (see Fig. 3), the accelerated aging due to voltage is more significant. For example, for {r0} at nominal V_{dd}, a 17.3mV shift is observed, while this is 25.8mV for +10% V_{dd} (see Table I). A second observation from the figure and table reveals that the σ *increases* with aging, even if balanced workload {r0r1} is applied. Both the average shift and increase in σ lead to *much higher offset requirement*. For example, at nominal V_{dd}, the required offset voltage is only 90.3mV when zero-time variability is considered; however, this is 111.6mV (which is an increase of 24%) when {r0} is applied and run-time variability is considered. It is worth noting that applying a balanced workload {r0r1} results in an offset specification of 98.8mV (which is only an increase of 9.4%); this indicates the importance of balanced workload for optimal designs.

- **Temperature Dependency:** Fig. 6 shows the temperature dependency of the offset voltage at nominal V_{dd}. In addition to the baseline plot (time-zero variability), Fig. 6 depicts 6 plots: 2 temperatures (298K and 398K) $\times$ 3 workloads; the plots for temperature 348K are not included for clarity. However, they are included in Table II. The figure shows similar trends as in Fig. 5, but the impact is more severe.

  The offset specification is strongly dependent on both the workload and temperature. The shift for *unbalanced workload* is *significant*, while this is very marginal for balanced workload. The higher the temperature, the larger the shift. E.g., at T = 398K, the {r0} causes an offset voltage shift of 79mV! This is 76% more than the shift at T = 348K. Another important observation is that irrespective of the workload, the required offset voltage is higher when considering run-time variation. Obviously,

the offset voltage increase is much higher for unbalanced workloads and higher temperatures.

Moreover, the figure and table show that σ increases with temperature for all workload. Both the mean shift and standard deviation lead to *much higher offset voltage specification* irrespective of the workload; the higher the temperature, the higher the required offset voltage. E.g., the offset specification at T = 298K is just 90.3mV when only zero-time variability is considered, while this is 186.5mV (i.e., an increment of 106.5%!) at 398K for workload {r0}. Note that applying a balanced workload minimizes the impact; e.g., an offset specification of 114.8mV (this is up to 27.1%) is obtained at 398K when {r0r1} is applied.

C. Discussion

The proposed methodology for offset voltage quantification is unique not only in the sense that it uses an accurate BTI model and involves the workload dependency, but also because it involves both the zero-time variability as well as run-time variability. The obtained results clearly show that using only environmental run-time variability while considering zero-time variability analysis is not accurate enough. The offset voltage difference between time-zero and run-time variability can be as big as a factor of two.

Moreover, the dependency of offset voltage on workload (application) has been shown to be significant. Applying balanced workload results in reduced impact. Hence, thinking about incorporating some features in the circuits to internally create a balance workload during the lifetime of the application is important for optimal and reliable designs. Schemes such as bit-flipping [23] can be useful.

Finally, it is worth noting that the presented methodology of Figure 2 can be extended to any digital circuit, as long as there is a clear metric (such as offset specification) to be evaluated. For example, the critical paths in a pipeline stage can be evaluated based on the path delay metric.

V. Conclusion

This paper used an accurate offset voltage quantification method for the sense amplifier, considering both time-zero and run-time variability; the method takes into consideration process, voltage, and temperature variations, as well as degradation due to aging. The method incorporated also the workload dependency. The results showed a marginal impact of temperature and voltage on offset specification when considering process variability only, while this becomes more significant (up to 2×) when adding the run-time variability due to aging. Hence, ignoring the run-time variability is not suitable for a reliable and robust design. The proposed method gives designers a better way of determining the offset voltage specification which reduces the probability of having over- or under-design margins.

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