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Analysis of the impact of spatial and temporal variations on the stability of SRAM arrays and the mitigation technique using independent-gate devices

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HIGHLIGHTS

- We improved the NBTI induced Vth degradation model with process variations included.
- We analyzed the impact of Vth variations of different SRAM cell transistors.
- We extended the Vth mitigation technique to compensate Vth variations.
- We updated the IDDQ estimation model to capture the NBTI induced degradation.

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ABSTRACT

As planar MOSFET is approaching its physical scaling limits, FinFET becomes one of the most promising alternative structure to keep on the industry scaling-down trend for future technology generations of 22 nm and beyond. In this paper, we investigate the influence of NBTI degradation induced variation and random process variations on the stability of the FinFET-based 6T-SRAM cell. The contributions of transistor threshold voltage variation ΔV_{th} on the stability of the SRAM cell and the corresponding compensating bias schemes are thoroughly examined by means of SPICE simulations. A mitigation method for memory stability management under spatial and temporal variations is demonstrated by taking advantage of the independent-gate FinFET device structure in order to perform threshold voltage adjustment. The proposed technique allows for a practical compensation strategy able to preserve the SRAM cell stability while balancing performance and leakage power consumption. We demonstrate that the standby leakage current I_{DDQ} value can be utilized to assess the consequences of parameter variations and NBTI on the circuit performance and propose a model that captures this. We evaluate the impact of our proposal on the SRAM cell stability by means of SPICE simulations for 20 nm FinFET devices. Simulation results indicate that the proposed technique can effectively maintain stability of an SRAM array within the desired range during its operational life under both spatial and temporal variations, hence improve the system performance and reliability. Our method allows for maintaining the Static Noise Margin (SNM) degradation of SRAM cells under a certain range, e.g., 2% of fresh device after 1 year operation, which is about 55.56% improvement when compared with the 4.5% degradation corresponding to the uncompensated case.

1. Introduction

As technology scaling continues, the Integrated Circuits (ICs) feature size has been driven into the physical limitation edge of conventional MOSFET devices [5]. In order to keep technology scaling down further, two major issues have to be properly addressed: (i) the excessive leakage power, and (ii) the device/circuit reliability. Given that those issues have to be dealt with in the context of uncontrollable statistical process variations, the continuation of technology scaling seems to be more difficult than ever.

In order to keep on the industry scaling-down trend, novel devices and structures were proposed as potential candidates to replace the conventional planar MOSFET device [5,15]. Among these devices, FinFET seems to be the most promising alternative structure for future technology generations of 22 nm and beyond, owing to its fabrication process simplicity and good electrical characteristics [15]. Due to its structure consisting of single/multiple vertical fin(s) FinFET has better electrostatics on Short-Channel Effect (SCE), thus less static leakage current and power consumption.

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However, FinFET is also sensitive to temporal degradation mechanisms, e.g., Negative Bias Temperature Instability (NBTI), Hot Carrier Injection (HCI) etc. In other words, on top of the spatial uncertainty caused by process variations, also for FinFET various temporal degradations hold back the feature size of technology from further scaling.

In view of the previous argument, in this paper, we address the following aspects: (i) the modeling of SRAM cell stability under spatial and temporal V_{th} variations induced by process variation and NBTI stress; (ii) the dynamic characterization of NBTI induced V_{th} degradation by monitoring the supply leakage current I_{DDQ}, and (iii) performance, e.g., SRAM cell stability measured by the Static Noise Margin (SNM), mitigation methods able to compensate the effects of process variations and NBTI by taking advantage of the FinFET's special device structure.

We evaluated our proposal by SPICE simulations for 20 nm FinFET devices, and our results indicate that the proposed technique can effectively maintain stability of SRAM array within the desired range during its operational life under both spatial and temporal variations. For example, our method allows for maintaining the SNM degradation of FinFET SRAM cells under 2% of the fresh device SNM after 1 year operation, which is about 55.56% improvement when compared with the 4.5% SNM degradation corresponding to the uncompensated case.

The rest of this paper is organized as follows: In Section 2 we introduce the temporal V_{th} degradation induced by NBTI under dynamic stress; In Section 3 we analyze the impact of V_{th} variations caused by process variations and NBTI degradation on the stability of SRAM cells; In Section 4 we propose a V_{th} compensation technique using independent double-gate FinFET to improve SRAM's stability and the proposed scheme is evaluated in Section 5 by means of SPICE simulations; In Section 6 we concludes our work.

2. Temporal and spatial V_{th} variations

The Negative Bias Temperature Instability (NBTI) phenomenon and its consequences have been extensively studied [14,2,3] and there is clear indication that NBTI caused degradation is becoming a major reliability concern for nanoscale CMOS technology. NBTI is prominent in PMOS devices and it causes a threshold voltage (V_{th}) shift, which results in poor drive current and in shorter device and by implication circuit lifetime.

NBTI occurs along the entire transistor channel at elevated temperature when negative gate-to-source voltage is applied. Holes from the inversion layer can tunnel into the gate oxide, break the Si–H bond leaving behind an interface trap, which results in a positive V_{th} shift. Traditionally, the interface trap generation is modeled within the Reaction–Diffusion (R–D) framework [2], which gives a power-law time evolution of V_{th} degradation. A long-term V_{th} shift under dynamic stress is given by [3]:

$$\Delta V_{th} = At^n = \left(\frac{\sqrt{K_v^2 \alpha T_{clk}}}{1-\beta_t^{1/2n}}\right)^{2n}, \tag{1}$$

where $n = 1/6$ is the power-law time constant, T_{clk} is the clock period, α ($0.1 \le \alpha \le 0.9$) is the NBTI stress probability, i.e., the NBTI duty-cycle. β_t is a coefficient reflecting the NBTI recovery effect and is computed as follows:

$$\beta_t = 1 - \frac{2\xi_1 t_e + 2\sqrt{\xi_2 C(1-\alpha)T_{clk}}}{2t_{ox} + \sqrt{Ct}}, \tag{2}$$

where ξ_1, ξ_2, and C are fitting constants, t_{ox} is the oxide thickness, t_e is the effective diffusion distance of hydrogen species. K_v stands for technology, supply voltage, and operating temperature dependence associated with NBTI degradation. At its turn K_v is computed as [3]:

$$K_v = \left(\frac{qt_{ox}}{\epsilon_{ox}}\right)^3 K_1^2 C_{ox}(V_{gs} - V_{th})\sqrt{C}\exp\left(\frac{2E_{ox}}{E_0}\right), \tag{3}$$

where q, k, ϵ_{ox}, K_1, C_{ox}, V_{gs}, E_{ox}, and E_0 are the elementary charge, Boltzmann's constant, oxide permittivity, constant factor, oxide capacitance per area, gate–source voltage, vertical oxide field, and fitting constant, respectively.

Apart of NBTI, the V_{th} is also influenced by Process Variations (PV), which induce spatial uncertainties on the device performance relevant parameters. Process variations become particularly important in smaller technology nodes (< 65 nm) as when the feature size is scaling down the variation consequences are becoming more significant and have larger impact on device size and performance. Process variations are typically divided into two components: (i) inter-die (global), which accounts for chip- or wafer-level variations and (ii) intra-die (local), which accounts for variations between different devices in the same die.

For simplicity, we assume that the PV-induced ΔV_{th} is static and the time evolution of V_{th} can be expressed as follows:

$$V_{th} = V_{th0} + \Delta V_{th}^g + \Delta V_{th}^l + \Delta V_{th}^{nbti}(t), \tag{4}$$

where V_{th0} is the nominal V_{th} value, ΔV_{th}^{nbti} is the NBTI-induced V_{th} degradation, and ΔV_{th}^g and ΔV_{th}^l are V_{th} alterations due to global and local variations, respectively.

As device dimension scale down into nanometer region, Random Dopant Fluctuation (RDF) becomes one of the major variations affecting the performance of device. RDF directly affects the threshold voltage of a MOSFET, since V_{th} depends on the charge of the ionized dopants in the depletion region [1]. According to [17], the variance of V_{th} mismatch caused by RDF follows a Gaussian distribution, and its standard deviation can be modeled as:

$$\sigma_{\Delta V_{th},RDF} = \frac{t_{ox}}{\epsilon_{ox}} \cdot \frac{\sqrt[4]{2q^3\epsilon_{si}N_a\phi_B}}{\sqrt{3W_{eff}L_{eff}}}, \tag{5}$$

where N_a is the channel doping concentration, ϵ_{si} is the Si permittivity, ϕ_B is the difference between the Fermi Level and the intrinsic level, and $W_{eff}L_{eff}$ denotes the transistor's active area.

The PV-induced V_{th} variations define the statistical reliability profile of the circuit, SRAM cells in our case, at time 0, i.e., when devices are fresh. As known, NBTI induces a temporal V_{th} degradation and, for an individual device, V_{th} evolution in time is governed by Eq. (1). However, due to the RDF effect, the Si–H bonds dissociation and re-passivisation processes experience stochastic fluctuations. Thus, by taking the PV influence into consideration, the long term V_{th} degradation induced by NBTI can be expressed as [18]:

$$\Delta V_{th}(t) = A\left(1 - S_v(\Delta V_{th}^g + \Delta V_{th}^l)\right)t^n, \tag{6}$$

where S_v is a threshold voltage sensitivity coefficient. As a result, the variation of V_{th} temporal shift due to NBTI, given its mean $\mu(\Delta V_{th}(t))$, can be expressed as [13]:

$$\sigma_{\Delta V_{th},NBTI} = \sqrt{\frac{2q}{\epsilon_{si}} \cdot \frac{t_{ox}\mu(\Delta V_{th}(t))}{W_{eff}L_{eff}}} \propto t^{1/12}. \tag{7}$$

Finally, the variation of V_{th} when considering both mismatch and NBTI effects can be calculated as

$$\sigma_{\Delta V_{th}} = \sqrt{\sigma_{\Delta V_{th},RDF}^2 + \sigma_{\Delta V_{th},NBTI}^2}. \tag{8}$$

Fig. 1 represents the calculated mean value and standard deviation of the NBTI-induced ΔV_{th} degradation according to the discussion above. After a short stressing period ($t > 10^2$ s), the power-law dependence can be clearly observed for both PTM 32 nm planar and 20 nm FinFET technologies [12].

Thus we can conclude here, the NBTI failure mechanism not only shifts the V_{th} parameter, but also increases the spread of its value. Hence, the influence of device parameter variation on the circuit performance should be taken care dynamically.

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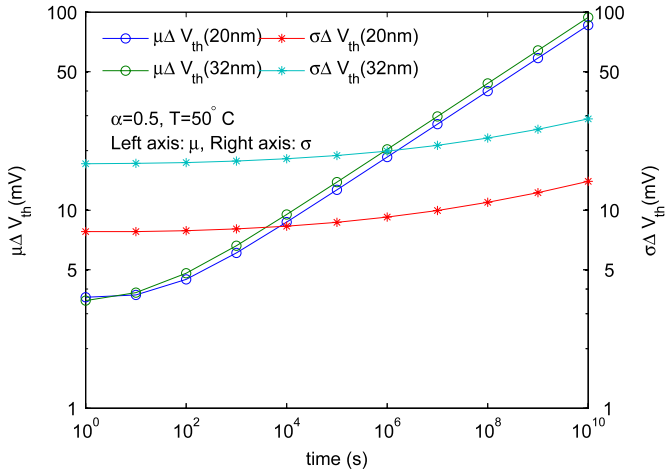

Fig. 1. NBTI induced V_{th} degradation mean value and standard deviation for PTM 32 nm and 20 nm FinFET [12].

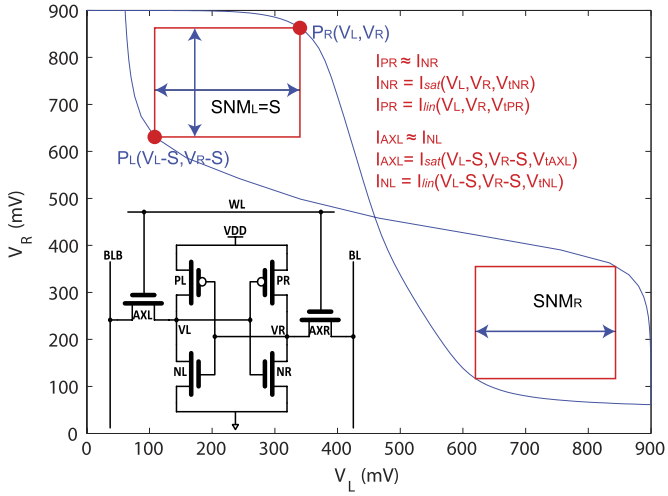

Fig. 2. 6T SRAM cell schematic and butterfly curve (PTM 32 nm technology, V_{DD} = 0.9 V).

3. ΔV_{th} impact on SRAM cell stability

As a major part of modern processors, SRAM drives the technology scaling direction in industry. Hence, ensuring the SRAM cell reliability is critical for technology scaling, as due to its small area and power consumption it is more sensitive to temporal degradation and spatial variations than other components. In view of this in the following we study the influence of threshold voltage value and variation on the SNM, which is a metric reflecting the memory cell stability.

3.1. SNM vs. ΔV_{th}

A conventional 6T SRAM cell and its stability diagram are presented in Fig. 2. The most critical SNM is READ SNM, since READ operation has a more severe condition than HOLD and WRITE operations. The SNM (for READ, hereinafter if without special specification) can be derived by solving the Kirchhoff's Current Law (KCL) at the cell storage nodes *VL* and *VR* for read operation, respectively:

$$I_{NR} = I_{PR} + I_{AXR},$$
$$I_{NL} = I_{PL} + I_{AXL}. \quad (9)$$

For the simplicity of discussion, the drain current can be estimated by an alpha-power law current model [16]. If we assume that $V_L \approx V_{dd}$ and $V_R \gg V_{tPL}$ for the left side SNM, then I_{AXR} and I_{PL} are negligible. As depicted in Fig. 2, in the *PR* and *PL* neighborhood

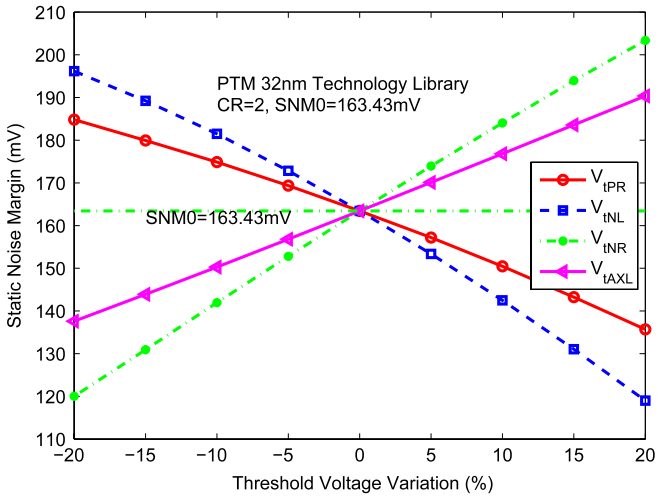

Fig. 3. SNM_L vs. ΔV_{th} variations for the 6T SRAM cell transistors (PTM 32 nm planar devices, CR = β_{NL}/β_{AXL} = 2).

solving the KCL equations for V_R yields:

$$V_{dd} - \frac{\beta_{NR}}{\beta_{PR}} \frac{(V_L - V_{tNR})^{\alpha}}{(V_{dd} - V_L - V_{tPR})} = V_{tNL} + S + \frac{\beta_{AXL}(V_{dd} - V_L + S - V_{tAXL})^{\alpha}}{\beta_{NL}(V_L - S)}, \quad (10)$$

where V_L is the node voltage at left SRAM node when $S = SNM_L$ reaches maximum, α is the constant from alpha-power law current model [16], and $\beta_x = \mu_{eff} C_{ox} W_x/L$ are the coefficients in the current equation and V_{tx} are the threshold voltages, where $x \in \{AXL, NL, PR, NR\}$, as depicted in Fig. 2. A similar relationship can be derived for the SNM of right node.

From Eq. (10) we can deduce that SNM_L is determined by four transistors, namely PR, NR, AXL, and NL. Hence, the SNM_L fluctuation is a function of the V_{th} variations of these four transistors, i.e.,:

$$\Delta SNM_L = \sum_i \frac{\partial SNM_L}{\partial V_{ti}} \cdot \Delta V_{ti}, \quad (11)$$

where $i \in \{PR, NR, AXL, NL\}$.

Applying partial derivative on both sides of Eq. (10), we can solve the dependence of SNM_L on the V_{th} variations of the corresponding transistors, which can be expressed as:

$$\frac{\partial SNM_L}{\partial V_{ti}} = k_i(V_{dd}, \beta, V_{tj})$$

where $j \in \{PR, NR, AXL, NL\} \cap j \neq i$. We can assume that the V_{thj} values are constant for a specific technology, then k_i is constant. Hence, SNM_L has a linear dependence on the V_{th} variations. We verified this relationship by means of SPICE simulation, the results are presented in Fig. 3 for a PTM 32 nm planar-device technology library.

3.2. SNM vs. ΔV_{th} modulation

In order to control the variation-induced stability fluctuations in the 6T-SRAM cell, Adaptive Body Bias (ABB) can be dynamically applied to modulate the V_{th} value of the corresponding transistors, i.e., transistors PR, NR, AXL, and NL for SNM_L. Notice that SNM_L has positive depending-coefficients on ΔV_{th} in transistor AXL and NR, and has negative depending-coefficients on ΔV_{th} in transistor PR and NL. Hence, to compensate the V_{th}-variation induced SNM fluctuations, Forward Body Bias (FBB) is required for AXL and NR; and Reverse Body Bias (RBB) is required for PR and NL.

Furthermore, to increase SNM_L, high V_{tNL} and low V_{tNR} are of interest. Symmetrically, to increase SNM_R, low V_{tNL} and high V_{tNR} should be targeted. As a result, V_{tNL} and V_{tNR} are not suitable to be

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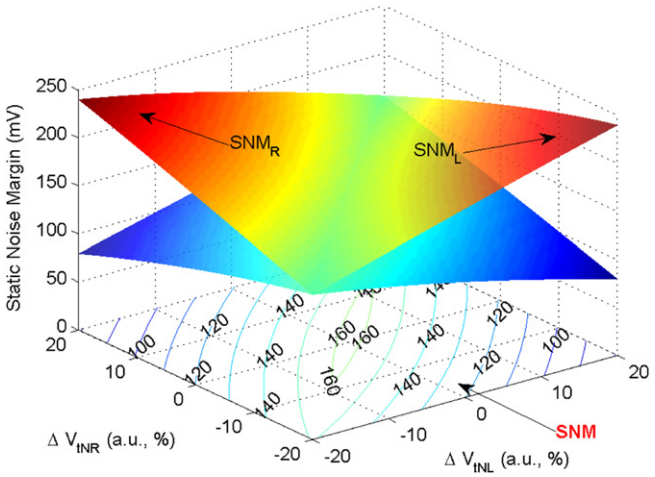

Fig. 4. The SNM vs. ΔV_{th} variations (NL, NR transistors). The contour lines on the bottom plane represent the overall $SNM = min(SNM_L, SNM_R)$ of the cell.

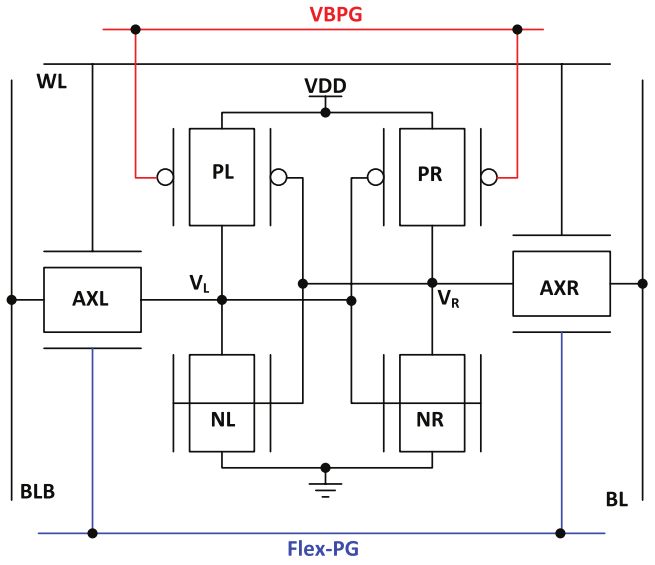

Fig. 5. IG-FinFET 6T SRAM with V_{th} compensation/adjustment for PMOS and pass gates: *VBPG* bias compensates the PMOS NBTI induced V_{th} degradation, and *Flex-PG* bias adjusts the V_{th} of the pass gates to improve the SRAM cell stability.

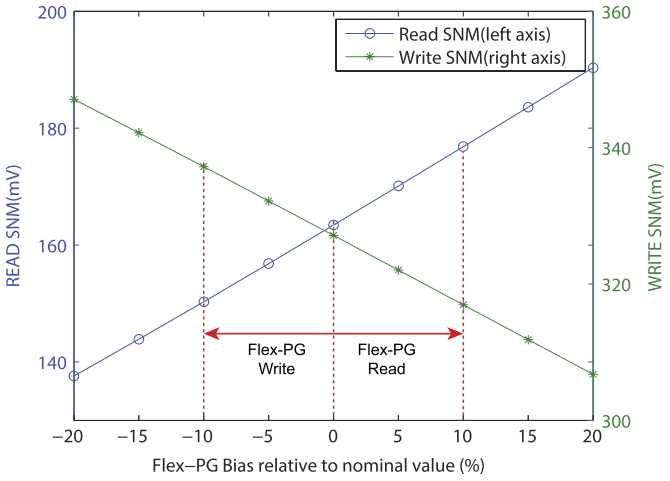

Fig. 6. *Flex-PG* vs. SRAM read/write stability.

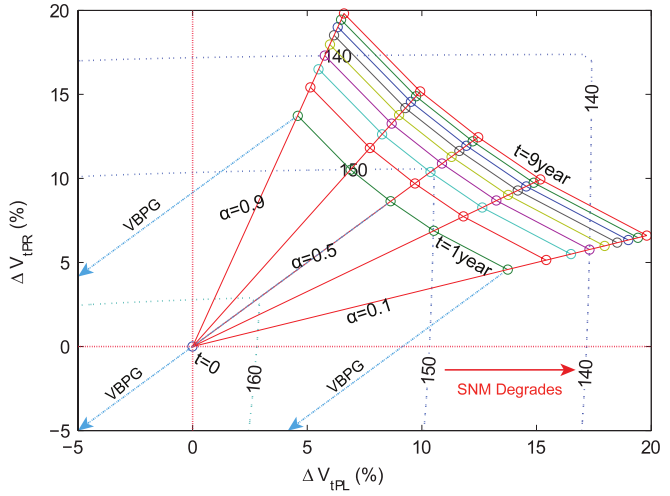

Fig. 7. NBTI-induced cell SNM degradation presented in the $\Delta V_{tPL} \times \Delta V_{tPR}$ plane. The dashed lines with number labels are contour lines for overall SNM of the two nodes. The color lines with cycles are the degraded SNMs after 1–9 year(s), and the solid straight red lines represent the SNM time evolution for a given signal probability α at the left node of the SRAM cell. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

utilized as compensating parameters in a symmetric design. This conclusion is illustrated in Fig. 4. As we can observe in the figure, the optimized overall SNM of a cell ($SNM = min(SNM_L, SNM_R)$) is located at the point where $\Delta V_{tNL} = \Delta V_{tNR} \approx 0$, which means zero bias is always preferred.

With novel device structures specific to emerging technologies, we have opportunities to compensate/suppress the variation-induced stability fluctuations more efficiently. In the next section, we introduce a variation suppression and mitigation technique for SRAM array using double-gate devices.

4. IG-FinFET SRAM stability mitigation

In an independent-gate configuration of FinFET (IG-FinFET) [15], a separated back-gate can be used to control the threshold voltage of the device. The "front-coupling" dependence of the threshold voltage on the back-gate voltage can be expressed as [7]:

$$\gamma_b = \frac{\partial V_{th}}{\partial V_{bg}} = -\frac{C_{si}C_{ox2}}{C_{ox1}(C_{si} + C_{ox2})}, \quad (12)$$

where $C_{ox1/2} = \epsilon_{ox}/t_{ox1/2}$ and $C_{si} = \epsilon_{si}/w_{si}$ are the front- and back-gate oxide capacitance and body capacitance, respectively. The negative sign in Eq. (12) indicates that the direction of threshold voltage change is opposite to that of the back-gate voltage change.

4.1. IG-FinFET based V_{th} compensation scheme

Fig. 5 presents the configuration of an IG-FinFET based 6T SRAM cell with V_{th} compensation for PMOS (through the extra bias *VBPG*) and V_{th} adjustment for the pass gates AXL and AXR (through the extra bias *Flex-PG*) to improve its stability. The *Flex-PG* technique was proposed in [11] to improve the read and write stability by adjusting the V_{th} of the pass gates. A high V_{th} is desirable for the READ stability and a low V_{th} is preferred to improve the WRITE stability. This relationship is illustrated in Fig. 6. During the read operation, the access transistors are forward biased to increase the READ SNM; while during write operation, they are reverse biased to increase the WRITE SNM. The relationship between stability modulation and the value of the applied bias is straight forward, which simplifies the strategy for performance management. In our proposal, the *Flex-PG* range is fixed to compensate the PV-induced SNM fluctuations. The exact *Flex-PG* value is determined by a global PV-sensor, and this value is common to all SRAM arrays in a die.

The time-dependent stability fluctuation induced by NBTI is compensated by the *VBPG* bias. Fig. 7 depicts the NBTI-induced

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SNM degradation versus the ΔV_{th} of the two PMOS devices in the SRAM cell. As one can observe in the figure, the amount of SNM degradation is sensitive to the signal probability α (i.e., the probability that internal left/right node stores 0). The least degradation path (along which the SNM contour line decrease is the slowest) locates at $\alpha = 0.5$, which means the left and right node have an equal probability to store 0. A cell-flip technique was proposed in [8] to balance the signal probabilities between the two SRAM cell nodes. This proposal is efficient to slow down the NBTI induced degradation, however, it introduces a large area overhead and performance penalty for implementation. Instead of node-balancing, we employ a common bias for both nodes to compensate the performance degradation. As illustrated in Fig. 7, with the *VBPG* bias applied, the degradation can be compensated or even eliminated for the extreme unbalanced cases (i.e., $\alpha = 0.1$ or 0.9).

4.2. V_{th} compensation using supply leakage current monitoring

In [6] the authors have analyzed and proposed to use the standby leakage current I_{DDQ} to monitor and characterize the NBTI induced temporal performance degradation. As suggested by their work, a current sensor monitoring the I_{DDQ} for the entire SRAM array is a good indicator of the NBTI degradation. In this section we further extend this idea in order to introduce an NBTI mitigation technique.

The I_{DDQ} of a circuit is defined as the total leakage current in standby mode, which for an SRAM array with N cells can be expressed as follows:

$$I_{DDQ} = \sum_{i=1}^{N} I_{DDQi} = \sum_{i=1}^{N} I_0 \exp\left(-\frac{V_{ti}}{m v_T}\right), \tag{13}$$

where $I_0 = \beta(m-1)(1-\exp(-V_{ds}/v_T))$, m is the body effect coefficient, and v_T is the thermal voltage (kT/q). Under the assumption that the ΔV_{th} due to RDF and NBTI follows a Gaussian distribution, the leakage current value in SRAM cells follows a Log-Normal distribution [10], which gives:

$$\mu(I_{DDQi}) = I_0 \exp\left(\frac{-\mu + \sigma^2/2}{m v_T}\right), \tag{14}$$

$$\sigma^2(I_{DDQi}) = I_0 \left(\exp\left(\frac{\sigma^2}{m v_T}\right) - 1\right) \exp\left(\frac{-2\mu + \sigma^2}{m v_T}\right), \tag{15}$$

where μ and σ are the Mean and Standard Deviation of the V_{th} value, respectively.

According to the Central Limit Theorem, the summation of independent random variables (e.g., I_{DDQi}) can be assumed to follow a Normal Distribution. And given a sufficient large number of N, the total standby leakage current and its standard deviation can be expressed as:

$$\mu(I_{DDQ}) = \sum_{i=1}^{N} \mu(I_{DDQi}),$$

$$\sigma^2(I_{DDQ}) = \sum_{i=1}^{N} \sigma^2(I_{DDQi}). \tag{16}$$

From Eqs. (4), (6)–(8) and (16) we get:

$$\mu(I_{DDQ}) = I_{DDQ0} \cdot \exp\left(-\frac{K_n \Delta V_t(t)}{m v_T}\right), \tag{17}$$

$$\sigma(I_{DDQ}) = \sqrt{N}\sigma(I_{DDQi}) \tag{18}$$

where $K_n = (1 + q t_{ox})/\epsilon_{si} WL$ and

$I_{DDQ0} = N I_0 \cdot \exp(-(V_{th0} + \delta)/m v_T)$,

$\delta = \Delta V_t^g + \sigma \Delta V_{t,RDF}^2/2$,

where V_{t0} is the nominal value of threshold voltage.

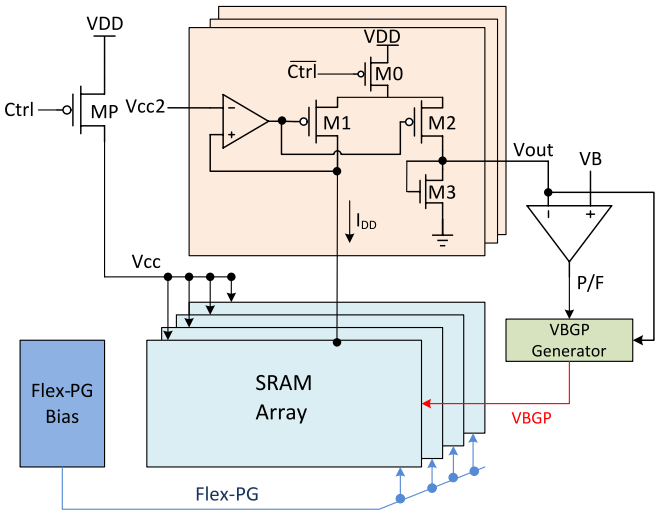

Fig. 8. NBTI mitigation using I_{DDQ} monitor.

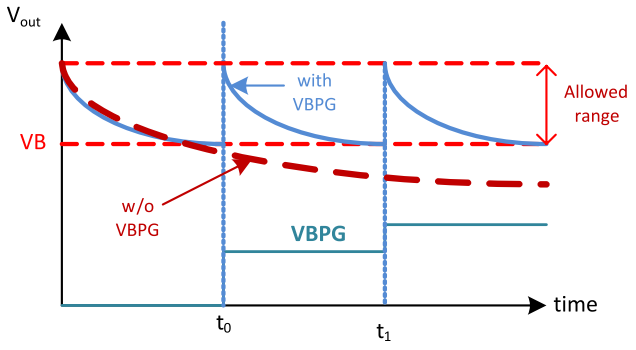

Fig. 9. A practical compensating strategy for NBTI induced degradation.

Eq. (17) suggests that the total standy leakage current I_{DDQ} decreases exponentially with time due to NBTI, hence, it is a good indicator to monitor the NBTI-induced degradation. The specific design of the proposed NBTI mitigation scheme using I_{DDQ} monitoring is depicted in Fig. 8. In the proposed scheme, an I_{DDQ} current sensor formed by the transistors $M1$–$M3$ is attached to each and every SRAM array. A signal called *Ctrl* is used to toggle the working mode of the sensor: during normal operation, the current sensor is bypassed through the transistor MP; while in the measurement mode, MP is cut off and the power supply current of the SRAM array under monitoring is forced to flow through M1. The current is then mirrored into M2 and is converted into a voltage signal by M3, generating an output signal *Vout*. The output signal is subsequently compared with a reference voltage *VB* to evaluate the severity of the NBTI induced degradation. The comparison result is utilized to activate the *VBGP* generator, which produces a proper bias and sends it to the back-gate of the PMOS devices in the SRAM array. The I_{DDQ} current is measured when the SRAM is in standby, i.e., the bit lines BL and BLB of the array are precharged and the word line WL is set to "0". Considering that the NBTI induced degradation is a relatively slow progress, the value of V_{th} compensation for the SRAM array needs to be calibrated only every now and then, thus the SRAM array can be almost all the time in normal operation mode.

The controlling bias *VB* in Fig. 8 determines the actual compensation strategy according to the information provided by the I_{DDQ} sensor. Since the magnitude of the output signal *Vout* is designed to be proportional to the leakage current I_{DDQ}, the compensation strategy is a trade off between performance and leakage power. A simple but efficient compensation strategy is to set a lower limit for

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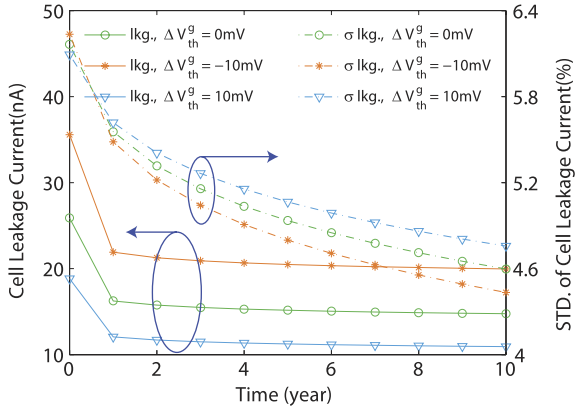
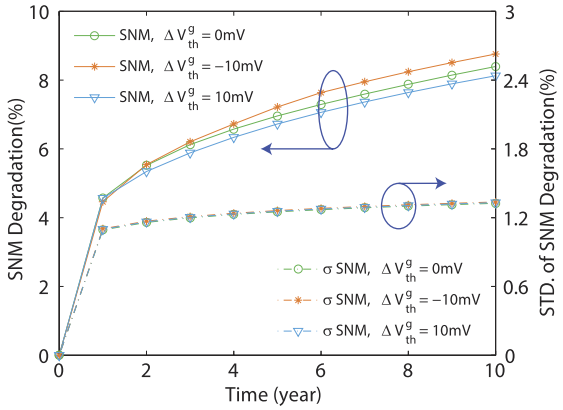
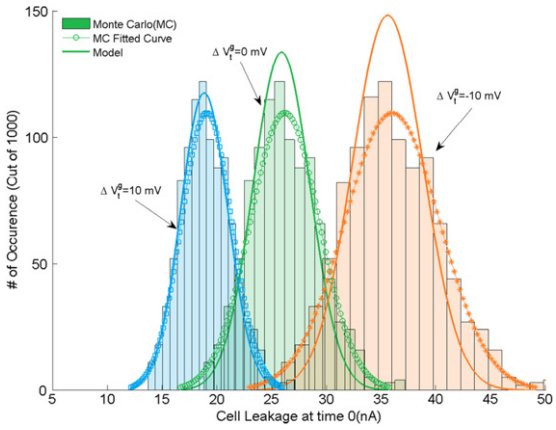


(a) Nominal I_{DDQi} ("lkg." on the left axis) and its relative standard deviation ("σlkg." on the right axis) vs. time.

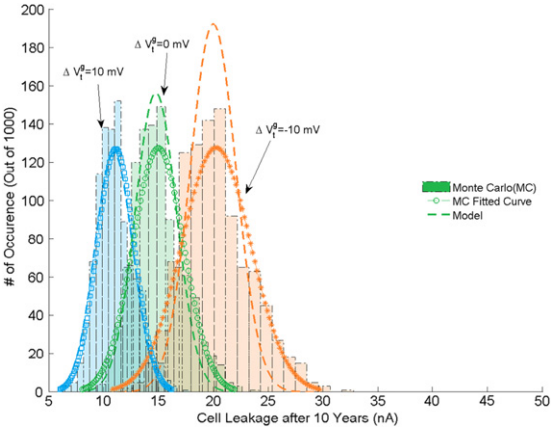


(b) Nominal SNM degradation relative to the fresh device SNM (left axis) and its relative standard deviation (right axis) vs. time.

Fig. 10. 6T-SRAM cell standby leakage and SNM degradation (10-year operation time at 50° C) using 20 nm FinFET technology with −10 mV, 0 mV and 10 mV global variations, respectively.



(a) Fresh device.



(b) After 10-year operation.

Fig. 11. 6T-SRAM cell leakage distribution of fresh device and aged device (10-year operation at 50° C) using 20 nm FinFET technology with −10 mV, 0 mV, and 10 mV global variations, respectively.

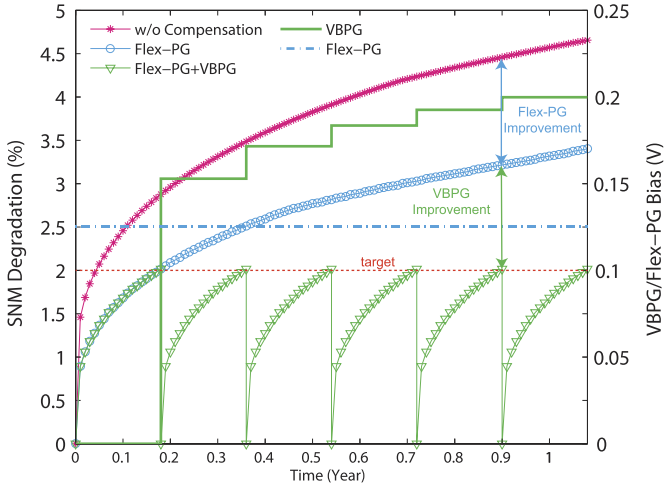


Fig. 12. SNM improvement with the *VBPG* and *Flex-PG* compensating technique with symmetric double-gate 20 nm FinFET technology: $t_{ox1} = t_{ox2} = 1.4$ nm, $w_{si} =$ tfin $= 15$ nm.

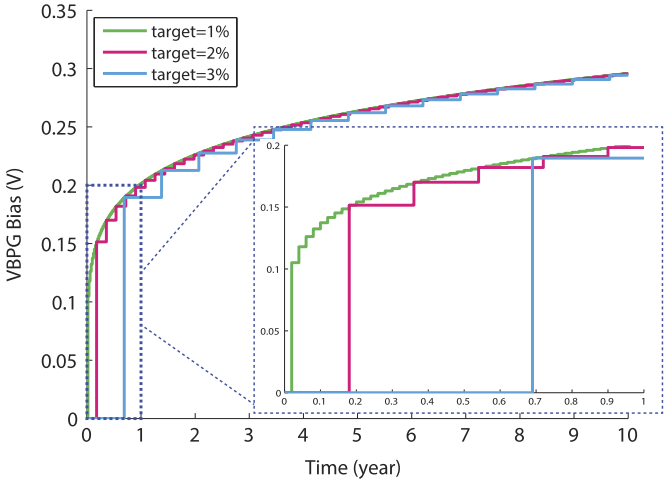


Fig. 13. The applied *VBPG* bias with different targeted SNM degradation margins.

the acceptable I_{DDQ} value. In this way, the performance degradation is set to be in an allowed range, which is determined by the *VB* value, to trade performance for the leakage reduction induced by NBTI. When the performance degradation exceeds the predefined range, the compensation scheme is activated to bring back the performance in the desired range. This strategy is demonstrated in Fig. 9. When the readout of I_{DDQ} *Vout* reaches the pre-defined bottom line *VB*, a corresponding *VBPG* is assigned to compensate the NBTI-induced degradation. This *VBPG* is kept until *Vout* reaches *VB* again.

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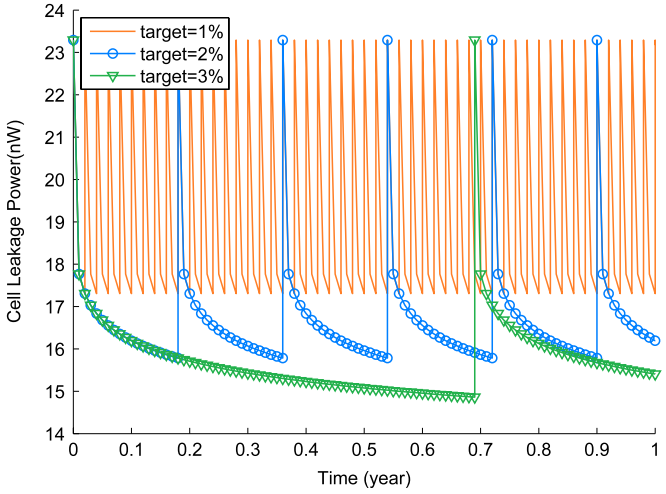

Fig. 14. The cell leakage power consumption versus different SNM degradation targets.

5. Simulations and results

In order to evaluate the efficiency of the proposed compensation technique, we run circuit simulations using the 20 nm PTM library for FinFET [12]. In this library, the BSIM CMG [4] model is utilized for simulation. As up to our best knowledge, no public SPICE model is available for IG-FinFET devices, we use the V_{th} deviation parameter to simulate the V_{th} modulation by back-gate bias. This simplification does not change the effectiveness of the proposed compensation technique, since back-gate modulation for V_{th} in IG-FinFET is verified by both simulations and experiments [9]. The PV variations are generated using a Gaussian distribution for RDF-induced V_{th} variation, as described by Eq. (5). The NBTI stress is set as 10-year operation at 50° C.

We first investigate the time evolution of the cell leakage current under NBTI stress. To demonstrate the influence of the global variation on the degradation, we considered three cases with −10 mV, 0 mV, and 10 mV global V_{th} variation, respectively. Fig. 10(a) represents the NBTI-induced cell leakage current (I_{DDQi}) degradation versus time for the 10-year period. As one can observe in the figure, the I_{DDQi} current decreases very fast at the beginning-of-life, because the NBTI-induced ΔV_{th} follows a power-law of time and I_{DDQi} has an exponential dependence on ΔV_{th}. This I_{DDQi} feature makes it a good indicator to assess the NBTI-induced degradation at the beginning of the operational life, which is crucial to control IC's performance degradation for components like SRAM. Furthermore, the global variation has significant influence on the I_{DDQi} magnitude, but has little effect on the deviation, which means that using I_{DDQi} as degradation indicator is stable in the presence of global variations. Fig. 10(b) presents the SNM degradation relative to the fresh device SNM and the deviation of SNM degradation relative to the SNM at corresponding time for the 10-year operation. The results suggest that ΔSNM follows a power-law rule, as described by Eq. (11). One can observe that the deviation of ΔSNM increases with time, which means that the performance uncertainty becomes larger at the end-of-life. As a result, the V_{th} compensation has to take this uncertainty into consideration for a heavily stressed component.

In order to evaluate the accuracy of the estimation model (i.e., Eqs. (14) and (15)) on the cell leakage distribution, we run Monte-Carlo simulations for RDF and NBTI induced ΔV_{th} variations and the simulation results are presented in Fig. 11. The data in the figure clearly indicate that, the distributions of cell leakage are accurately captured by the proposed I_{DDQi} model for both fresh devices and aged devices after 10-year operation. We recall that the accurate estimation on the I_{DDQi} magnitude and spread range is critical to set the allowed performance degradation range for the ΔV_{th} compensation technique. Its underestimation leads to an increasing soft error rate in the SRAM array while its overestimation leads to a higher leakage power consumption.

Fig. 12 presents the SNM improvement obtained by means of *VBPG* and *Flex-PG* compensation/mitigation techniques. The *VBPG* compensation trigger is set at 2% degradation of the fresh device SNM. A symmetric double-gate FinFET, with thickness of front- and back-gate oxide $t_{ox1} = t_{ox2} = 1.4$ nm, and fin thickness $w_{si} = 15$ nm was utilized in the simulation. One can observe in the figure that, when compared with the degradation without any compensation technique, *Flex-PG* can reduce about 26.67% of the SNM degradation at the end of one year operation (from ∼4.5% to 3.3% degradation versus fresh device SNM). *VBPG* compensation can maintain the SNM degradation after 1 year under 2% of the fresh device, which is about 55.56% improvement when compared with the uncompensated case. The magnitude of the applied forward bias *VBPG*, calculated by Eq. (12), is presented in the figure as well.

Fig. 13 presents the required *VBPG* bias corresponding to different SNM degradation margin targets for a 10-year operation. As one can observe in the figure, different degradation targets set different resolutions for the compensation bias *VBPG*. As degradation increases, the *VBPG* bias for different targets saturate to the same value towards the end-of-life. Hence, a more intelligent compensation strategy is to set a fine-grain *VBPG*-calibration at the beginning-of-life to improve the cell stability, and a coarse-grain *VBPG*-calibration after certain operation time (e.g., 1 year) to increase the availability in normal operation mode.

From the cell stability point of view, high *VBPG* is preferred. However, high *VBPG* increases the standby leakage significantly. Fig. 14 presents the average cell leakage power consumption corresponding to different SNM degradation targets. The average power consumption difference between the worst case (targeting 1% degradation) and the best case (targeting 3% degradation) could be as large as 20% (i.e., 19.45 nW vs. 15.63 nW). Hence, the compensation strategy is a trade-off between cell stability and power consumption, and between bias–calibration frequency and normal operation time as well.

For the simplicity of implementation, Eq. (17) implies a uniform NBTI duty-cycle "α" of the internal nodes (for the left and right node in a cell, $\alpha_L + \alpha_R \cong 1$) for cells in the SRAM array monitored by the same I_{DDQ} sensor. However, the cell duty-cycles are not uniform in practice. The real duty-cycle of a cell is dependent on the "0/1" value ratio (i.e., workload) stored in the cell. Other than previous works like [8] that introduces extra hardware and cycle time to balance the duty-cycles between the two internal nodes of the SRAM cell, we argue that the asymmetric degradation of the two nodes can be compensated by slightly increasing the *VBPG* bias.

To demonstrate our argument, we generated two sets of normally distributed α ratios to simulate the non-uniform NBTI duty-cycles in the SRAM cells. In one set of the ratios, the mean value of α is set to be 0.5, simulating the symmetric (i.e., $\alpha_L = \alpha_R$) case of workload for the two nodes of the SRAM cell; while in the other set of ratios, the mean value of α is set to be 0.3, simulating the asymmetric case of workload for the two nodes. The real distribution of α ratios is out of the scope of this work, but it should be close to the symmetric case. This holds true for example in the case of general purpose processors, when during the application execution, the probabilities of "0"/"1" occurring in a bit cell are very fast becoming equal, and the probability that one cell bit is always "0" or "1" is extremely small.

The SNM degradation results are presented in Fig. 15. As we can observe in the figure, the deviation of the symmetric workload case is indeed smaller than the one corresponding to the asymmetric

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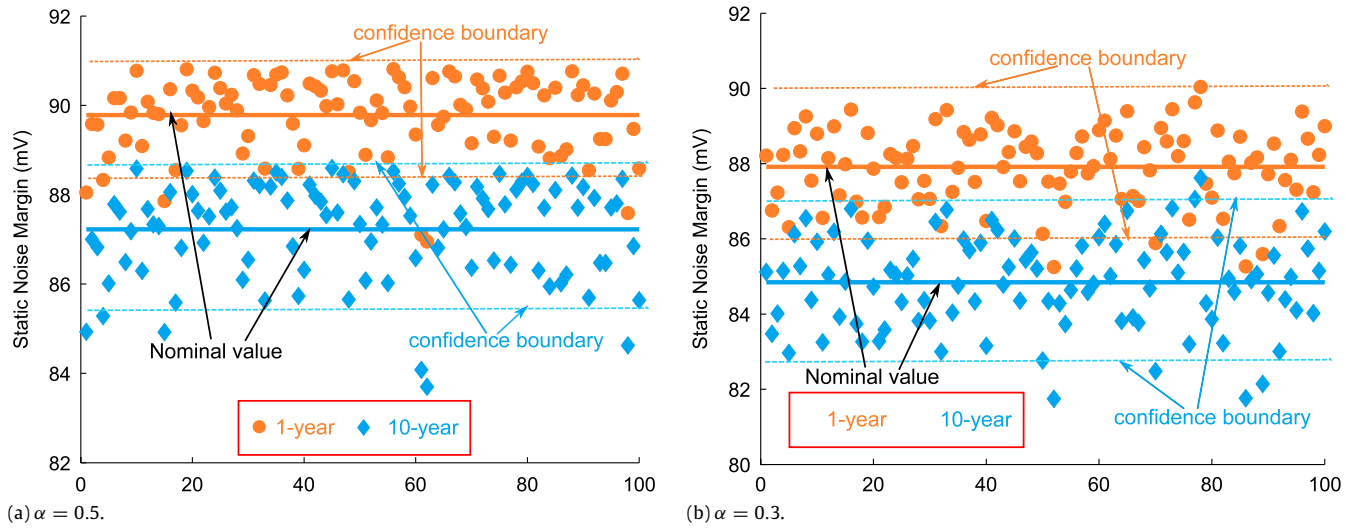
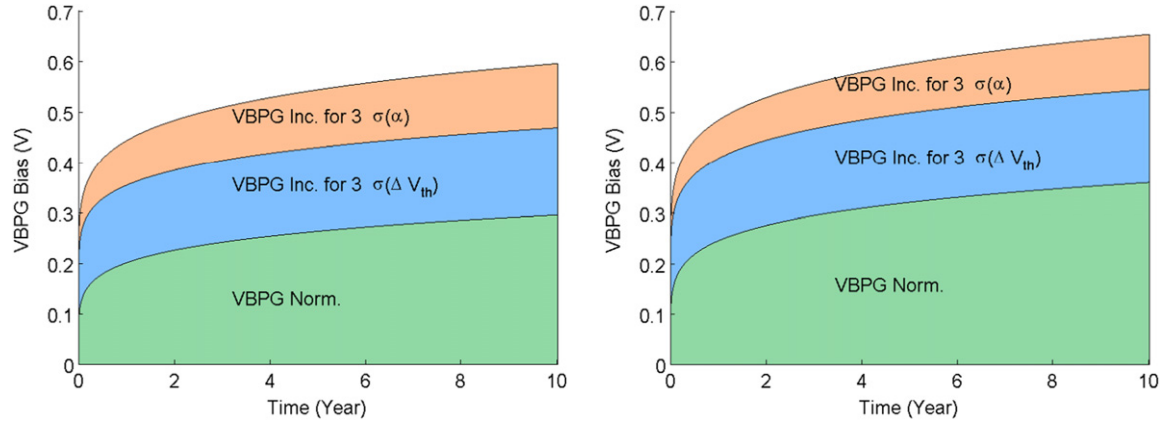


(a) $\alpha = 0.5$. (b) $\alpha = 0.3$.

Fig. 15. SNM fluctuations under normally distributed NBTI duty cycles α cases. For both cases the deviation $\sigma(\alpha)$ is set to be $0.2\mu(\alpha)$.



(a) $\alpha = 0.5$. (b) $\alpha = 0.3$.

Fig. 16. The required *VBPG* bias for non-uniform α ratios in SRAM arrays. For both cases the deviation $\sigma(\alpha)$ is set to be $0.2\mu(\alpha)$.

workload case. However, the spread of cell SNM degradation due to α variations for both cases is relatively small (about 2%). Further, Fig. 16 presents the corresponding required *VBPG* bias for these two non-uniform α-ratio cases. The blue and orange area in Fig. 16 stands for the required *VBPG* increment to cover $3-\sigma$ SNM variation induced by ΔV_{th} and the α-ratio randomness in the SRAM array, respectively. As one can observe in the figure, the *VBPG* increment induced by α-ratio randomness is smaller than the one induced by ΔV_{th} variations for both symmetric and asymmetric workload cases. Comparing the symmetric and asymmetric workload cases, one can find out that the required *VBPG* value in the asymmetric case is just slightly larger than the one in the symmetric case. Even though the stress ratio in all the cells can be perfectly balanced, the SNM deviation induced by ΔV_{th} variations is still large. In other words, without V_{th} compensation technique, the failure rate caused by stability fluctuation will be still very large for perfectly stress-balanced SRAM array using techniques like the cell-flipping proposed in [8]. In contrast, the proposed V_{th} compensation technique in this work is able to maintain the required cell stability in the presence of ΔV_{th} variations and α-ratio randomness.

6. Conclusions

In this paper, we investigated the influence of NBTI degradation induced variation and random process variations on the stability of the 6T-SRAM cell. Based on SPICE simulations, we thoroughly examined the contributions of ΔV_{th} variation in different transistors to the cell stability and the corresponding compensating bias schemes. After that, we proposed a variation mitigation technique able to maintain the SRAM cell stability within a targeted range. Our proposed approach relies on an I_{DDQ} current sensor, and on the FinFET capability to operate in the independent mode to assess the degradation level and to perform threshold voltage compensations, respectively. We evaluated the impact of our proposal on the SRAM stability by means of SPICE simulations for 20 nm FinFET devices. Simulation results indicate that the proposed technique can effectively maintain the stability of an SRAM array within the desired range during its operational life under both spatial and temporal variations, hence substantially improve the performance and reliability of the system. For example, our method allows for maintaining the SNM degradation of SRAM cells to 2% of fresh device after 1 year operation, which is about 55.56% improvement when compared with the 4.5% degradation corresponding to the uncompensated case.

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