Ultra Low Power NEMFET Based Logic

Marius Enachescu[1], Mihai Lefter[1], Antonios Bazigos[2], Adrian M. Ionescu[2] and Sorin Dan Cotofana[1]

[1]Computer Engineering Laboratory, Delft University of Technology
[2]Nanoelectronic Devices Laboratory, École Polytechnique Fédérale de Lausanne (EPFL)
m.enachescu@tudelft.nl, antonios.bazigos@epfl.ch

***Abstract*—In this paper, we introduce a Nano-Electro-Mechanical Field Effect Transistor (NEMFET) based logic family tailored to the implementation of low speed and ultra low energy functional units and processors. Basic Boolean gates implemented with NEMFETs only are analysed and compared against equivalent CMOS realisations. Our simulations suggest that the proposed short-circuit current free NEMFET gates exhibit up to 10x dynamic energy reduction and up to 2 orders of magnitude less leakage, at the expense of 10 to 20x slower operation, when compared with CMOS counterparts. We also analyse the fan-in influence on gate performance and observe that NEMFET the gate energy advantage increases with fan-in. Finally, we consider a 3D-Stacked hybrid NEMFET-CMOS computation platform running a heartbeat rate monitor application and demonstrate that NEMFET based logic is an enabling factor for the implementation of "zero-energy" operated systems.**

I. Introduction

While CMOS scaling substantially diminishes device delay the scalability frontier of the threshold voltage (V_T) limits the reduction of the supply voltage; thus, the energy consumption does not gracefully scale with feature size reduction. Moreover, feature size technology scaling implies high power density and leverages an abrupt leakage increase [1]. While for general purpose and high performance applications the throughput and/or latency is the most important figure of merit for many embedded applications, e.g., wireless sensor networks [2], the capability to operate without a battery change until they become obsolete is of premium importance. Such applications have a high idle rate and relaxed time constraints thus, to meet such a "zero-energy" operation requirement, they should be implemented with low speed and extremely low power technologies. Current CMOS technologies are not the best fit for their implementation as they even have large leakage and/or require high power supply thus tight "zero-energy" budgets cannot be satisfied.

With the advent of Nano-Electro-Mechanical Systems (NEMS) novel devices, e.g., NEM Field Effect Transistor (NEMFET) [3], have been proposed with ultra-low leakage currents, low active energy due to abrupt switching, and hysteresis. Such devices have been initially meant to be utilized in sensing [4]. However, their utilization as sleep transistors in power management schemes has been also investigated [5].

In this paper, we introduce a NEMFET based logic family tailored to the implementation of ultra-low energy functional units and processors. We introduce basic Boolean gates implemented with NEMFETs only, analyse their performance, and compare with CMOS counterparts. In our proposal, we make use of the NEMFET hysteresis and introduce short-circuit current free designs. Thus, the NEMFET gates do not experience short circuit path during switching, and that energy component is eliminated. Our simulations suggest that when compared with CMOS gates implemented in a technology with similar transistor size the NEMFET gates are between 10 to 20x slower but consume up to 10x less energy and have up to 2 orders of magnitude less leakage. We also perform an analysis of the fan-in influence on gate performance, which suggests that NEMFET gates are even more advantageous in terms of energy reduction as the number of inputs increases. We equipped the Trough Silicon Via (TSV) based 3D-Stacked hybrid NEMFET-CMOS computation platform in [5] with NEMFET implemented power management. This results in a further 5% energy reduction for the heart beat monitoring and 21% for application with 10x lower activities rate [6]. Due to this reduction the size of the vibration energy generator needed to power the SoC in a "zero-energy" regime decreases from 2.15cm^2 to 2.03cm^2 and 1.69cm^2, respectively. This clearly indicates that NEMFET-based logic is an enabling factor for the implementation of "zero-energy" operated systems.

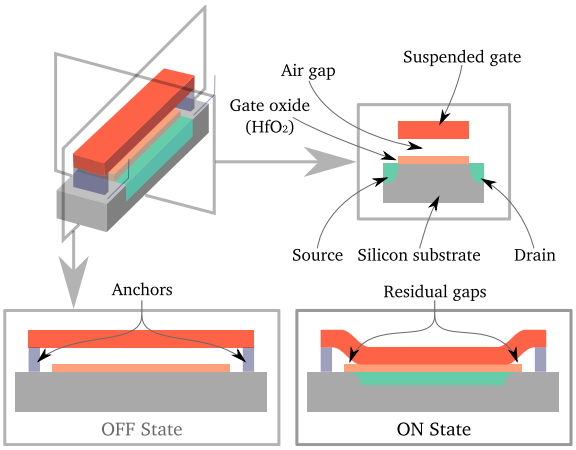

Fig. 1: Illustrative cross-section of NEMFET. The two states, e.g., pull-out (OFF) and pull-in (ON), are depicted.

The rest of the paper is organised as follows. In Section II, we provide a brief NEMFET overview and introduce a novel, compact model that allows us to simulate basic NEMFET based logic gates. Section III introduces the proposed NEMFET based logic family, analyses its performance, and positions it versus CMOS implementations. In Section IV, we make use of the NEMFET logic for the implementation of the power management circuitry and we evaluate this implication by considering a 3D-Stacked hybrid NEMFET-CMOS computation platform running a heartbeat rate monitor application as a case study and evaluate its potential "zero-energy" operation. Finally, Section V presents some conclusions.

II. NEMFET Background and Compact Modeling

The Nano-Electro-Mechanical Field Effect Transistor (NEMFET) has a 3D geometry and cross-section as presented in Fig. 1. It has ultra-low leakage currents, low active energy due to abrupt switching, and hysteresis.

Essentially speaking, the device behaves like an electromechanical switch which responds to gate bias changes as follows. When the gate voltage V_G is low, the gate-oxide capacitance is in series with the air-gap capacitance resulting in low electrostatic coupling of the gate to the channel, thus in a negligible drain current I_D. If V_G increases the situation remains unchanged until it reaches the pull-in voltage V_{PI}

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in which case the electrostatic force cannot be compensated anymore by the mechanical restoring force and the suspended gate (beam) snaps onto the gate oxide, thus turning on the device. After the pull-in, the I_D increase with V_G is comparable with the one of a standard MOSFET. On the other way around when V_G is decreased from some high value I_D starts decreasing until at a certain V_G value when the system becomes unstable due to combined electro-mechanical force and the beam is pulled-out. This causes an abrupt I_D decrease due to a large decrease in capacitance, i.e., the pull-out effect.

In our implementations, we make use of Fully Depleted Silicon on Insulator (FD SOI) NEMFETs and in order to analyse the performance and potential of our proposal we rely in circuit simulations. Thus, compact models are required to accurately capture the complex NEMFET behavior.

The model developed for the NEMFET consists of two main elements: (i) The BSIM-IMG FD SOI model [7], [8] is utilized for predicting the electrical behavior of the transistor; (ii) A Verilog-A-based compact model was developed to estimate the position of the suspended gate. Moreover, the variation of the capacitor in series with the gate was taken into consideration. As the nature of the device extends both in electrical and mechanical regimes, both such types of Verilog-A natures were addressed in the model. An in-depth description of the model can be found in [9].

The parameters of the model have been extracted after hybrid numerical simulations that combined multi-physics and semiconductor analyses [10], [11]. At the first step, the parameters of the BSIM-IMG FD SOI model were extracted, considering the NEMFET with a constantly pulled-in gate-beam. Subsequently, the parameters for the electromechanical addition of the suspended-gate model were as well extracted. In order to adapt the model to the TCAD results, further optimizations were required, i.e., adapting the initial nominal values for our parameters of interest. Since the model is written in Verilog-A it is portable in a wide variety of simulators. Therefore, two design-kits have been implemented that easily introduce the NEMFET model to the Agilent ADS and the Cadence Virtuoso software platforms.

III. Short Circuit Free NEMFET-based Logic

This section provides an answer to the following question: *"To which extent can CMOS alike NEMFET based logic supersede traditional logic?"* Hence, we introduce NEMFET based Boolean gates tailored to the implementation of ultra low energy functional units and processors, analyze and compare their performance with CMOS counterparts. Finally, we address the following issues related to NEMFET-based logic: (i) energy efficiency against the "classic" CMOS logic, and (ii) scaling for improved performance.

By wiring two NEMFETs together in a traditional manner, we form an inverter circuit. The dynamic inverter operation at a clock frequency of 125 MHz is depicted in Fig. 2, for a square-wave input signal supplied by a waveform generator. The NEMFET hysteresis allows for n/p NEMFET channel sizing that precludes the situation when the two NEMFETs are simultaneously open during the switching. In this way the most important power component, i.e., the power consumption given by the Short Circuit (SC) current, is diminished.

Fig. 3 depicts the SC current analysis of an NEMFET inverter without and with hysteresis. First, if no proper attention is given to NEMFET sizing, the inverter behaves like a normal CMOS gate (left side of Fig. 3). However, by proper dimensioning of the n/p-NEMFETs (Fig. 3 right side) we can adjust the occurrence of the Pull-In (PI) and Pull-Out (PO) events as follows: (i) the nNEMFET PI takes place after the pNEMFET PO; (ii) the pNEMFET PI takes place before the nNEMFET PO. In this way, we arrange the switching

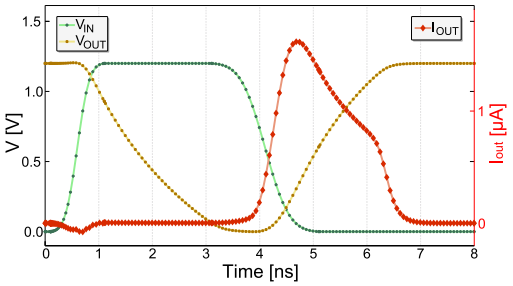


Fig. 2: NEMFET inverter transfer characteristics.

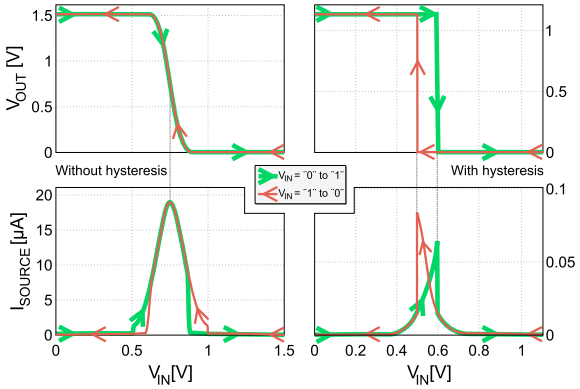


Fig. 3: NEMFET inverter SC current analysis.

moments such that the two transistors are never conducting at the same time, which is practically cancelling the short circuit current and results in 2 order of magnitude reduction of the energy consumption per switching event.

We can build upon the Inverter and construct basic Boolean gates operating according the same SC free paradigm. The voltage transfer functions for two-input (NAND, NOR) gates are depicted in Fig. 4, for a 100 MHz clock period. Thus, the NEMFET gates do not experience the creation of a short circuit path during switching, and that energy component is eliminated.

Table I presents the delay and the static and dynamic energy parameters for various (INV, NAND, NOR) gates implemented with NEMFETs and in a commercial CMOS 65nm Low Power (LP) technology. The figures of merit of the CMOS High-V_T logic gates were obtained using Cadence Spectre while Agilent ADS was utilised for the NEMFET-based logic.

TABLE I: CMOS vs. NEMFET gates.

	NAND		NOR		INV	
	C	**N**	**C**	**N**	**C**	**N**
E dynamic [fJ]	3.27	0.65	2.72	0.57	1.33	0.41
P leakage [pW]	11.72	0.16	13.44	0.16	8.21	0.08
Delay [ns]	0.04	0.80	0.05	0.78	0.03	0.31

C, N stands for CMOS and NEMFET, respectively.

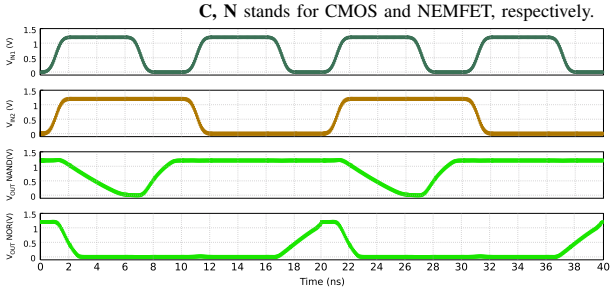


Fig. 4: Transfer characteristics for NEMFET NOR/NAND.

One can observe in the table that NEMFET gates are between 10x to 20x slower but consume up to 10x less energy and have up to 2 orders of magnitude less leakage. Having these results in mind, we can conclude that the NEMFET logic application field is rather limited for the time being to ultra low energy, low frequency, low activity designs, e.g., wireless sensor node running a heart beat rate application [5]. However, since it has been already proven that the NEMFET beam could scale at least up $260nm$ x $65nm$ [12] and the scaling is predicted to continue in the following years [13], we expect the NEMFET delay to decrease thus to make NEMFET logic more competitive.

We also perform an analysis of the fan-in influence on gate performance which results are presented in Table II. The Table suggests that NEMFET gates are even more advantageous in terms of energy reduction as the number of inputs increases. For example while a NAND2 CMOS consumes 5x more dynamic energy than a NAND2 NEMFET this factor becomes 10x for the NAND4 case.

TABLE II: CMOS vs. NEMFET - variable fan-in NAND.

	NAND2		NAND3		NAND4	
	C	**N**	**C**	**N**	**C**	**N**
E dynamic [fJ]	3.27	0.65	6.90	0.96	11.20	1.24
P leakage [pW]	11.72	0.16	13.28	0.22	14.42	0.28
Delay [ns]	0.04	0.80	0.06	1.20	0.09	1.55

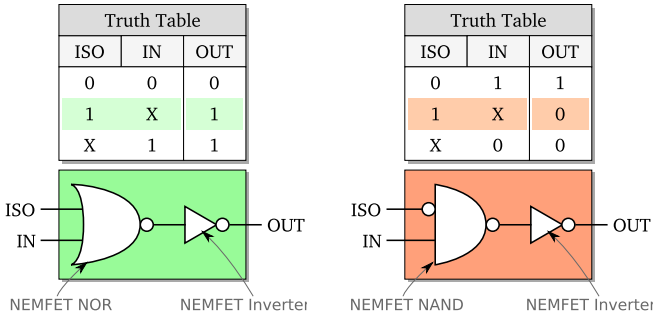
C, N stands for CMOS and NEMFET, respectively.

IV. NEMFET-based Power Management Logic

State of the art ultra low power designs employ specific Power Management (PM) circuitry to turn off inactive units in order to achieve energy savings [14]. While PM is substantially reducing the idle parts leakage by separating them from the supply voltage by means of High-V_T MOSFET or NEMFET [15] based Sleep Transistors (STs), it has been noticed in [15] that the always-active PM circuitry significantly contributes to the total energy consumption of low activity rate applications. Thus, in this section, we make use of the proposed SC-free NEMFET logic for the implementation of the PM circuitry, i.e., Isolation Cells (ISO), State Retention (SR) cells, and PM Controller (PMC). Additionally, to evaluate the impact of utilising SC-free NEMFET based logic for the PM circuitry implementation, we consider, as a case study, a 3D Through-Silicon Via (TSV) based hybrid NEMFET-CMOS computation platform running a heartbeat rate monitor application.

Next, we describe how the basic NEMFET logic gates can be utilised to implement the PM circuitry in a heterogeneous 3D stacked power management architecture composed out of a NEMFET and a CMOS tier.

1) Isolation Cells: Isolation cells (ISO) control the floating output of powered down blocks and clamp the outputs to a specific, legal value. Thus, they prevent short circuit current generation from the power gated block floating connections. NEMFET-based logic gates are employed for Retain 1/Retain 0 isolation cells as depicted in Fig. 5a, and Fig. 5b, respectively. An ISO group part of the same power domain can share the isolation control signal. Every isolation cell requires 2 TSVs, one for the input signal coming from the powered-down block, and the other for the output to be clamped. The isolation control signals are generated by the PMC and since it is implemented on the same NEMS die as the isolation cells, no TSVs are needed for the control signals. Hence, the total cost in terms of number of TSVs is given by $N_{TSVsISO} = 2N_{ISOCELLS}$, where $N_{ISOCELLS}$ is the total number of isolation cells.



(a) Retain "1" isolation cell. (b) Retain "0" isolation cell.

Fig. 5: NEMFET-based isolation cells in commercial designs and associated truth table.

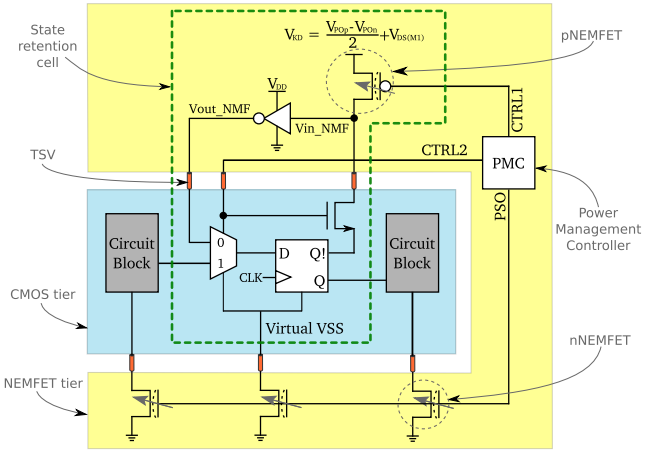


Fig. 6: Heterogeneous state retention cell.

2) State Retention: The storage capacity of the NEMFET inverter makes it suitable also for state retention schemes [16]. Thus, we propose a NEMFET-based state retention cell which preserves the state of a register before a module shuts down, with the hybrid NEMFET-CMOS structure depicted in Fig. 6 and operating according with the signal waveforms from Fig. 7. A specialised dual-function NEMFET inverter with the input connected to the to-be-saved register acts as a classic inverter while the gated block is powered on, and as a memory cell when the power is switched off. A multiplexer selects the value (normal operation or saved) to be written in the flip-flop register. The multiplexer and the flip-flop register, active during normal operation of the power gated block, are implemented on the CMOS tier. In contrast with the ISO case, the NEMFET part of the SR circuit together with the inter-die TSV links are inactive during normal powered operation. Hence, the scheme does not incur any delay penalty that might have detrimental influence on the clock period. Every state retention cell needs 2 TSVs, one for the saved signal value, and the other one for the restored value. The TSV required for the control of the specialised inverter can be shared across all the state retention cells that commute in the same time. The total number of TSVs needed for the SR cells is given by N_{TSVsSR} = $2N_{SRCELLS} + N_{PD}$, where $N_{SRCELLS}$ is the total number of retention bits, and N_{PD} is the number of power domains.

3) Power Management Controler: The PMC is typically a finite state machine that controls the sequence of power-down and power-up events. Its functionality is highly dependent on the actual design implementation and the power modes specifications. The amount of communication between PMC and the design depends on the

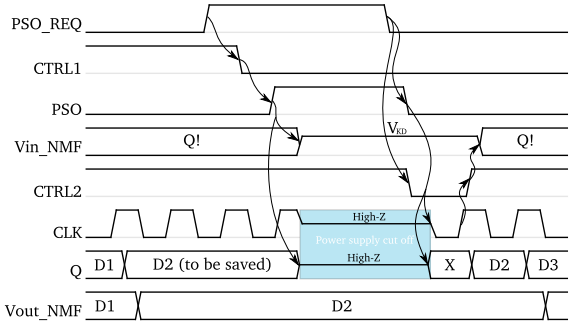


Fig. 7: State retention signal wave forms.

transition rules between power modes. At least a TSV is required to indicate the power state of each power domain. The delay penalty of the NEMFET logic is usually tolerable if the switching between different power modes is done not very frequently. Thus, the controller can run at a reduced clock rate without impeding the overall application performance. This is the case for the considered application presented in our example below.

A. Case Study

To get a more accurate insight on the "zero-energy" potential of the NEMFET-based power management circuitry, we consider a heart beat rate monitoring application running on a typical SoC for low power embedded devices [5]. The SoC consists of a 16-bit processor core, with program and data memory, peripherals, and PM circuitry implemented with either CMOS or NEMFET-based logic.

For this platform, the PM circuitry is composed of isolation cells and PMC only as no SR cells are being present due to the fact that the system state is software-saved in the always-on data memory before the processor core is powered down. The PM circuitry consists of 74 isolation cells and 22 gates for the PMC.

The power consumption values obtained after simulation in best-case technology corner for CMOS, with respect to power consumption, and after simulation with the NEMFET model in Section II, for both the ISO cells and PMC, are presented in Table III. We can observe from Table III that while the active power consumption during operation and during idle is halved when we switch from CMOS to NEMFETs technology, for both ISO cells and PMC, the leakage power is diminished by about 2 orders of magnitude.

We note that for ISO cell implementation we relied on complex gates (see Fig. 5a) for the CMOS case, while for the NEMFET case we cascaded simple gates, which resulted in a larger number of NEMFET gates even though the number of transistors is the same in both implementations. Although a proper area comparison between NEMFET and CMOS-based gates is difficult because of the differences in gate geometries, preliminary results indicate that a NEMFET transistor is typically four times larger than its CMOS counterpart for the same maximum I_{ON} current value. Thus our approach results in an area overhead on the NEMFET tier and an CMOS tier are reduction. Given that in 3D-Stacked technology the design footprint is the relevant area metric, our approach may even result in a footprint reduction. For the time being, NEMFET circuits operating frequency is limited to about 125MHz, which may be high enough given that for most application the PM circuitry operates at low frequency (the entire power management philosophy relies on the assumption that parts of the system stay idle for long periods of time). In case this is not the case, the utilisation of NEMFET based PM circuitry may result in some extra cycles, but with no fundamental implications on the application performance.

TABLE III: PM Circuitry Power Consumption.

	No. Gates	SoC ON	SoC OFF	
		$P_{dynamic}$ [uW]	$Leakage$ [nW]	$P_{dynamic}$ [nW]
ISO CMOS	74	15.63	195	136
ISO NEMFET	158	7.69	2.11	66
PMC CMOS	22	217.73	49.81	1.79
PMC NEMFET	22	107.12	0.58	0.88

Our simulations indicate that if we replace the CMOS PM circuitry of the System-on-Chip presented in [15] with NEMFET one, we can further reduce the energy budget by 5%. We note, however that for an application that has an activity factor 10x lower [6] than the proposed heart rate monitor the energy savings increases to 21%. Due to this reduction, the size of the vibration energy generator needed to power the SoC in a zero-energy regime decreases from 2.15cm^2 to 2.03cm^2 and 1.69cm^2, respectively.

V. Conclusions

In this paper, we introduced a NEMFET based logic family tailored to the implementation of ultra low energy functional units and processors. Basic Boolean gates implemented with NEMFETs only were analyzed and compared with CMOS counterparts implemented in a technology with similar transistor size. Our simulations indicate that the proposed NEMFET based gates consume up to 10x less energy and up to 2 orders of magnitude less leakage, at the expense of up to 20x delay increase. Moreover, for larger fan-in gates, the energy consumption benefit is increasing. Finally, we considered a 3D-Stacked hybrid NEMFET-CMOS architecture running a heartbeat rate monitor application and demonstrated that NEMFET based logic is an enabling factor for the implementation of "zero-energy" operated systems.

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