Lifetime Reliability Assessment with Aging Information from Low-Level Sensors

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ABSTRACT

Aggressive technology scaling has led Integrated Circuits (ICs) suffer from ever-increasing wearout effects. As a consequence, Dynamic Reliability Management (DRM) becomes an essential approach to assure IC's lifetime reliability. Accurate and efficient reliability modeling from low-level aging sensor measurements is critical to DRM systems. This work presents a Time-Sharing Sensing (TSS) method for V_{th}-sensor based DRM to assess the dynamic NBTI-induced degradation experienced by the circuit under monitoring. SPICE simulation results suggest that the proposed TSS method can accurately capture the circuit reliability status under random stress conditions.

Categories and Subject Descriptors

B.8 [**Performance and Reliability**]: Reliability, Testing, and Fault-Tolerance.

Keywords

Dynamic Reliability Management, NBTI, Reliability.

1. INTRODUCTION

Due to the aggressive MOSFET technology scaling that took place in the past decades, reliability has been becoming a rising concern for processor designers. The increasing power densities and operating temperatures made integrated circuits (ICs) suffer from multiple intrinsic failure mechanisms during their servicing time. As a result, device performance degrades gradually and consequently might lead to fails during IC's expected lifetime [3]. To combat the gloomy outlook of reliability situation, a variety of techniques have been proposed to ensure ICs' lifetime reliability. Dynamic Reliability Management (DRM) techniques [5, 6] attempt to hide the inherent pessimistic reliability landscape while maintaining the system performance and lifetime expectation within the desired range. This work presents a Time-Sharing Sensing (TSS) method, for threshold voltage (V_{th}) sensor based DRM systems to assess NBTI-induced degradation in ICs. Our simulations demonstrate that it can accurately capture the dynamic reliability status from the circuits under monitoring with a limited number of aging sensors, which is crucial for DRM practical implementations.

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2. DELAY SHIFT DUE TO AGING

NBTI has been considered as the most dominant failure mechanism in current and future CMOS technology nodes [3], and it is well understood that $|V_{th}|$ increases due to NBTI stress. A long-term V_{th} shift under dynamic NBTI stress is given by [2]:

$$\Delta V_{th} = \left(\frac{\sqrt{K_v^2 \alpha t_{clk}}}{1-\beta_t^{1/2n}} \right)^{2n} = A \cdot (\alpha t)^n, \quad (1)$$

where $n = 1/6$ is the power-law time constant, K_v is the accelerating coefficient (including temperature and electrical field), T_{clk} is clock period, α ($0.1 \leq \alpha \leq 0.9$) is the stress probability of NBTI, i.e. NBTI duty-cycle, β_t is a coefficient reflecting the recovery effect of NBTI, and A is the NBTI time-evolution dependence.

According to the alpha-law model [4], the first order of delay shift due to V_{th} degradation can be expressed as:

$$\Delta\tau_{pd} = \frac{\alpha\tau_0}{V_{dd}-V_{th0}} \cdot \Delta V_{th} = k_\tau \Delta V_{th} \cdot \tau_0, \quad (2)$$

where k_τ is the ΔV_{th} correlation efficient. In a V_{th}-sensor based DRM system, aging sensors are designed to replicate the NBTI stress of a device in the critical paths (CPs) or potential critical paths (PCPs), such that the aging status (i.e., delay shift) of CPs and PCPs can be estimated from the aging sensors output by Eq. (2).

According to Eq. (2), the gate-level delay shift for the NAND and NOR gate can be expressed as:

$$\Delta\tau = \begin{cases} \Delta\tau_{pd,i}, & \text{for NAND,} \\ \sum_{i=1}^{n} \Delta\tau_{pd,i}, & \text{for NOR,} \end{cases} \quad (3)$$

where $\tau_{pd,i}$ is the delay shift of the i^{th} PMOS device in the gate. In other words, the delay shift of the NAND gate is determined by the delay shift of the PMOS device in the CP or PCP, while the delay shift of the NOR gate is the sum of delay shifts of all the PMOS devices in the gate.

Assuming that the NBTI effect on NMOS is negligible, the delay shift of a CP (or PCP) $\Delta\tau_{cp}$ is then the sum of delay shifts of the Pull-Up Gates (PUGs). From Eq. (2), $\Delta\tau_{cp}$ can be derived as:

$$\Delta\tau_{cp} = \sum_{i \in PUGs}^{l} \Delta\tau_i = k_\tau \sum_{i=1}^{h} \Delta V_{th,i}, \quad (4)$$

where l is the CP depth, $\Delta\tau_i$ is the delay shift of a single logic gate, and h equals the number of PMOS devices in

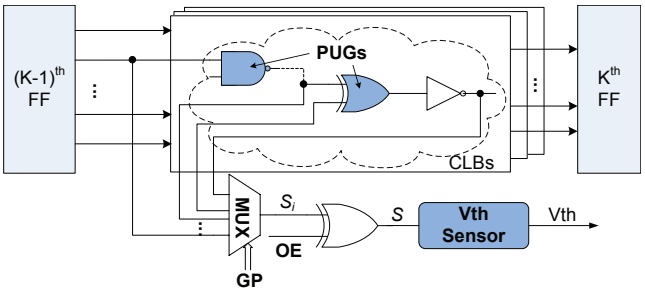

Figure 1: Schematic of Time-Sharing Sensing.

the PUGs. Notice that only half of the logic gates (i.e., odd-/even-stage gates) in the CP is in the PUGs during an input signal transition.

3. TIME-SHARING SENSING SCHEME FOR AGING ASSESSMENT

In order to obtain an accurate $\Delta\tau_{cp}$ estimation, we propose a TSS scheme for V_{th} aging sensors, as illustrated in Figure 1. TSS scheme allows the V_{th} sensor to probe the stress on different nodes at different time moments. This is achieved by routing all the necessary signals (including all inputs of NORs in the PUGs) from the CP to a MUX, and the MUX selects one signal from the inputs and sends it to the V_{th} sensor. The the input signal selection is controlled by the *GP* signal based on a round-robin algorithm, and the selection bit shifts at every time interval Δt.

Based on the proposed scheme, the ΔV_{th} of aging sensor after N intervals can be expressed by:

$$\Delta V_{th} = \sum_{i=1}^{N} \Delta V_{th,i} = \sum_{i=1}^{N} A_i(\alpha_i \Delta t_i)^n, \quad (5)$$

where $\Delta V_{th,i}$ is the parameter degradation during the i^{th} time interval. Further assume $N = k \cdot h$, then the time intervals can be divided into k sub-sequences $\Delta T_j = h \cdot \Delta t$, where $j = 1, 2, ...k$. For the j^{th} sub-sequence, assume the sampled activity ratio of the m^{th} logic gate is the activity ratio for the entire time span, i.e, $\bar{\alpha}_{t\in T_j} \approx \alpha_{t\in(T_{j-1}+m\Delta t)}$, then according to Eq. (1), the total ΔV_{th} of the m^{th} logic gate at the end of sub-sequence ΔT_j can be written as:

$$\Delta V_{th,t\in\Delta T_j} = \left(\frac{\Delta T_j}{\Delta t}\right) \cdot \Delta V_{th,t\in\Delta t_m} = h\Delta V_{th,t\in\Delta t_m}, \quad (6)$$

where t_m is the m^{th} interval Δt in ΔT_j. Insert Eq. (6) into Eq. (4), the delay shift of the entire CP during a large time interval ΔT_j can estimated as:

$$\Delta\tau_{cp,t\in\Delta T_j} = hk_\tau V_{th,t\in\Delta T_j}. \quad (7)$$

Then, the accumulated delay shift can be estimated as:

$$\Delta\tau_{cp} = \sum_{j=1}^{k} \Delta\tau_{cp,t\in\Delta T_j} = hk_\tau V_{th}. \quad (8)$$

Eq. (8) suggests that by introducing the TSS scheme into a DRM system, the long-term delay shift of a critical path is proportional to the V_{th} degradation measured from the associated aging sensor. In other words, the V_{th} sensor measurement indicates the NBTI-induced degradation of the entire CP in TSS scheme, instead of the degradation of one single device in the conventional configuration, which is a significant improvement in terms of area and power efficiency.

Table 1: TSS Based Delay Shift Estimation for ISCAS85&89 Circuits

Name	Estimation Error by TSS Scheme relative to time 0 delay (%)							
	Δt = 1000 clk		Δt = 2500 clk		Δt = 5000 clk		Δt = 10000 clk	
	Cst.	Dvt.	Cst.	Dvt.	Cst.	Dvt.	Cst.	Dvt.
C432	2.34	3.28	2.31	2.73	2.26	2.77	2.19	2.32
C499	4.73	6.17	4.45	5.09	4.27	3.46	4.11	3.89
C880	2.89	2.21	2.64	3.17	2.37	2.55	2.17	2.25
C1908	4.18	3.96	4.73	8.07	4.65	4.12	4.53	4.79
C3540	4.46	2.95	4.37	3.51	4.28	3.29	4.25	5.03

4. EXPERIMENTAL RESULTS

In order to validate the proposed reliability modeling framework, simulations are conducted for a set of ISCAS85 and ISCAS89 benchmark circuits. A PTM [1] 32nm technology library is used for SPICE simulation. The technology library consists of 5 different cells: INVERTER, 2-input NAND, 3-input NAND, 2-input NOR and 3-input NOR. The simulations for SPICE are performed in HSPICE at an accelerated condition, i.e., $T = 120°C$, with an equivalent lifetime of 10-year operation at normal condition.

Table 1 presents the absolute errors of the proposed TSS scheme for delay shift estimation. Four different sampling intervals are investigated, i.e., Δt = 1000, 2500, 5000, and 10000 cycles, respectively. Two kinds of input signal are evaluated: *Cst.* corresponds to a constant activity ratio ($\alpha = 50\%$) signal, and *Dvt.* corresponds to variable activity ratio signals ($\alpha = 50\% \pm 10\%$). The results indicate TSS scheme can accurately capture the delay shift due to NBTI at circuit level.

5. CONCLUSIONS

In this work we presented a time-sharing sensing method for existing V_{th}-sensor based DRM systems to assess NBTI-induced degradation in ICs. SPICE simulation results indicate that the proposed TSS method can achieve accurate reliability assessment under random stress conditions.

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