Temperature Dependence of NBTI Induced Delay

Seyab Khan Said Hamdioui
Delft University of Technology Computer Engineering Laboratory
Mekelweg 4, 2628 CD Delft,The Netherlands
E-mail: {M.S.K.seyab, S.Hamdioui}@tudelft.nl

***Abstract*—Negative Bias Temperature Instability (NBTI) has become a major reliability concern for nanoscaled PMOS transistors. NBTI is a thermally activated process and its aftereffects (e.g. threshold voltage shift, current degradation and delay increment) increase exponentially with the rise in temperature. This paper presents a model of temperature impact on NBTI induced delay for PMOS transistor. It demonstrates the model on 90nm, 65nm and 45nm Predictive Technology Model (PTM) designs operating at temperature range 25-125°C. The results show a strong correlation of NBTI induced delay with threshold voltage shift and holes mobility degradation. The key insights observed are: (a) NBTI induced threshold voltage shift is temperature sensitive and increases up to 42% at high temperatures, (b) NBTI degrades holes mobility in PMOS inversion layer and the degradation reaches 8% in 45nm technology and (c) The impact of NBTI on PMOS transistor delay becomes significant at high temperature and increases by approximately 2.5% in each successive technology reaching 11.5% in 45nm technology.**

I. Introduction

Aggressive scaling of transistor dimensions has fronted reliability concerns [1]. Industrial data reveal that as the gate oxide thickness reaches 4nm, NBTI becomes a dominant concern for PMOS transistors [2], [3], [4]. NBTI results in threshold voltage increment, saturation current degradation and delay degradation. Analysis shows that these effects increase exponentially with technology scaling and rise in operating temperature [4].

NBTI degrades performance of PMOS transistor under a negative gate stress at elevated temperature 100-200°C. The degradation results from several electro-chemical sub-processes inside the oxide layer. Modeling the kinetics of NBTI is a challenging task because the sub-processes have temperature and/or field dependencies. To date, the focus of NBTI literature is to model NBTI degradation at *constant* transistor temperature [3], [5], [6], [7]. However, transistors on-chip dies experience significant temperature variations depending on their locations and the operation conditions. The variations become more significant as technology scales down [1]. It has been shown in [8] that the variations reach up to 20°C in the high end modern microprocessor chips. Since, NBTI depends on thermally activated sub-processes, it is necessary to include the temperature impact on all sub-processes to accurately model NBTI. Several authors [9], [10] have made attempts to include such an impact, but their analysis are limited to few sub-processes. Hence, an NBTI model that considers temperature impacts on all known sub-processes is needed.

NBTI degrades PMOS transistor physical parameters like threshold voltage and channel holes mobility. These parametric degradations affect PMOS transistor delay. The impact of NBTI induced threshold voltage degradation on the delay has been analyzed in [9], [11]. However, their analysis do not consider the impact of holes mobility degradation. Holes mobility degradation due to NBTI have a significant effect on transistor parameters [12], [21]. However, a delay degradation model that combines the impacts of hole mobility and threshold voltage degradations on PMOS transistor delay is rarely available.

This paper presents an NBTI induced delay model that considers temperature dependent threshold voltage increment and hole mobility degradation. Initially, we review our previous NBTI analytical model that considers on-chip temperature variations [15]. Thereafter, we analyze the impact of temperature on threshold voltage increment and holes mobility degradation to come up with a new NBTI induced delay model. The main contributions of this paper are:

- Brief review of the most popular NBTI model and discussion of our previous NBTI induced model that consider temperature variation.
- An analytical analysis of NBTI impact on inversion layer hole mobility and threshold voltage under temperature variation.
- A transistor delay model that considers both threshold voltage increment and holes mobility degradation.

The model is simulated on 90nm, 65nm and 45nm transistor nodes under the temperature range of 25-125°C. Simulation results show that by considering mobility degradation the delay increases significantly with the rise in temperature. Additionally, scaled transistors are more sensitive to temperature variations and they reach their degradation's limit earlier at higher temperature.

The rest of the paper is organized as follows. Section II reviews the popular NBTI model and our our previous NBTI model that considers the impact of temperature on all known sub-processes contributing to NBTI degradation [15]. Section III presents transistor delay degradation model that accommodates NBTI induced threshold voltage increment and inversion layer holes mobility degradation. Section IV gives simulation results and their analysis. Finally, Section V concludes the paper.

978-1-4244-7723-4/$26.00 ©2010 IEEE

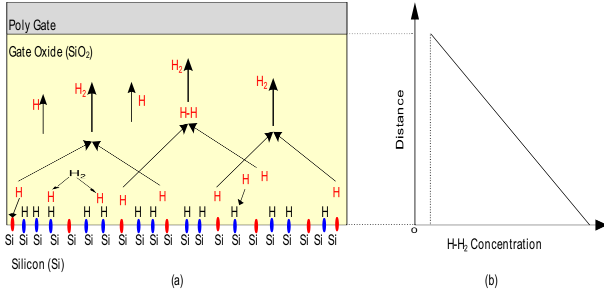


Fig. 1. (a) Schematic view of Si-H bond breaking, atomic and molecular Hydrogen diffusions and their interconversion at Si/Si0$_2$ interface and inside oxide dielectric (b) H and H_2 concentration in oxide layer

II. NBTI Modeling Under Temperature Variation

NBTI was recognized as a reliability concern since 1970s, and the well established Reaction Diffusion (RD) model was presented at that time [5]. The model interprets power law time dependence (t^n) of PMOS degradation due to NBTI, e.g., For threshold voltage increment, $\Delta V_{th} \sim t^n$ [3], [4]. The original RD model assumes a higher time exponent of $n=1/4$ [5]. Later refinements of the model suggest a lower time exponent of $n=1/6$, especially for longer stress time [13]. A recently proposed model [7], [13], initially suggests a higher time exponent, and a lower exponent if stress is maintained for longer time. In the following we review the RD model [13] and our previous temperature aware NBTI model [15].

A. Reaction Diffusion Model

RD model explains the physics of NBTI degradation in terms of different sub-processes. According to the model, NBTI degradation originates from Silicon Hydrogen bonds (≡Si-H) breaking at Silicon-Silicon dioxide (Si-SiO$_2$) interface during negative stress (V_{gs}=-V_{dd}), as shown in Fig. 1(a). The broken Silicon bonds (≡Si-) act as interface traps that cause NBTI degradation. The number of interface traps (N_{IT}) depends on ≡Si-H bond breaking rate (k_f) and ≡Si- bond recovery rate (k_r). The N_{IT} generation rate is given by [3]:

$$\frac{dN_{IT}}{dt} = k_f(N_o - N_{IT}) - k_r N_{IT} N_H^0, \quad (1)$$

where N_o and N_H^0 denote the initial bond density and the atomic Hydrogen density at Si-SiO$_2$ interface. The H atoms released from ≡Si-H bond breaking contribute to three sub-processes including: (a) diffusion towards the gate, (b) combination with other H atoms to produce H_2, or (c) recovery of the broken bonds. Similarly, H_2 participate in the diffusion towards poly gate or in the dissociation to produce H atoms. All these sub-processes are schematically shown in Fig. 1(a) [13]. Obviously these sub-processes determine the N_{IT} count. These sub-processes are formulated as [7]:

$$\frac{dN_H}{dt} = D_H \frac{d^2 N_H}{dx^2} - k_H N_H^2 + k_{H_2} N_{H_2}, \quad (2)$$

$$\frac{dN_{H2}}{dt} = D_{H2} \frac{d^2 N_{H2}}{dx^2} + \frac{1}{2} k_H N_H^2 - k_{H2} N_{H2}, \quad (3)$$

where N_H and N_{H_2} are densities, D_H and D_{H_2} are diffusion rates of atomic and molecular Hydrogen, while k_H and k_{H_2} are interconversion rates of H and H_2 respectively.

Initially, the bond breaking and bond recovery sub-processes dominate at the Si-SiO$_2$ interface. While, the diffusing species in SiO$_2$ layer is mainly atomic Hydrogen. However, if the stress is maintained for longer time, most of the H atoms are converted to H_2. Hence, sub-processes related to H_2 become dominant. The diffusion in SiO$_2$ layer becomes H_2 dominated. Under such conditions the N_{IT} is obtained by solving Eq. 1 and Eq. 3 [21]:

$$N_{IT}(t) = \left(\frac{k_f N_o}{k_r}\right)^{2/3} \left(\frac{k_H}{k_{H_2}}\right)^{1/3} (6D_{H2}t)^{1/6}. \quad (4)$$

The equation shows that interface traps generation process manifest itself from different sub-processes. These sub-processes have field and/or temperature dependencies that must be considered for accurate NBTI modeling.

B. NBTI Model with Temperature Variation

RD model assumes that NBTI degradation is temperature dependent, but does not give any physical basis for such dependency [21]. Similarly, the origin of temperature increment in scaled PMOS transistors and its impact on NBTI degradations have not been explored in the model. In this subsection, we describe our previous work related to the origin of temperature increment in scaled PMOS transistors and accommodate its impact in RD model sub-processes [15].

In order to meet the 30% delay reduction in each successive technology generation, the hole speed in PMOS inversion layer has to increase. The fast moving holes come closer to ≡Si-H bonds at Si-SiO$_2$ interface. Approximately, 0.2-0.3eV energy is consumed to bring a hole close to ≡Si-H bond [14]. The interaction results in breaking of ≡Si-H bond, producing an interface trap and H atom with 1.3eV energy release. Therefore, the net energy gain in a single interface trap production is 1.1eV [14]. The gain raises temperature to T_{max} from a reference temperature T_{ref} (25°C). Some of the released energy is consumed by recovery of the broken ≡Si- bonds. Therefore, temperature $T(t)$ at any stress instant t can be modeled as [9]:

$$\begin{aligned} T(t) &= [(1/2)(T_{max} + T_{ref})] \\ &+ [(1/2)(T_{max} - T_{ref}) sin(2\pi f t)], \quad (5) \end{aligned}$$

where f is the thermal frequency. The impacts of temperature increments on rate co-efficients e.g. D_H, D_{H_2}, k_H, k_{H_2}, k_f and k_r of RD model are described below.

Temperature dependence of diffusion rates

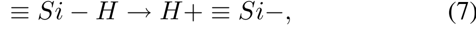
The diffusion sub-processes in oxide layer follow Fick's law, e.g., D_H decreases linearly with decreasing H density from Si-SiO$_2$ interface as shown in Fig 1(b) [3]. Temperature variation strongly affects the diffusion rates D_H and D_{H_2}. The effect is based on Arrhenius relation, which can be written as [3]:

$$D_H = D_{H_o} exp\left(-\frac{E_a}{kT}\right), \quad (6)$$

where D_{H_o} is the diffusion rate at T_{ref}, E_a is the activation energy, k is Boltzmann's constant, and T is temperature. The equation shows that the temperature increment accelerates D_H. Such an acceleration towards the gate attenuates the ≡Si-broken bond recovery sub-process at Si-SiO_2 interface and increases the N_{IT}.

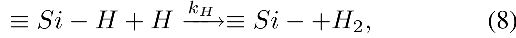
Temperature dependence of conversion rate

The negative gate stress breaks ≡Si-H bonds at Si-SiO_2 interface resulting in ≡Si- broken bonds and H atoms by:



$$\equiv Si - H \rightarrow H + \equiv Si-, \tag{7}$$

most of the H atoms released convert to H_2 molecules. The H to H_2 conversion at Si-SiO2 interface and inside SiO_2 is a complex mechanism. We assume that the conversion takes place when a free H atom approaches a ≡Si-H bond within a distance of $r_H < 1.0$nm and breaks it by reaction [16]:



$$\equiv Si - H + H \xrightarrow{k_H} \equiv Si - + H_2, \tag{8}$$

where k_H is the rate constant of H to H_2 conversion. The temperature impact on conversion can be understood by inspecting the rate constant k_H as:

$$k_H[T(t)] = 4 \times \pi . D_H[T(t)].r_H.\xi_{1(x)}. \tag{9}$$

For atomic Hydrogen diffusion the parameter $\xi_1(x)$ is equal to $\sim 10^{-4}$. Temperature impact on k_H comes from two parts. First, since the conversion takes place when Hydrogen approaches at distance $r_H < 1.0nm$ to a ≡Si-H bond, the Hydrogen diffusion is involved, and (see Eq. 6 which shows the temperature dependence of diffusion). Second, at higher temperature the ≡Si-H bonds vibrate that bring H atoms, ≡Si-H at $r_H < 1.0nm$, and hence accelerate k_H sub-process.

Temperature dependence of reaction rates

The N_{IT} during stress phase mainly depends on ≡Si-H bond breaking and ≡Si- broken bond recovery sub-processes. The sub-processes rates k_f and k_r depend on oxide layer temperature. The dependence can be expressed as:

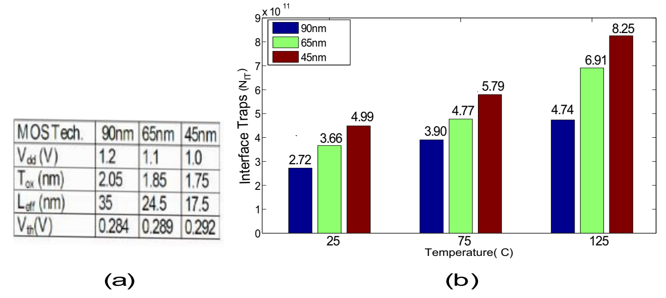
$$k_f T[(t)] \propto E_{ox}.exp(E_{ox}/E_o).exp(E_a(k_f)/E_o)/kT(t),$$
$$k_r T[(t)] \propto exp(E_a(k_r)/E_o)/kT(t), \tag{10}$$

where E_{ox} is the oxide field, E_o is field acceleration constant, and $E_a(k_f)$, $E_a(k_r)$ are k_f and k_r activation energies respectively. At intermediate and longer stress time, both k_f and k_r take place in parallel. Under this condition ratio between k_f and k_r is used as given by [3]:

$$\frac{k_f}{k_r} \propto E_{ox}exp(E_{ox}/E_o)exp[-E_a(k_f) + E_a(k_r)]/kT. \tag{11}$$

The quick recovery of ≡Si- bonds during recovery phase suggests that $E_a(k_f) \approx E_a(k_r)$. If the E_a's were different, it would be impossible for H atoms to recover ≡Si- bonds. Considering $E_a(k_f) \approx E_a(k_r)$, we obtained:

$$\frac{k_f}{k_r} \propto E_{ox}exp\left(\frac{E_{ox}}{E_o}\right), \tag{12}$$



MOS Tech.	90nm	65nm	45nm
V_{dd} (V)	1.2	1.1	1.0
T_{ox} (nm)	2.05	1.85	1.75
L_{eff} (nm)	35	24.5	17.5
V_{th}(V)	0.284	0.289	0.292

Fig. 2. (a) Equivalent parameters of PTM models (b) Number of Interface traps in different technologies at different temperatures

The equation shows that when k_f and k_r take place in parallel, the reaction rates become temperature independent.

In conclusion, Eq. [6,9,10,12] present the temperature impact on NBTI sub-processes. By considering these impacts, the temperature dependent N_{IT} during negative stress is given by:

$$N_{IT(T(t))} = (N_o.E_{ox}exp(E_{ox}/E_o))^{2/3}.(k_H[T(t)]/k_{H2})^{1/2} \times (D_{H2}[T(t)].t)^{1/6}. \tag{13}$$

We consider equivalent parameters for 90nm, 65nm and 45nm transistor models from [20], and take three temperatures 25°C, 75°C, and 125°C to represent temperature variations of modern microprocessor chips. Numeric simulation results of the above equation are given in Fig. 2. During simulation we keep the transistor dimensional ratio i.e. W/L constant as we move from one temperature to another. The N_{IT} generation phenomenon is simulation time is 10^5seconds. Analysis of the figure shows that:

- The temperature increment accelerates NBTI sub-processes and increases N_{IT} count. For example, for 65nm technology the N_{IT} is 3.66×10^{11} at 25°C, while the count approaches to 6.91×10^{11} at 125°C.
- For a given range of temperature and stress duration, the increment in N_{IT} count is higher for smaller technologies. For example, for 90nm and temperature increment from 25°C to 125°, the increment in N_{IT} is 2.02×10^{11}. However, for 65nm and 45nm the N_{IT} increment reach to 2.94×10^{11} and 3.26×10^{11} respectively.

III. NBTI Induced Delay Model

In this section we develop an NBTI induced PMOS transistor delay model. First, NBTI impact on two transistor parameters namely the threshold voltage and channel hole mobility is presented. Thereafter, a transistor delay model that considers the two parameters is discussed.

A. Transistor Parameters Degradation

The N_{IT} build up at the Si-SiO_2 interface directly impact transistor parameters namely the threshold voltage V_{th} and the effective hole mobility μ_{eff}.

Threshold Voltage Degradation

The threshold voltage V_{th} of a PMOS transistor is [14]:

$$V_{th} = V_{FB} + V_{OX} + \phi s \tag{14}$$

where V_{FB} is the flat band voltage, V_{OX} is the oxide potential and ϕs is the surface potential. At the flat band condition V_{OX}=ϕs=0. This implies that no charges exist in the SiO_2 layer or at Si-SiO_2 interface. Under this condition the threshold voltage is equal to flat band voltage, which is given by [14]:

$$V_{FB} = \psi_M - \psi_S \quad (15)$$

where ψ_M and ψ_S are the gate and Si work functions. In case of any charge inside oxide layer or at Si-SiO_2 interface, the flat band voltage degradation is given by:

$$V_{FB} = \phi_{MS} - \frac{Q_{int}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}} \quad (16)$$

where ϕ_{MS} is the work function difference, C_{ox} is the oxide capacitance, Q_{ox} is the charge inside oxide and Q_{int} is the positive charge at the Si-SiO_2 interface.

NBTI produces charges both at Si-SiO_2 interface and inside the oxide layer [21]. However, for simplicity we assume that charges inside oxide layer have negligible impact [3]. Under this assumption, we have Q_{ox}=0 and Q_{int}=qN_{IT}. So the flat band voltage is a function of temperature dependent N_{IT}. Since, we have assumed that Q_{ox}=0, the threshold voltage will be affected by the flat band voltage only. The threshold voltage shift is given by:

$$\Delta V_{th} = \Delta V_{FB} = -\frac{qN_{IT}}{C_{ox}} \quad (17)$$

The equation shows threshold voltage shift depends on the temperature dependent interface traps.

This voltage shift generated due to NBTI mechanism is an extra voltage and must be added to the charge free threshold voltage. The time required to overcome the voltage shift increases the delay of PMOS transistor.

Hole Mobility Degradation

Hole mobility in the inversion layer depends on external voltages, device structure and temperature. These parameters contribute to three scattering mechanisms namely Coulomb, phonon and surface roughness scattering Islam. Combined impact of these mechanisms on effective holes mobility μ_{eff} is based on Mathiessen's rule as Islam:

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_{PH}} + \frac{1}{\mu_{SR}} + \frac{1}{\mu_C} \quad (18)$$

where μ_{PH}, μ_{SR} and μ_C are phonon, surface and Coulomb scatterings respectively. Temperature impact on mobility degradation can be explained by investigating phonon and coulomb scatterings. First, the phonon scattering originates from vibration of atoms and collisions with other atoms in the lattice that disturbs holes movement in the channel. The hole scattering rate due to phonon mechanisms is proportional to the atomic mean free time (τ_{PH}) between collisions; i.e. $\mu_{PH} \propto 1/\tau_{PH}$. Phonon scattering increases with rise in temperature due to fast atomic vibrations at higher temperatures that decreases the mean free time. Second, Coulomb scattering arises from Coulombic forces between similar or opposite charges that scatters carrier moving in the channel.

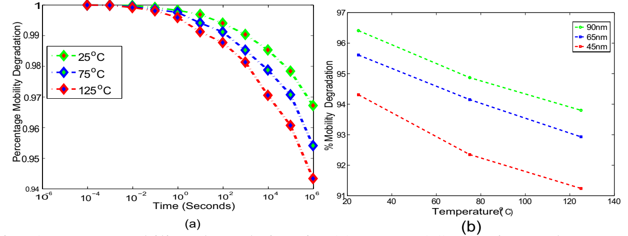


Fig. 3. (a) Mobility degradation in 90nm PMOS transistor, (b) Percent mobility degradation in different technology nodes at various temperatures

The charges contributing to Coulomb scattering are charges in the oxide layer, ionized impurities, and N_{IT} at Si-SiO_2 interface. Contribution of each charge type depends on the operating temperature. At lower temperature, Coulomb scattering is mainly dominated by the oxide charges and the impurity charges . However, at higher temperature, interface traps are main contributor to Coulomb's scattering [17], [19]. The contribution can be expressed as:

$$\frac{1}{\mu_C} = \frac{1}{\mu_{Cbo}} \left(\frac{10^{18}}{N_B + N_{IT(T(t))}/z} \right)^{-1} \left(\frac{10^{12}}{Q_{inv}} \right)^{\alpha}, \quad (19)$$

where μ_{Cbo} is pre-stress hole mobility, N_B is substrate doping density, z is channel thickness, and Q_{inv} is the inversion layer charge. In above equation μ_{Cbo} and N_{IT} are continuous function of temperature. Due to temperature dependence of phonon and Coulomb scatterings the mobility becomes a strong function of temperature. Using equivalent parameters of [20] and N_{IT} of eq. [13, 18 and 19], the numeric simulation for mobility degradation has been performed; the results are shown in Fig. 3. They reveal that for 90nm mobility degrades as the temperature increases reaching 6% at 125°C. Additionally, the degradation is more significant in smaller technologies. For example, the mobility degradation is 6% for 90nm, while it reaches 9% for 45nm transisor node.

The NBTI induced degradation of the channel hole mobility is equivalent to a drain-source parasitic resistance. The resistance opposes drain-source current flow resulting in additional transistor delay.

B. Transistor Delay Model

So far, we have analyzed temperature impact on NBTI induced threshold voltage increment and hole mobility degradation. But, to analyze temperature impact at the circuit level, it is important to make a link e.g. between transistor parameters such as threshold voltage and mobility and transistor's delay.

The NBTI induced ΔV_{th} and $\Delta\mu_{eff}$ degradations [see Eq. 17 and 19], effect the delay of the PMOS transistor. Generally, the delay (t_d) dependence on threshold voltage and mobility degradation can be written as [11]:

$$t_d = \frac{C_L V_{ds}}{I_D} = \frac{\mu_{eff}.\beta}{(V_g - V_{th})^{\alpha}} \quad (20)$$

where

$$\beta = \frac{LC_L V_{dd}}{WC_{ox}}$$

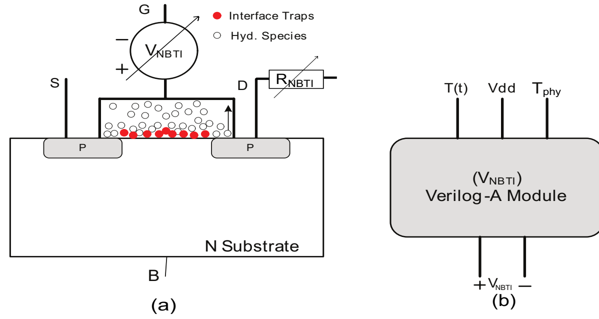


Fig. 4. (a) PMOS transistor degradation model due to NBTI. (b) The Verilog-A source representing NBTI degradation at different temperatures.

V_g and V_{dd} are gate and drain voltages of the transistor respectively, α is the velocity saturation index; C_L, C_{eff}, and W_{eff} are load capacitance, effective capacitance, and channel width respectively. In order to get the additional delay due to threshold voltage and mobility degradation, we expand the delay equation. After neglecting the higher order terms we get:

$$\Delta t_{d(T(t))} = \frac{\alpha \Delta\mu_{eff} \Delta V_{th}}{(V_{gs} - V_{th})} . t_{do} \quad (21)$$

where t_{do} is the transistor delay at T_{ref}, and $\Delta t_{d(T(t))}$ PMOS transistor delay that consider threshold voltage and mobility degradations under temperature variation.

IV. Simulation Results and Discussion

In this section, we present simulation results of temperature impact on NBTI and key insights observed. We use PTM 90nm, 65nm and 45nm Bulk PMOS transistor models.

The NBTI impact on PMOS transistor threshold voltage is modeled using an external voltage source (V_{NBTI}) as shown in Fig.4(a). Similarly, the holes mobility degradation is modeled using an external resistance (R_{NBTI}). Behaviors of V_{NBTI} and R_{NBTI} are defined using a Verilog-A modules; e.g., the external voltage source V_{NBTI} is shown in Fig. 4(b). Inputs of this module are the temperature T(t), supply voltage V_{dd} and transistor physical parameters T_{phy} (i.e. T_{ox}, L and W).

The simulation results of temperature impact on NBTI induced threshold voltage shift and delay are reported in the following sub-sections.

A. Threshold voltage shift

The most obvious impact of NBTI is the increase in threshold voltage of PMOS transistor. Fig. 5 validates this increment for different technologies. From the figure we can conclude that:

- For a given PMOS transistor and stress duration, the threshold voltage shift increases with temperature increment. For instance, after 10^5sec stress on 65nm PMOS transistor the threshold voltage shift is 18 mV at 25°C. However, the shift approaches 26 mV at 125°C. Therefore, a PMOS transistor will degrade ahead of predicted lifetime at high temperature.
- Operation under higher temperature (e.g. 125°C) and stress time (10^5sec) causes higher voltage shift in 45nm PMOS transistor (approx. 42%) as compared to 90nm PMOS transistor (approx. 34%). Therefore, under same operating conditions 45nm PMOS transistors will early reach the limit of degradation.

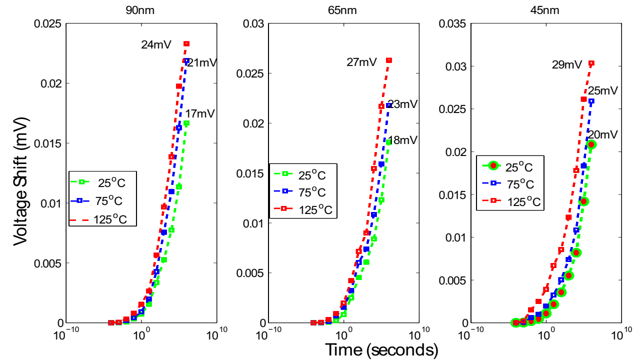


Fig. 5. Threshold voltage shift due to NBTI degradation

B. NBTI Induced Delay

NBTI degradation significantly effects PMOS transistor delay. The delay results from threshold voltage increment and inversion layer mobility degradation. We divided our experiment into two steps. First, we performed the simulation by ignoring the mobility degradation and then by including its impact. The results are described below.

NBTI Induced Delay: Mobility degradation excluded

We measured the PMOS transistor delay at time $t = 0$sec and after 10^5sec stress for each technology (e.g. 90nm, 65nm and 45nm) at 25°C, 75°C and 125°C are shown in Fig. 6. The figure shows time and temperature dependencies of the delay degradation. From the figure we can observe two obvious trends:

- For a given PMOS technology and temperature the delay degradation increases with increase in stress time. For example, after 10^{-3}sec the degradation of 90nm PMOS transistor at 25°C is 0.0%. However, if the stress is maintained for 10^{+5}sec at 25°C, this reaches to 2.63%.
- For a given stress time and temperature the delay degradation is very significant for smaller PMOS transistors. For instance, after 10^5sec stress at 125°C temperature, the degradation for 90nm PMOS is approximately 4.87%. However, under the same temperature, the delays for

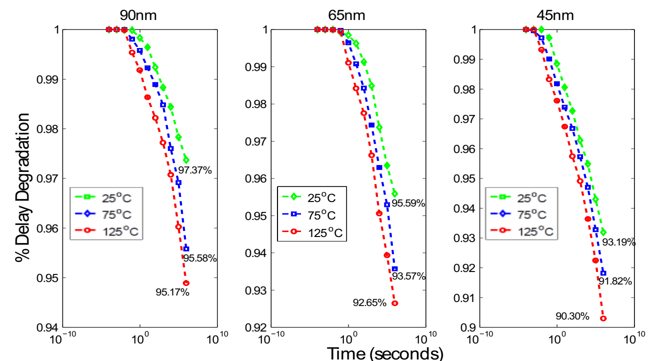


Fig. 6. Percent delay degradation due to threshold voltage shift

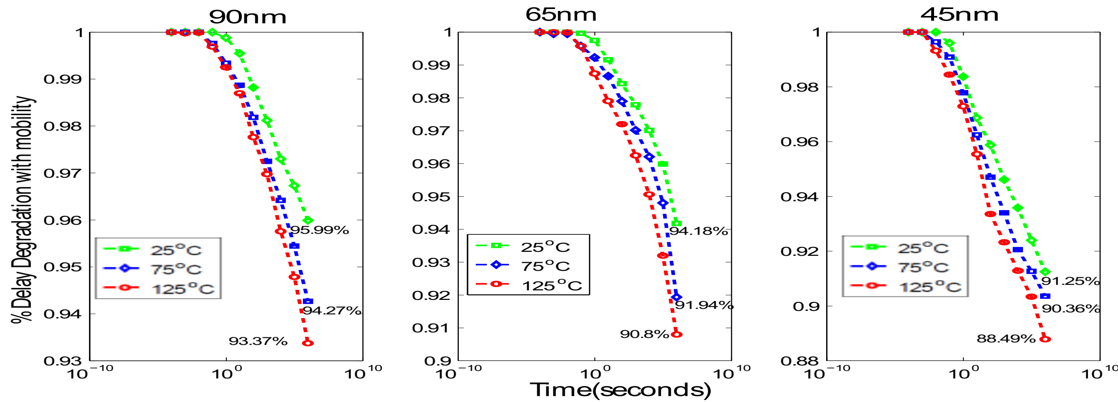


Fig. 7. Percent delay degradation with mobility degradation.

65nm and 45nm technologies are approximately 7.35% and 9.70%, respectively. Our analysis is consistent with Paul's analysis [11] and showed that percent of delay is approximately 4 times less than that of the threshold voltage shift. However, both results are optimistic because the impact of mobility degradation are neglected in these analyses.

NBTI Induced Delay: Mobility degradation included

It has bees shown in Section II-A (see Fig. 3) that interface traps at Si-SiO_2 interface degrades holes mobility in the channel. This degradation decreases the drain current and hence increases transistor delay. Fig. 7 shows the percent of delay increment by considering both the NBTI induced threshold voltage shift and mobility degradation under temperature variation. The Figure shows that the delay due to mobility degradation has the same trends in all technologies. However, the impact of mobility increases in smaller technologies. From the Figure, we can conclude that :

- The impact of mobility on delay increases with temperature. For instance, in 90nm transistor after 10^{+5}sec stress at 25 ^oC, the additional delay due mobility degradation is 1.30% (comparing Fig. 6 and 7). However, If temperature increases to 125°C, the additonal delay degradation reaches 1.82%.
- The impact of mobility degradation on PMOS transistor delay gets worst as technology scales down. For example, for 90nm PMOS transistor at 125°C overall delay (considering both threshold voltage shift and mobility degradation) is 6.63%. However, under the same temeperature, the overall delay reaches 9.20% for 65nm and 11.50% for 45nm PMOS transistor technologies.

V. Conclusion

In this paper we proposed an analytical model for NBTI induced delay that consider both threshold voltage shift and holes mobility degradation under temperature variation. We observed that by neglecting mobility degradation the PMOS transistor delay after 10^5 seconds at 125 ^oC reaches 4.83%, 7.35% and 9.70% in 90nm, 65nm and 45nm PMOS transistors respectively. However, by considering both the threshold voltage shift and the hole mobility degradation NBTI induced delay at 125°C reaches to approximately 6.63%, 9.2% and 11.5% in 90nm, 65nm and 45nm in PMOS transistors respectively.

References

[1] S. Borkar, et al., "Micro architecture and Design Challenges for Giga Scale Integration", *Proc. of Intl. Sympos. on Micro Architecture*, pp:3-3, 2004.
[2] N. Kizmuka "The Impact of BTI for Direct Tunneling Ultra Thin Gate Oxide of MOSFET Scaling", *Sympos. on VLSI Technology*, pp:73-74, 1999.
[3] M.A. Alam, et al., "A Comprehensive Model of PMOS NBTI Degradation", *Microelectronics Reliability* , Vol:45, Issue:1, pp:71-81, 2005.
[4] W. Abadeer, et al., "Behaviour of NBTI Under AC Dynamic Circuit Conditions", *Proc. of IPRS*, 2003.
[5] K.O. Jeppson, et al., "Negative bias stress of MOS devices at high electric fields and degradation of MOS devices", *Journal of Applied Physics* , Vol:48, Issue:5, pp:2004-2014, 1977.
[6] R. Vattikonda, et al., "Modeling and Minimization of PMOS NBTI Effect for Robust meter Design", *Pro. of DAC*, pp:1047 - 1052 , 2006.
[7] A.E. Islam, et al., "Recent Issues in NBTI: Initial Degradation, Field Dependence of Interface Traps Generation, Hole Trapping Effect, and recovery", *IEEE Transaction on Electron Devices* , Vol.54, Issue: 9, pp: 2143-2154, 2007.
[8] J.D. Warnock, et al., "The circuit and physical design of the POWER4 microprocessor", IBM Journal of Research and Development, Vol. 46, Issue. 1, 2002.
[9] H. Luo, et al., "Modelling of PMOS NBTI Effect Considering Temperature Variation", *Pro. of 8th ISEQD*, pp:139-14, 2007.
[10] B. Zhang, et al., "Modeling of NBTI Induced PMOS Degradation Under Arbitrary Dynamic Temperature Variation", *Proc. of ISQED*, pp:774-779, 2007.
[11] B.C. Paul, et al., "Impact of NBTI on Temporal Degradation of Digital Circuits", *Electronics Device Letter*, Vol.26, No:8, 2005.
[12] A.T. Krishnan, et al., "NBTI Impact on Transistor and Circuit: Model, Mechanisms and Scaling Effects ", *Pro. of IEDM*, pp:349-352, 2003.
[13] H. Kufluoglu, et al., "A Generalized Reaction-Diffusion Model With Explicit H-H_2 Dynamics for NBTI", *IEEE Trans. on Electron Devices*, pp:1101-1107, May 2007.
[14] S.N. Rashkeev, et al., "Defect Generation by Hydrogen at the Si-SiO_2 Interface", *Physics Review Letter* , Volume: 87 , No: 16 , Oct 2001.
[15] S. Khan and S. Hamdioui, "NBTI Modeling in the Framework of Temperature Variation", *to appear in DATE 2010*.
[16] G.V. Gadiyak, "Hydrogen Redistribution in Thin Silicon Dioxide Films Under Electron injections in High Field", *Journal of Applied Physics* , Vol:82, 1997.
[17] F. Stern, "Calculated Temperature Dependence of Mobility in Silicon Inversion Layer", Physical Review Letter, Vol.44, No. 22, 1980.
[18] S. Takagi, et al., "On the University of Inversion-layer Mobility in the N- and P-channel MOSFET's", Proc. of IEDM, 1988.
[19] B. Cheng, et al., "A Temperature Dependent MOSFET Inversion Layer of Carrier Mobility Model for Device and Circuit Simulation", *IEEE Trans. on Electron Devices* , pp:343-345, Feb 1997.
[20] W. Zhao, et al., "New Generation of Predictive Models for sub-45nm Design Exploration", *Proc. of ISQED*, pp: 585-590, 2006.
[21] A.E. Islam, et al., "Mobility degradation due to interface traps in plasma oxynitride PMOS devices", *Proc. of IPRS*, pp: 87-96, 2008.