Transition Fault Testing for Offline Adaptive Voltage Scaling

Mahroo Zandrahimi[*], Philippe Debaud[+], Armand Castillejo[+] and Zaid Al-Ars[*]
Delft University of Technology, The Netherlands[*], STMicroelectronics, Grenoble, France[+]

Abstract

In this paper, we propose using transition fault test patterns to perform adaptive voltage scaling (AVS) as a low-cost alternative to process monitoring boxes (PMBs) while improving accuracy of voltage estimation. The paper discusses a case study on real silicon comparing the accuracy of voltage estimation using PMBs and the TF-based approach on a 28nm FD-SOI device. The results show that the PMB approach can only account for 85% of the variability in the measurements, while the TF-based approach can account for 99% of that variability.

1. Introduction

AVS has been used widely to compensate for process, voltage, and temperature variations as well as power optimization of integrated circuits. The current industrial state-of-the-art AVS approaches embeds several PMBs on chip so that based on the frequency responses of these monitors during production, the chip performance is estimated and the optimal voltage is adapted exclusively to each operating point of each manufactured chip [1,2]. PMBs have shown some limitations in terms of cost and accuracy that limit their benefit [3]. This paper proposes using TF testing during production as an alternative approach that is both cheaper and more accurate. Since transition fault testing covers many path-segments of the design [4], it can be a better performance representative than a PMB.

Here, we propose a flow of the TF-based AVS approach that could be used during production. The proposed flow performs a binary search to identify the minimum voltage (Vmin), at which the chip can pass all TF test patterns. The following steps are performed for each operation point of the chip: 1) Apply chip setup at nominal values and initialize variables; 2) Set supply voltage to Vmax and wait for stabilization; 3) Apply transition fault at speed test; 4) If the chip fails the test, discard it, otherwise; 5) compute new values and do a binary search to find Vmin.

2. Industrial case study

In this section, we compare PMB versus TF for AVS during production using measurements on real silicon. Our case study is a 28nm FD-SOI device on which a number of PMBs are distributed. During the characterization phase of chip production, the correlation between frequency of PMBs and the actual frequency of the device is measured for a number of chips representative of the process window so that during production, and according to the frequency responses of PMBs, optimal voltage estimation is done for each chip. Alternatively, voltage estimation can be done using transition fault testing during production as well at no extra costs. Also, since transition fault testing represents a direct measurement of chip performance, the expensive correlation during the characterization phase is not needed anymore, which reduces time to market dramatically.

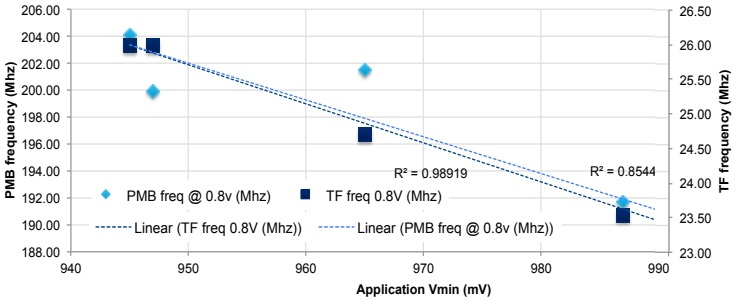

Figure 1. Application Vmin versus TF and PMB results

We have done silicon measurement on 5 chip samples. First, we have measured the real value of optimal voltage (Vmin) for each chip operating at its nominal frequency using functional patterns. To understand whether PMB or TF is more accurate for performance prediction, we have to identify which of them is more correlated with application Vmin. Therefore, we mapped both frequency response of PMB and the TF frequency to the Vmin of the chip in which that PMB is located. Then, we performed a linear least square regression analysis of the correlation between application Vmin and PMB frequency as well as the TF frequency, and measured the coefficient of determination (R^2) for both correlation functions. R^2 is a key output of regression analysis. It is interpreted as the proportion of the variance in the dependent variable (Vmin in this case) that is predictable from the independent variable (PMB frequency and TF frequency). Results are presented in Figure 1. R^2 for the correlation of application Vmin versus PMB is 0.85, while it has a value of 0.99 for the correlation versus TF, which means that Vmin estimation using the PMB approach can only account for 85% of the variability in the measurements, while Vmin estimation using the TF approach can account for 99% of that variability. These results confirm that we can achieve higher accuracy in Vmin estimation using TF.

3. References

[1] M. Zandrahimi and Z. Al-Ars, A Survey on Low-power Techniques for Single and Multicore Systems, in ICCASA, pp. 69-74, 2014.
[2] Q. Liu and S.S. Sapatnekar, Capturing Post-Silicon Variations Using a Representative Critical Path, in TCAD, vol. 29, no. 2, pp. 211-222, 2010.
[3] M. Zandrahimi, Z. Al-Ars, P. Debaud, and A. Castillejo, Challenges of Using On-Chip Performance Monitors for Process and Environmental Variation Compensation, in DATE, 2016.
[4] B. Kruseman, A. Majhi, and G. Gronthoud, On Performance Testing with Path Delay Patterns, in VTS, 2007.